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PART NUMBER
R6531

Rockwell

R6500 Microcomputer System

DATA SHEET

ROM-RAM-I/O-COUNTER (RRIOC)

SYSTEM ABSTRACT

The ROM-RAM-I/O Counter (RRIOC), Part Number R6531, further enhances the cost-effectivity of the R6500 NMOS 8-bit microcomputer system by providing a powerful, flexible two-chip minimum system option. Produced with N-channel depletion load, silicon gate technology, the R6500 system employs advanced architecture, including 13 instruction addressing modes to achieve third generation performance speeds and smaller chips, the threshold to lower hardware and design costs. Included in the R6500 system are 10 software-compatible microprocessor (CPU) options, a growing number of memory and I/O devices, a very efficient, low-cost SYSTEM 65 development aid and complete documentation.

DESCRIPTION

The R6531 is primarily designed to provide innovative Equipment Designers with a wide span of two-chip minimum systems in combination with the R6500 family of 10 CPUs. It can also be combined in a variety of multi-chip system configurations with other R6531's, ROMs, RAMs and other I/O devices.

There are two R6531 versions: a 40-pin dual-in-line package; another with expanded I/O in a compact 52-pin quad-in-line package — see Table I. Both versions contain a 2048 x 8 mask-programmable ROM, a 128 x 8 static RAM, a software programmable multi-mode counter, an 8-bit serial data channel, and 15 bidirectional data lines (two ports) with a handshake control mode and four interrupts inputs. The 52-pin version has an 8-bit output port and a 4-bit input port for a total of 27 I/O lines. Several mask options are available to provide a RAM standby power pin and chip selects for multi-chip systems — see Figure 1.

A 52-pin, quad in-line prototyping circuit is also available in 1- and 2-MHz versions. The order numbers are R6531-099 and R6531-099A, respectively.

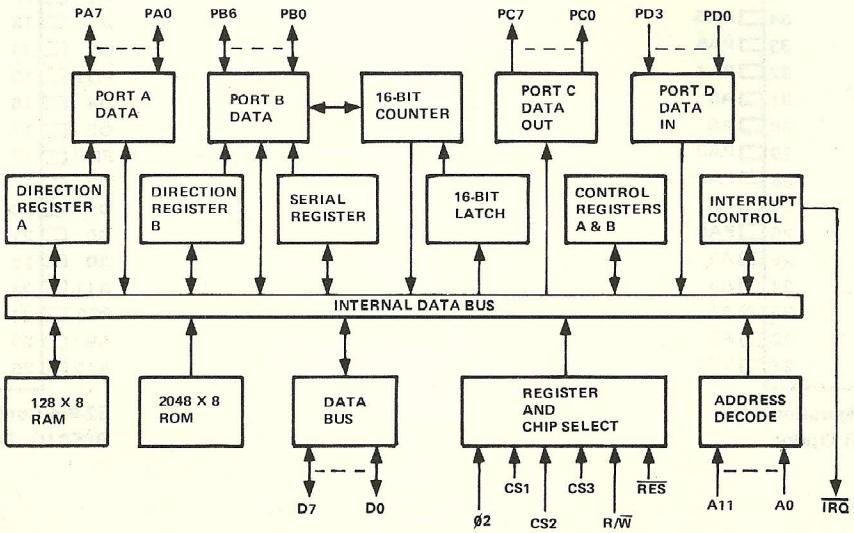
FEATURES

- 2048 x 8 mask programmable ROM
- 128 x 8 static RAM
- 16-bit multi-mode counter/latch
  - interval timer (one shot or free running)
  - pulse generator (one shot or free running)
  - event counter
- 8-bit serial channel
- TTL compatible I/O, drive one TTL load
- 15 bidirectional I/O lines (2 ports — 40 pin package)
- Expansion 8-bit output port and 4-bit input port (52 pin package)
- I/O handshake control
- Four edge sensitive interrupt inputs
- 2 MHz or 1 MHz operation
- Single +5V power supply

Table 1 Ordering Information

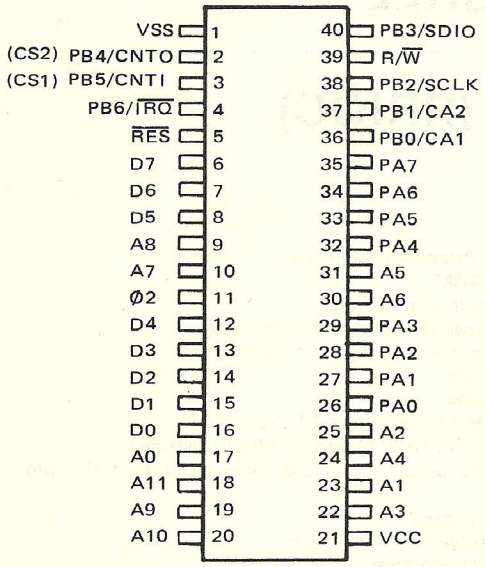
Order Number: R6531

- Temperature Range:
  - No suffix = $0^{\circ}C$ to $+70^{\circ}C$
  - E = $-40^{\circ}C$ to $+85^{\circ}C$ (Industrial)
- Package:
  - C = 40-Pin DIP, Ceramic
  - P = 40-Pin DIP, Plastic
  - Q = 52-Pin QUIP, Plastic
- Frequency Range:
  - No suffix = 1 MHz
  - A = 2 MHz

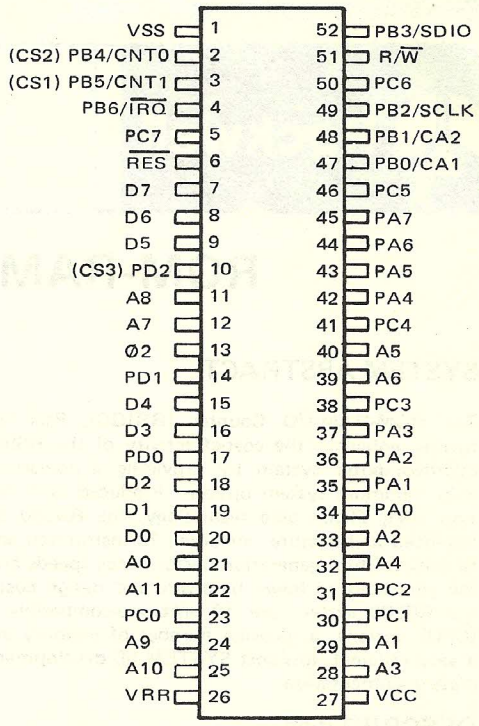


R6531 Block Diagram

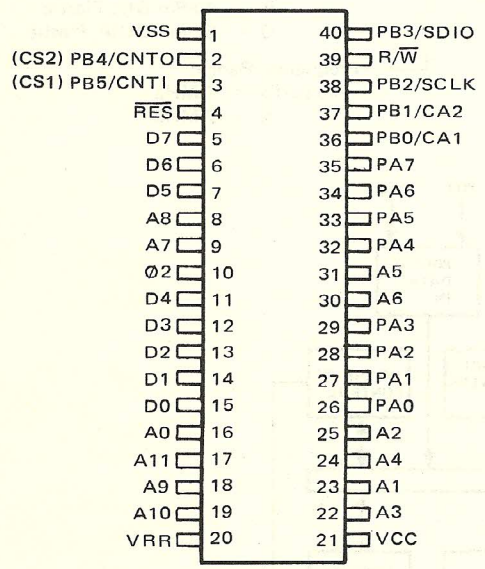
Specifications subject to change without notice



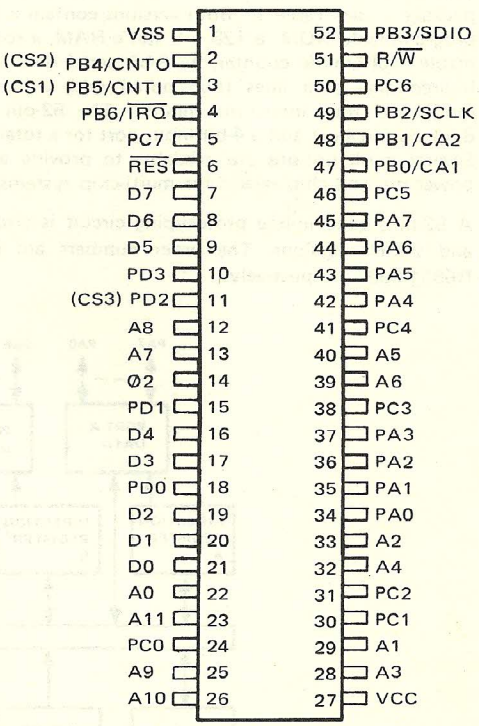
40- Pin Configuration
R6531, PB6 Option



52-Pin Configuration
R6531Q, VRR Option



40-Pin Configuration
R6531, VRR Option



52-Pin Configuration
R6531Q, PD3 Option

Figure 1. R6531 Pin Configuration Options

INTERFACE SIGNALS

RESET ($\overline{RES}$)

This active, low signal is used to initialize the R6531. It clears all internal registers (except the counter and serial registers) to logic zero. This action places all bidirectional I/O lines in the input state and the Port C outputs in the high state. The timer, shift register, and interrupts are disabled. The $\overline{RES}$ signal must be low for at least four clock periods when reset is required.

ADDRESS BUS (A0-A11) AND CHIP SELECTS (CS1-CS3)

Memory and register selection is accomplished using the 12 address lines and in multiple device systems also using one or more of the three Chip Select mask options. When PB4, PB5, or PD2 are chosen as chip selects, they cannot be used as peripheral I/O pins.

DATA BUS (D0-D7)

The R6531 has eight data bus lines. These lines connect to the microcomputers data bus and allow transfer of data to or from the microprocessor. The output buffers remain in the off-state except when the R6531 is selected for a read operation.

READ/WRITE (R/$\overline{W}$)

The R/$\overline{W}$ signal is supplied by the microprocessor and is used to control the transfer of data to and from the microprocessor and the R6531. A high on the R/$\overline{W}$ pin allows the processor to read (with proper addressing) the data supplied by the R6531. A low on the R/$\overline{W}$ pin allows a write (with proper addressing) to the R6531.

PERIPHERAL DATA PORTS (PA0-PA7, PB0-PB6, PC0-PC7, PD0-PD3)

Both versions of the R6531 have 15 pins available for peripheral I/O operations. Each pin is software programmable to act as an input or an output. The pins are grouped into an 8-bit port, PA0-PA7, and a 7-bit port, PB0-PB6. The lines of the PB port may serve other functions. Ports PA and PB have associated data direction registers.

The expanded I/O of the 52-pin version provides an 8-bit output only port, PC0-PC7, and a 4-bit input only port, PD0-PD3. PD2 and PD3 may be assigned other functions as described herein.

The outputs are push/pull type drivers capable of driving a single TTL load. When inputs are selected the lines float. If PB6 is programmed as the $\overline{IRQ}$ request output, the line is driven low and requires an external pull-up, thus allowing the wire OR-ing of $\overline{IRQ}$ from other devices.

RAM RETENTION VOLTAGE (VRR)

A separate pin for a power supply for the read/write memory is available as a mask option. This allows the retention of RAM data by using a battery back-up for the RAM only. Pin PB6 in the 40-pin version or PD3 in the 52-pin version is mask programmable as the VRR pin. Address line A10 must be held in the logic state which deselects RAM (user-defined) in order to protect the RAM data when VCC falls below the specified level or is turned off.

INTERNAL ORGANIZATION

The R6531 is divided into three basic functions: ROM, RAM, and I/O. The selection of any one of these three is accomplished by issuing the appropriate address information on the address bus when the chip is selected.

ADDRESSING

Addressing of the R6531 offers many variations to the user for system configuration flexibility. Combination with other R6531's, ROMs, RAMs or I/O devices is possible without need for external address decoding. Each of the three basic functions on the device has its own decode mask for unique selection.

The specific address ranges and chip selects are defined by the user and are dependent on the number of chips in the system. The programmed options to be fixed by masking are:

R6531 Function	Chip Selects			Address Inputs (A0-A11)											
	CS3	CS2	CS1	11	10	9	8	7	6	5	4	3	2	1	0
ROM	X	X	X	X	2K ROM Decode										
RAM	Y	Y	Y	Y	Y	Y	Y	Y	128 RAM Decode						
I/O	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	I/O Decode		

The X, Y, and Z bits may be selected as high, low or no effect.

The chip select pins are also discrete I/O pins PB5, PB4, and PD2. The pins are independent of each other in that any one may be used as a chip select. The user specifies as mask options which pins are to be used as I/O and which as chip selects.

ROM – 2K BYTES (16K BITS)

The 16K ROM is a 2048 x 8 bit configuration. An address on lines A0-A10 uniquely selects one byte of ROM. Additionally, address line A11 and the chip selects are required to select the ROM function on a given chip. In a system with multiple R6531's, the CS1, CS2, and CS3 mask options allow up to seven devices with 14K bytes of ROM without the need for external decoding.

RAM – 128 BYTES (1024 BITS)

The 128 x 8 static RAM of a given R6531 is addressed by lines A0-A6. Additionally, address lines A7-A11 and chip selects CS1, CS2, and CS3 provide selection of the RAM section of the device as well as the device itself when additional RAM devices or R6531's are in the system.

R6531 PROTOTYPING CIRCUIT

The prototyping circuits for the R6531 (R6531-099, 1 MHz and R6531-099A, 2 MHz) are packaged in the 52-pin quad in-line package, with VRR option. PD2 is used as a chip select (CS3), and PB4 and PB5 are available as I/O lines.

Access codes for the prototyping circuit are shown in the table below.

R6531-099 Function	Chip Selects			Address Inputs (AO-A11)											
	CS3	CS2	CS1	11	10	9	8	7	6	5	4	3	2	1	0
ROM	H	N	N	H	2K ROM Decode										
RAM	L	N	N	L	L	L	N	L	128 RAM Decode						
I/O	L	N	N	L	H	H	H	L	L	L	L	I/O Decode			

The 128 words of RAM have been mapped into the first half of both Page 0 and Page 1, to accomodate zero page addressing and stack operations. The full I/O capabilities described for the R6531 are available in the prototyping circuit, except that I/O lines PD2 and PD3 are dedicated to the VRR and CS3 mask options.

INPUT/OUTPUT

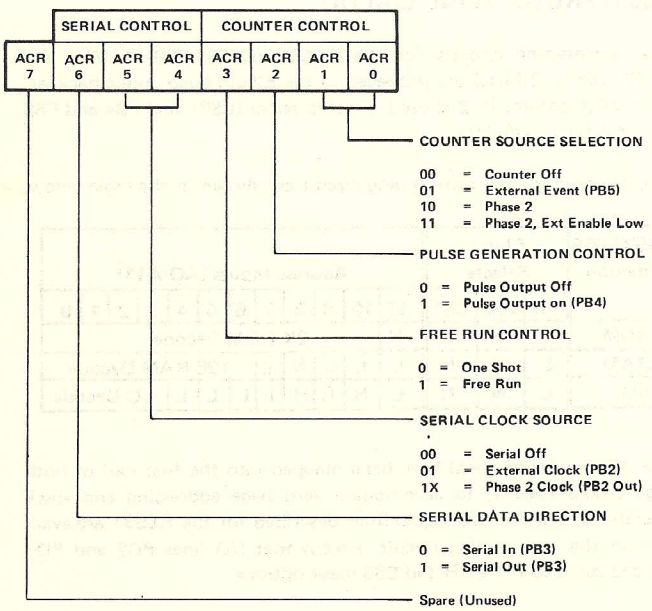
The input/output section is comprised of the data ports, direction registers, counter and associated latches, control registers, and interrupt registers. These I/O functions are all accessible by the R6502 CPU's instruction set using address bits A0-A3 for the specific function of the device. Address bits A4-A11 and CS1, CS2, and CS3 additionally may be decoded to select a given R6531 device in a multichip system. The addresses of the 15 internal peripheral registers are:

A3	A2	A1	A0	Register
0	0	0	0	Port A
0	0	0	1	Port B
0	0	1	0	Port C (write only)
0	0	1	1	Port D (read only)
0	1	0	0	Read Lower Counter/Write Lower Latch
0	1	0	1	Read Upper Counter/Write Upper Latch and Download
0	1	1	0	Write Lower Latch
0	1	1	1	Write Upper Latch
1	0	0	0	Serial Data Register
1	0	0	1	Interrupt Flag Register
1	0	1	0	Interrupt Enable Register
1	0	1	1	Auxiliary Control Register
1	1	0	0	Peripheral Control Register
1	1	0	1	*Data Direction Register — Port A
1	1	1	0	*Data Direction Register — Port B

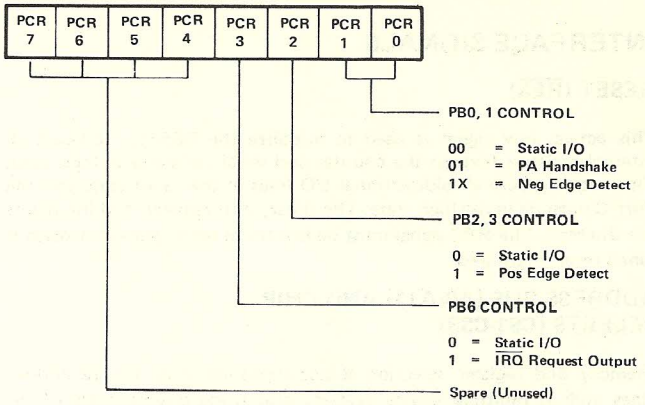
* Write Only

CONTROL REGISTERS

Two control registers, Peripheral Control and Auxiliary Control, are provided for software selection of various I/O functions. The Peripheral Control Register is primarily associated with Port B functions and the Auxiliary Control Register is associated with the counter and serial data functions which also affect Port B. The register bit assignments are:



Auxiliary Control Register (ACR)



Peripheral Control Register (PCR)

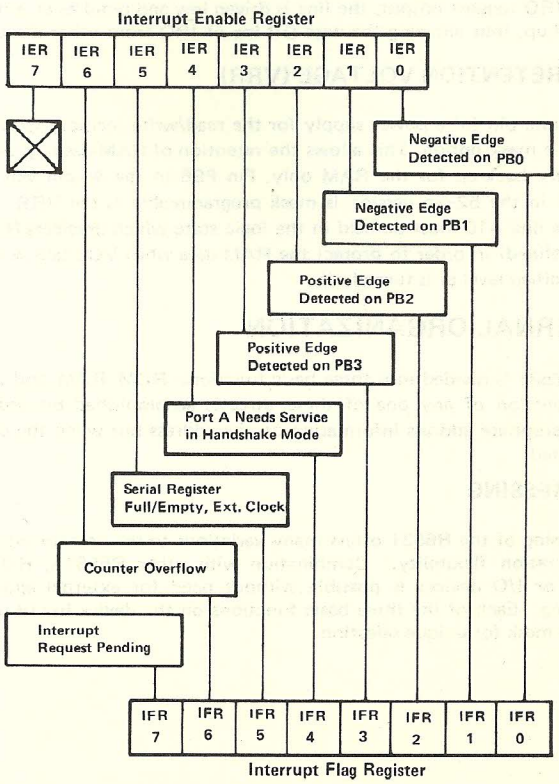
INTERRUPT ENABLE AND FLAG REGISTERS

Two registers are provided for interrupt control. Corresponding bits in the enable and flag registers are logically ANDed to set the Interrupt Request Pending flag. If the pending flag is set and PB6 is selected as an $\overline{IRQ}$ Request Output, then PB6 will be set low to request the R6502 CPU to service $\overline{IRQ}$.

The interrupt enable bits are set or reset by writing into the Interrupt Enable Register. The interrupt flag bits IFR0-IFR6 can be cleared directly by writing a byte to the flag register which has 1's in those bit positions to be cleared.

IFR4 and IFR5 may also be cleared by reading or writing the Port A or Serial Data Registers respectively. IFR6 may also be cleared by reading the lower counter with I/O address hex 4 or writing the upper latch with I/O addresses hex 5 or 7.

These registers and their bit assignments are:



Interrupt Flag Register

PERIPHERAL DATA PORTS

Each line of the 8-bit data Port A may be individually selected as an input or output. Associated with the port is Data Direction Register — Port A (DDRA). Each line of the 7-bit date Port B may be individually selected as an input or an output. This port also has a Data Direction Register (DDRB). The two data direction registers (A and B) control the direction of the data into and out of the peripheral pins. A "1" written into the Data Direction Register sets up the corresponding peripheral pin as an output. Therefore, anything written into the data register will appear on that corresponding peripheral pin. A "0" written into the DDR inhibits the output buffer from transmitting data from the data register. For example, a "1" loaded into DDRA, position 3, sets up peripheral pin PA3 as an output. If a "0" had been loaded, PA3 would be configured as an input and would be in a float state.

Note that when lines in the PB port are used alternately as control lines for other on-chip functions, Direction Register B must also be loaded to set up the proper direction — the Control Registers have no effect on data direction.

The 8-bit data Port C is an output only port. The 4-bit data Port D is an input only port.

For those lines being used as outputs, the data registers are used to latch data from the Data Bus during a Write operation so the peripheral device can read the data supplied by the microprocessor.

For the lines being used as inputs, the microprocessor is reading the peripheral data pins. For the peripheral data pins which are programmed as outputs the microprocessor will read the corresponding data bits of the Output data.

EDGE DETECT LOGIC

Operating in parallel with the I/O operation of PB0-PB3 is edge detect logic that is enabled by Peripheral Control Register bits 1 and 2. PCR1 enables logic that upon detection of a negative edge on PB0 or PB1 will set a corresponding flag in the Interrupt Flag Register. PCR2 enables logic that upon detection of a positive edge on PB2 or PB3 will set corresponding flags in the Interrupt Flag Register. If corresponding bits are set in the Interrupt Enable Register, then the Interrupt Request Pending flag will be set.

MULTI-MODE COUNTER/LATCH

The R6531 contains a 16-bit counter with an associated 16-bit latch whose modes are software selectable by setting appropriate bits in the Auxiliary Control Register. The latch holds the counter preset value and all 16 bits download to the counter simultaneously upon command (I/O address hex 5) of the software or automatically in free run modes upon overflow of the counter. The counter is a decrementing counter and causes the setting of a flag in the Interrupt Flag Register when it overflows. This interrupt flag, bit 6, is logically ANDed with a corresponding counter overflow interrupt enabled bit to set the Interrupt Request Pending flag. The Auxiliary Control Register is used to set four basic modes which specify the source of the count information, and to select two mode modifiers that apply equally to the three active modes.

Mode 0 — Counter Off

Mode 1 — Event Counter — counts external event inputs (negative transitions) at PB5

Mode 2 — Interval Timer — counts Ø2 system clock pulses.

Mode 3 — External Trigger — counts Ø2 system clock pulses starting with a negative transition on PB5.

Mode Modifier A — Pulse Generation Control — causes the output level on PB4 to switch low each time the counter is loaded using I/O address hex. 5. At counter overflow, PB4 switches high. If in the free run mode, PB4 continues to toggle at each subsequent counter overflow; otherwise there are no further transitions until the counter is reactivated by the software.

Mode Modifier B — Free Run Control — causes the full 16-bit latch to be downloaded to the counter, continues to count, and sets the counter overflow flag bit every time the counter overflows. Otherwise the counter is a one shot mode in which the counter overflow flag is set one time only until the counter is reactivated by the software.

SERIAL DATA CHANNEL

The R6531 has an 8-bit serial channel. PB2 and PB3 are software selectable as the serial clock (SCLK) and serial data (SDIO) lines respectively.

The software sets Auxiliary Control Register bits 4 and 5 to enable the serial channel and to specify the source of the shift clock. Selection of the internal clock will shift data at one half the system Ø2 clock rate. If the external clock is used, data may be shifted at any rate up to one half the system Ø2 clock rate. In the external clock mode, the counter may be operated in the free run pulse generator mode using the CNTO line externally connected to the SCLK line to provide the desired shift rate.

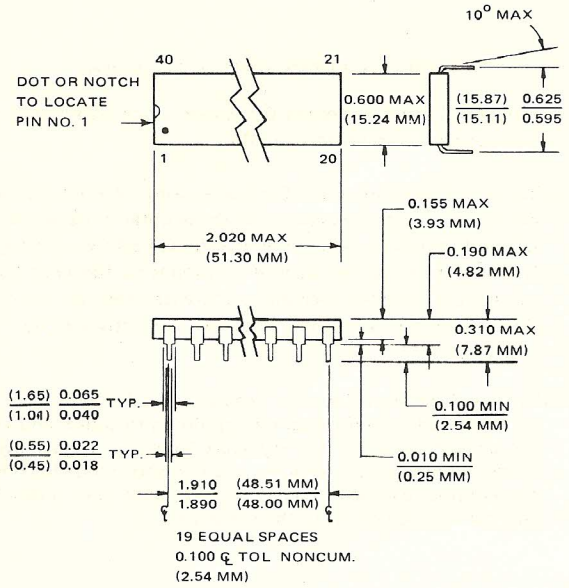
Auxiliary Control Register bit 6 sets the serial data direction. Data are shifted in or out with the most significant bit first under control of the shift clock.

In the external clock mode, the completion of eight shifts of the serial register will set bit 5 of the interrupt flag register. If the corresponding bit of the Interrupt Enable Register is also set an Interrupt Request Pending flag will be set.

HANDSHAKE OPERATIONS

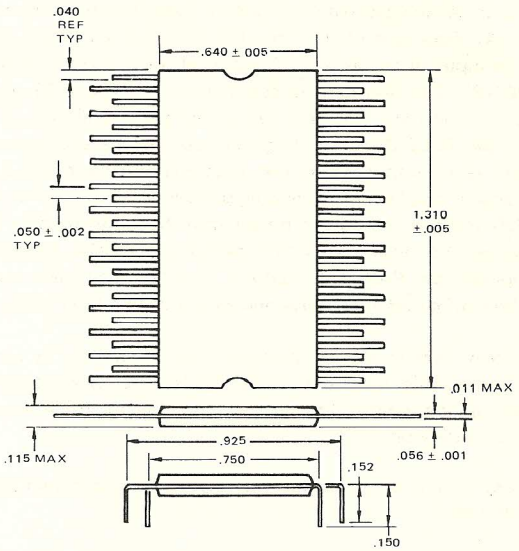
PB0 and PB1 may be used as handshake control lines for date transmissions over Port PA; see PCR definition. PB0 is a control input, PB1 is a control output. PB1 switches low on a read or write to Port PA, and switches high in response to a negative transition on PB0.

IFR4 in the Flag Register is set by a negative transition on PB0, and cleared by a Read or Write to Port PA; see Handshake Timing Diagram for timing details.

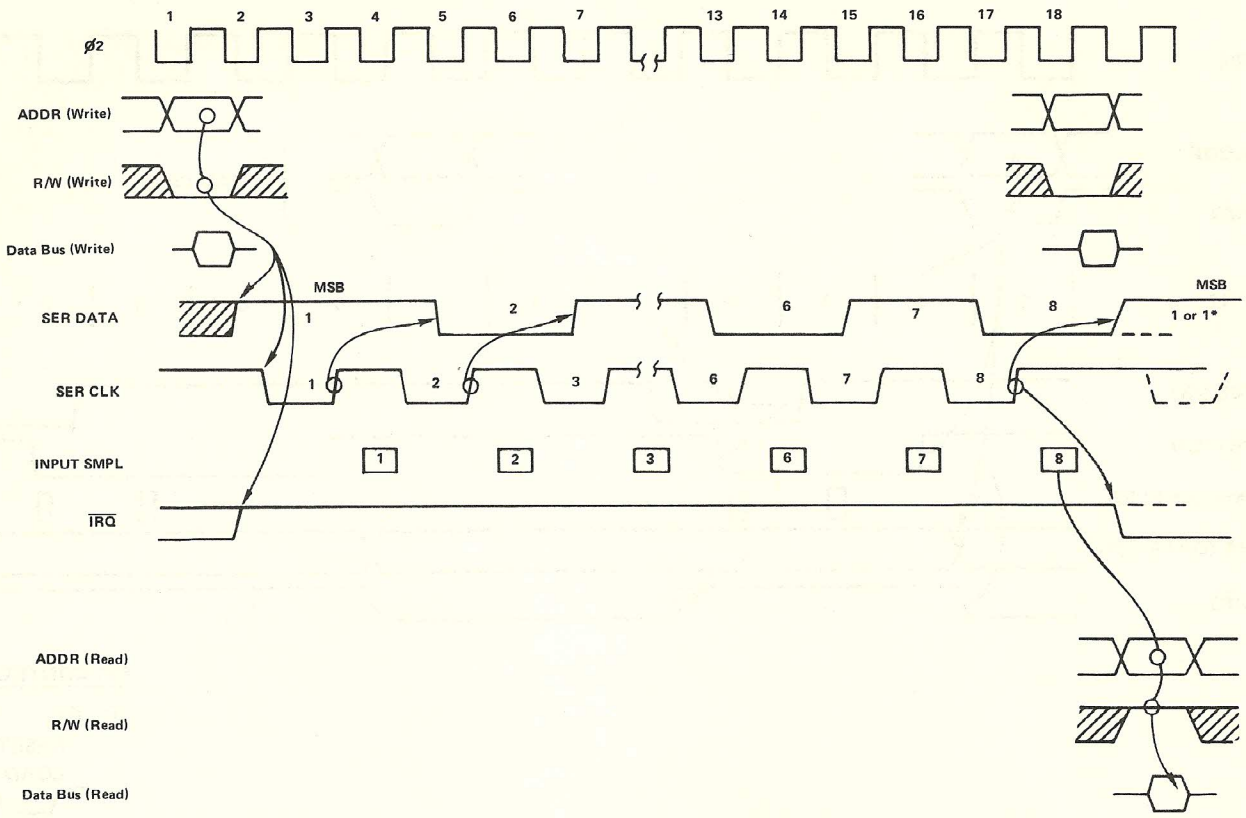


NOTE: Pin No. 1 is in lower left corner when symbolization is in normal orientation

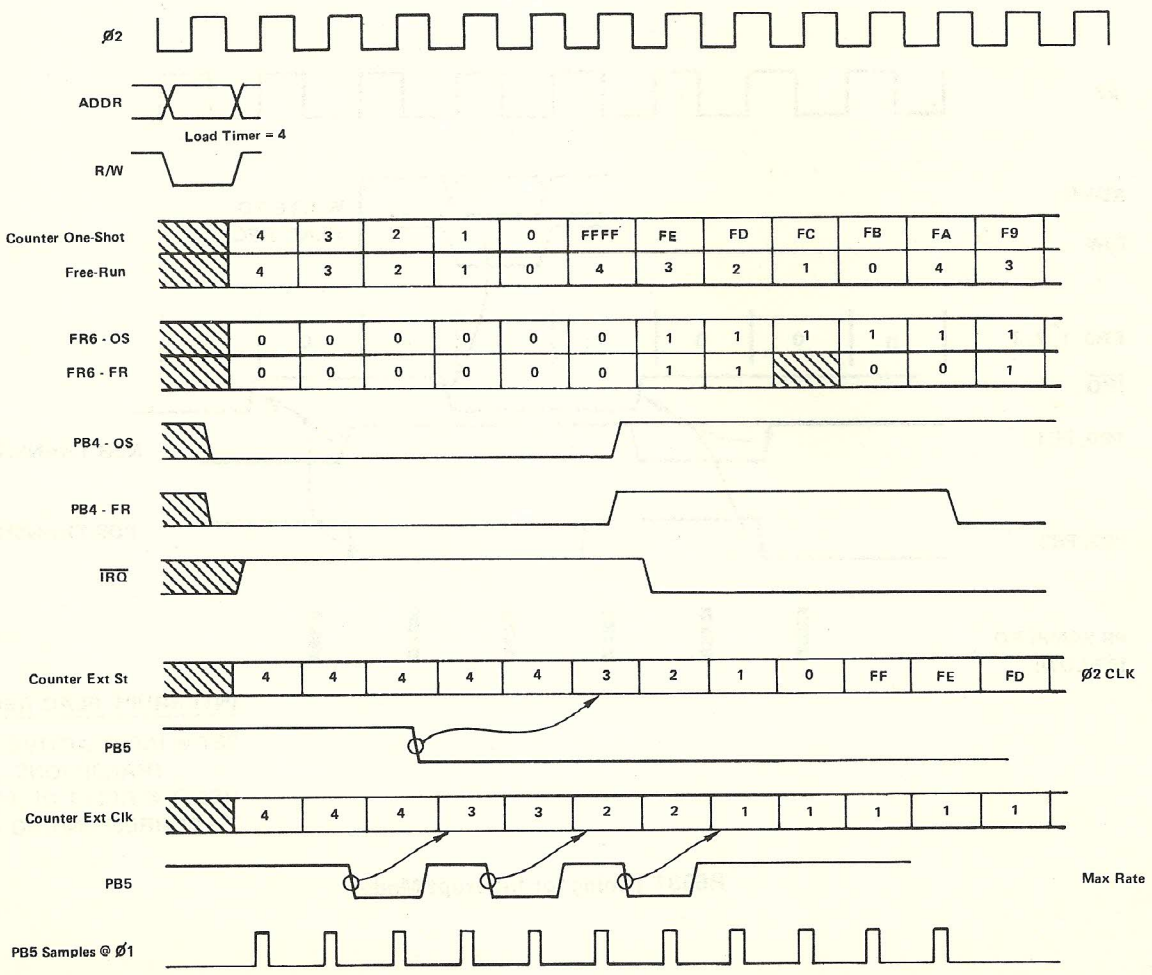
40-Pin Packaging Diagram



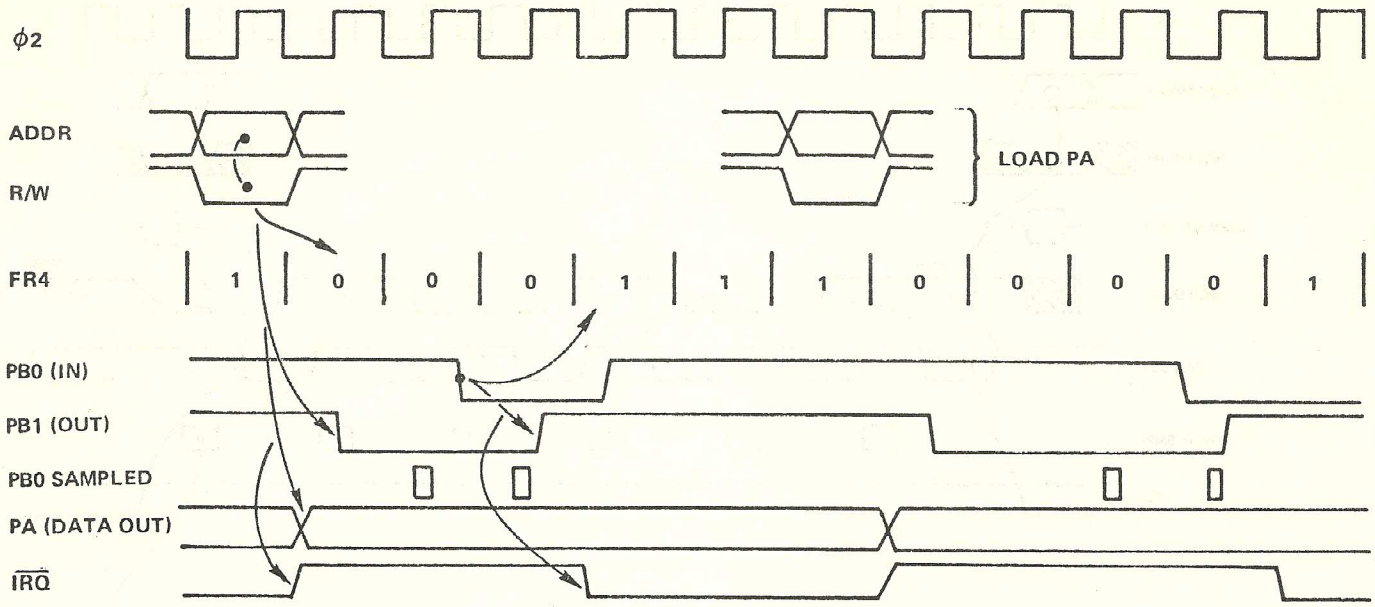
52-Pin Packaging Diagram



R6531 Serial Timing



R6531 Counter/Timer Timing

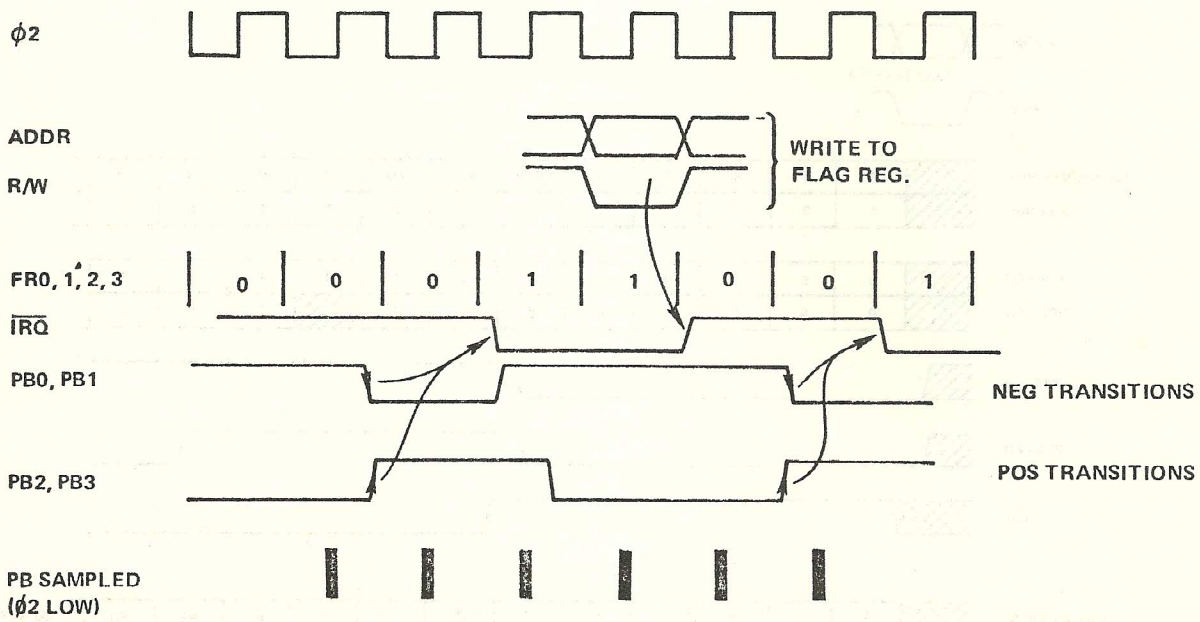


PB1 CONTROL

SET BY:
- RESET
- LOAD CRB
- ON PB0

RESET BY:
- LOAD PORT PA
- READ PORT PA

R6531 Timing for Handshake Mode



INTERRUPT FLAG REG. CONTROL

SET @ INPUT ACTIVE TRANSITIONS

RESET @ RESET OR WRITE "1" TO CORRESPONDING IFR BIT

R6531 Timing for Interrupt Mode

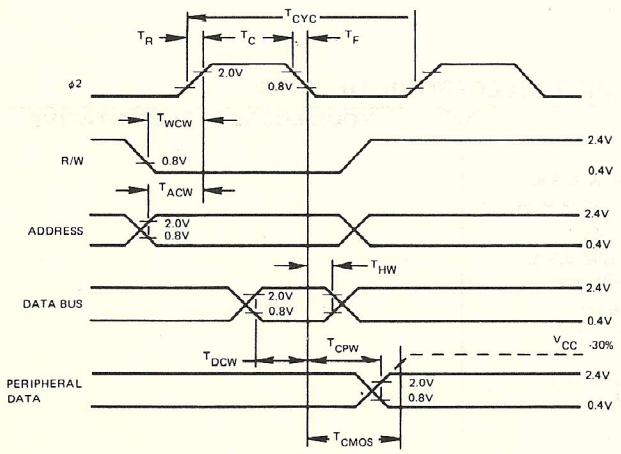
Write Timing Characteristics

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
Clock Period	T_{CYC}	1	10	0.5	10	μs
Rise & Fall Times	T_R, T_F		25		15	ns
Clock Pulse Width	T_C	470		235		ns
R/W valid before positive transition of clock	T_{WCW}	180		120		ns
Address valid before positive transition of clock	T_{ACW}	180		120		ns
Data Bus valid before negative transition of clock	T_{DCW}	270		135		ns
Data Bus Hold Time	T_{HW}	10		10		ns
Peripheral data valid after negative transition of clock	T_{CPW}		900		450	ns

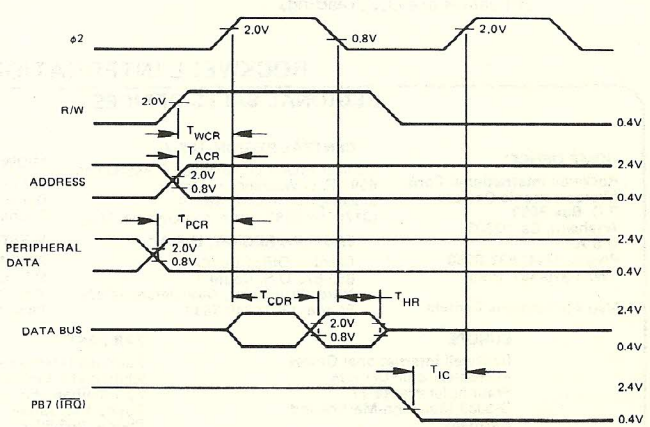
Read Timing Characteristics

Characteristic	Symbol	1 MHz		2 MHz		Unit
		Min	Max	Min	Max	
R/W valid before positive transition of clock	T_{WCR}	180		120		ns
Address valid before positive transition of clock	T_{ACR}	180		120		ns
Peripheral data valid before positive transition of clock	T_{PCR}	270		135		ns
Data Bus valid after positive transition of clock	T_{CDR}		350		180	ns
Data Bus Hold Time	T_{HR}	10		10		ns
IRQ valid after negative transition of clock	T_{IC}		900		450	ns

Loading = 100 pF + 1 TTL load for PA0-PA7, PB0-PB6, PCO-PC7
= 100 pF + 1 TTL load for D0-D7 (R6531A)
= 130 pF + 1 TTL load for D0-D7 (R6531)



Write Timing Characteristics



Read Timing Characteristics

SPECIFICATIONS

Maximum Ratings

Rating	Symbol	Voltage	Unit
Supply Voltage	VCC	-0.3 to + 7.0	V
Input/Output Voltage	V_{IN}	-0.3 to + 7.0	V
Operating Temperature Range	T_A	0 to 70	^oC
Storage Temperature Range	T_{STG}	-55 to + 150	^oC

All inputs contain protection circuitry to prevent damage due to high static changes. Care should be exercised to prevent unnecessary application of voltage outside the specification range.

Electrical Characteristics

(VCC = 5V ± 10% for R6531, VCC = 5V ± 5% for R6531A)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	VCC	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Input Leakage Current; $V_{IN} = V_{SS} + 5V$, $V_{CC} = +5V$ A0-A11, CS, R/W, RES, $\phi 2$, PD0-PD3	I_{IN}		2.5	μA
Leakage Current for High Impedance State, $V_{CC} = +5V$ (Three State); V_{IN} = 0.4V to 2.4V; D0-D7, PA0-PA7, PB0-PB6	I_{TSI}		±10.0	μA
Output High Voltage VCC = MIN, $I_{LOAD} \leq$ -200 μA (PA0-PA7, PB-PB6, D0-D7)	V_{OH}	VSS + 2.4		V
Output Low Voltage VCC = MIN, $I_{LOAD} \leq$ 2.1 mA	V_{OL}		VSS + 0.4	V
Output High Current (Sourcing); VOH ≥ 2.4V (PA0-PA7, PB0-PB6, PC0-PC7, PD0-PD3, D0-D7)	I_{OH}	-200		μA
Output Low Current (Sinking); $V_{OL} \leq$ 0.4V (PA0-PA7) (PB0-PB6) (PC0-PC7)	I_{OL}	2.1		mA
Clock Input Capacitance, V_{CC} = 5V	C_{Clk}		20	pF
Input Capacitance, V_{CC} = 5V	C_{IN}		10	pF
Output Capacitance, V_{CC} = 5V, chip deselected	C_{OUT}		10	pF
Power Dissipation	P_D		1.0	W

*When programmed as address pins

All values are D.C. readings

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YOUR LOCAL REPRESENTATIVE

PROGRAMMING INSTRUCTIONS

The Rockwell R6531 utilizes computer aided techniques to manufacture and test custom bit patterns. The custom bit pattern and address information is supplied on mini-floppy diskettes prepared on the SYSTEM 65, or paper tape, or standard 80-column computer cards in the format described below.

All addresses and related output patterns must be completely defined. Mask options should be noted on the ROM order form and in the title cards.

Title Cards

A set of seven Title Cards should accompany each data deck. These cards give our computer programs additional information necessary to accurately produce high density ROMS. These seven Title Cards must contain the following information:

	Column	Information
First Card	1-30	Customer Name
	31-50	Customer Part Number
	60-72	Rockwell Order Number (Example: R6531XX)
Second Card		Customer Contact Name, Customer Contact Phone Number
Third Card (2)		XX Pin Version with (without) VRR option. Example: 52 pin version without VRR option.
Fourth Card (2)		Pin 3 = CS1 or PB5 Pin 2 = CS2 or PB4 Pin 11 = CS3 or PD2 (52-pin version without VRR option only) Pin 10 = CS3 or PD2 (52-pin version with VRR option only) Example: Pin 3 = CS1, Pin 2 = PB4, Pin 11 = CS3
Fifth Card (2)	(1)	ROM SEL, CS1 = X, CS2 = X, CS3 = X, A11 = X Example: ROM SEL, CS1 = L, CS2 = N, CS3 = L, A11 = L
Sixth Card (2)	(1)	RAM SEL, CS1 = X, CS2 = X, CS3 = X, A11 = X, A10 = X, A9 = X, A8 = X, A7 = X Example: RAM SEL, CS1 = L, CS2 = N, CS3 = H, A11 = H, A10 = L, A9 = L, A8 = L, A7 = L
Seventh Card (2)	(1)	I/O SEL, CS1 = X, CS2 = X, CS3 = X, A11 = X, A10 = X, A9 = X, A8 = X, A7 = X, A6 = X, A5 = X, A4 = X Example: I/O SEL, CS1 = H, CS2 = N, CS3 = H, A11 = L, A10 = L, A9 = L, A8 = L, A7 = L, A6 = L, A5 = L, A4 = L

(1) X = H or L or N
H = +2.4 Volts L = +0.4 Volts N = No Effect

(2) Free Format — Delimiters are commas or blanks

Data Card Format

The required data card format is generated by the Cross Assembler. All addresses are coded in hexadecimal form (0 through FFFF). All output words are coded both in binary and octal forms. Output 8 (DB7) is the MSB, and Output 1 (DB0) is the LSB.

The format for all cards in a file, except the last card, is as follows:

$$;3S_2S_1S_0\not{b}N_1N_0\not{b}A_3A_2A_1A_0D_1D_0D_1D_0\not{b}X_3X_2X_1X_0$$

(1 = D_1D_0, 2 = D_1D_0)

The format for the last card in a file is as follows:

;40000

EXAMPLE:

```
;30001 10 0000 6964656475647964006D4C047D4C0479 054F
;30002 10 0010 4C0461647164296425643564396400 2D 0463
;30003 10 0037 24642C4C04000000000000000000000000 0104
;40000
```

Paper Tape Format

Rockwell can accept ROM coding in paper tape prepared using SYSTEM 65, Cross Assembler or AIM 65 output. Mask options should be noted on the ROM order form. The format for paper tape is as follows:

$$;N_1N_0A_3A_2A_1A_0D_1D_0D_1D_0X_3X_2X_1X_0CRLF$$

(1 = D_1D_0, 2 = D_1D_0)

The format for the last record in a file is as follows:

$$;00C_3C_2C_1C_0X_3X_2X_1X_0$$

NOTE 1

1. 00 = zero bytes of data in this record. This identifies this as the final record in a file.

2. $C_3C_2C_1C_0$ = the total number of records (in hexadecimal) in this file, including the last record.

3. The valid record is identified by the starting delimitor (;) and terminated by the check sum ($X_3X_2X_1X_0$). All other characters such as the CR and LF are not processed. The next semi-colon initiates the next record.

EXAMPLE:

```
;18F000CA86004C00F0FDF9212D21FF292DBF2161F5F7FF657D677D00D40
;18F018E564672DFD7575E50000CF4112F800925198D200539192F20C98
;18F03008DB02880810DE12D894189AC2830E9800FBB6232F087F650AA5
;0000030003
```

Unless otherwise stated, the field definitions are defined as follows:

1. All Characters (N,A,D,X) are the ASCII characters 0 through F, each representing a hexadecimal (hex) digit.

2. ; is a record mark indicating the start of a record.

3. N_1N_0 = the number of bytes of data in this record (in hex). Each pair of hex characters (D_1D_0) represents a single byte in the record.

4. $A_3A_2A_1A_0$ = the hex starting address for the record. A_3 represents address bits 15 through 12, etc. The 8-bit byte represented by $(D_1D_0)_1$ stored in address $A_3A_2A_1A_0$; $(D_1D_0)_2$ stored in $(A_3A_2A_1A_0) + 1$, etc.

5. (D_1D_0) = two hex digits representing an 8-bit byte of data. (D_1 = high-order 4 binary bits and D_0 = low-order 4 bits). A maximum of 18 (hex) or 24 (decimal) bytes of data per record is permitted.

6. $X_3X_2X_1X_0$ = record check sum. This is the hex sum of all characters in the record, excluding the record mark and the check sum characters. To generate the check sum, each byte of data (represented by two ASCII characters), is treated as 8 binary bits. The binary sum of these 8-bit bytes is truncated to 16 binary bits (4 hex digits) and is then represented in the record as four ASCII characters ($X_3X_2X_1X_0$).

7. $S_2S_1S_0$ = the hex sequence number for the card record.

8. CR = ASCII character for Carriage return.

9. LF = ASCII character for line feed.

10. ␣ = Space character

Mini-Floppy Diskette Format

Rockwell can accept ROM coding on mini-floppy diskettes prepared using the SYSTEM 65 Assembler output. The format is similar to the Paper Tape format shown in the preceding paragraph. Title card information should be recorded using the file name "TITLE." Data information should be recorded using the file name "DATA." Mask options should be noted on the ROM Order form.

ROM ORDER FORM–R6531

Please fill in the following information, and send form and bit pattern data to:

Rockwell International, Microelectronic Devices
3310 Miraloma Ave. P.O. Box 3669; Anaheim, CA 92803
Attn: Marketing Administration; D815; RC48

1. Your Company _____

2. Purchase Order No. for this ROM _____

3. Device Number: R6531 _____ * (*Complete number will be assigned by Rockwell)

4. ROM is for: _____ (System Identification)

5. ROM Start and Stop Address in your system.

   ROM Data Start Address in System is: ____ ____ ____ ____ (four hexadecimal digits)

   ROM Data Stop Address in System is: ____ ____ ____ ____ (four hexadecimal digits)

6. ROM Start and Stop Address in Submitted Media (Tapes, Cards, Diskettes).

   ROM Data Start Address is: ____ ____ ____ ____ (four hexadecimal digits)

   ROM Data Stop Address is: ____ ____ ____ ____ (four hexadecimal digits)

7. Fill in the following chart for each Select Term with either "H" for +2.4 volts, "L" for 0.4 volts, or "N" for No Effect.

	CS1	CS2	CS3	A11	A10	A9	A8	A7	A6	A5	A4
ROM Select											
RAM Select											
I/O Select											

8. Specify Configuration (check one)

   ☐ 40-pin version without VRR option ☐ 40-pin version with VRR option

   ☐ 52-pin version without VRR option ☐ 52-pin version with VRR option

9. Specify Chip Selects (check one on each line)

   ☐ CS1 ☐ PB5
   ☐ CS2 ☐ PB4
   ☐ CS3 ☐ PD2 **Note:** This line applies only to 52-pin versions

10. Fill code to be used for unused ROM locations is: ____ ____ (two hexadecimal digits)

Deliver Completed ROM to: _____
(Name) (Phone: Area/Number)

_____ _____
(Dept./Mail Stop) (Company)

_____ _____
(Street Address/P.O. Box) (City, State, Zip Code)

ROM Ordered By: _____ Order Approved By: _____
(Name) (Date) (Name) (Date)