



COMMODORE SEMICONDUCTOR GROUP

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HMOS

23128 STATIC READ ONLY MEMORY (16384x8)

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DESCRIPTION

The 23128 high performance read only memory is organized 16384 words by 8 bits with a wide range of access times. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels.

The 23128 operates totally asynchronously. No clock input is required. The programmable chip select inputs allow selection of 8 ROMS.

- 16384 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time — 450ns, 300ns, 250ns
- Completely TTL Compatible
- Totally Static Operation
- Three-State Outputs for Wire-OR Expansion
- Three Programmable Chip Selects
- 2732/2764 EPROMS Accepted as Program Data Inputs
- 400mV Noise Immunity on Inputs

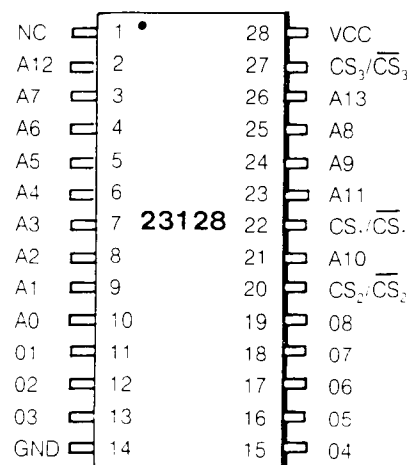
ORDERING INFORMATION MXS 23128

FREQUENCY RANGE
 NO SUFFIX = 450ns
 A = 300ns
 B = 250ns
 C = 200ns* (1)

PACKAGE DESIGNATOR
 D = CERAMIC
 P = PLASTIC

(1) = 200ns available in 1987

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

| | |
|------------------------------------|-----------------|
| Ambient Temperature under Bias | -65°C to +70°C |
| Storage Temperature | -65°C to +150°C |
| Supply Voltage to Ground Potential | -0.5V to +7.0V |
| Applied Output Voltage | -0.5V to +7.0V |
| Applied Input Voltage | -0.5V to +7.0V |
| Power Dissipation | 1.0W |

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D. C. CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$, unless otherwise specified)

| Symbol | Parameter | Min. | Max. | Units | Test Conditions |
|-----------|------------------------|------|------------|---------------|--|
| I_{CC1} | Power Supply Current | | 100 | mA | $V_{IN} = V_{CC}$, $V_O = \text{Open}$, $T_A = 0^\circ\text{C}$ |
| I_{CC2} | Power Supply Current | | 95 | mA | $V_{IN} = V_{CC}$, $V_O = \text{Open}$, $T_A = 25^\circ\text{C}$ |
| I_O | Output Leakage Current | | 10 | μA | Chip Deselected, $V_O = 0$ to V_{CC} |
| I_I | Input Load Current | | 10 | μA | $V_{CC} = \text{Max.}$, $V_{IN} = 0$ to V_{CC} |
| V_{OL} | Output Low Voltage | | 0.4 | Volts | $V_{CC} = \text{Min.}$, $I_{OL} = 2.1\text{mA}$ |
| V_{OH} | Output High Voltage | 2.4 | | Volts | $V_{CC} = \text{Min.}$, $I_{OH} = -400\mu\text{A}$ |
| V_{IL} | Input Low Voltage | -0.5 | 0.8 | Volts | See Note 1 |
| V_{IH} | Input High Voltage | 2.0 | $V_{CC}+1$ | Volts | |

A. C. CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$, unless otherwise specified)

| Symbol | Parameter | 23128 | | 23128A | | 23128B | | Units | Test Conditions |
|-----------|--|-------|------|--------|------|--------|------|-------|-----------------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| t_{ACC} | Address Access Time | | 450 | | 300 | | 250 | ns | See Note 2 |
| t_{CO} | Chip Select Delay | | 200 | | 100 | | 100 | ns | |
| t_{DF} | Chip Deselect Delay | | 175 | | 75 | | 75 | ns | |
| t_{OH} | Previous Data Valid After Address Change Delay | 40 | | 40 | | 40 | | ns | |

CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$, See Note 3)

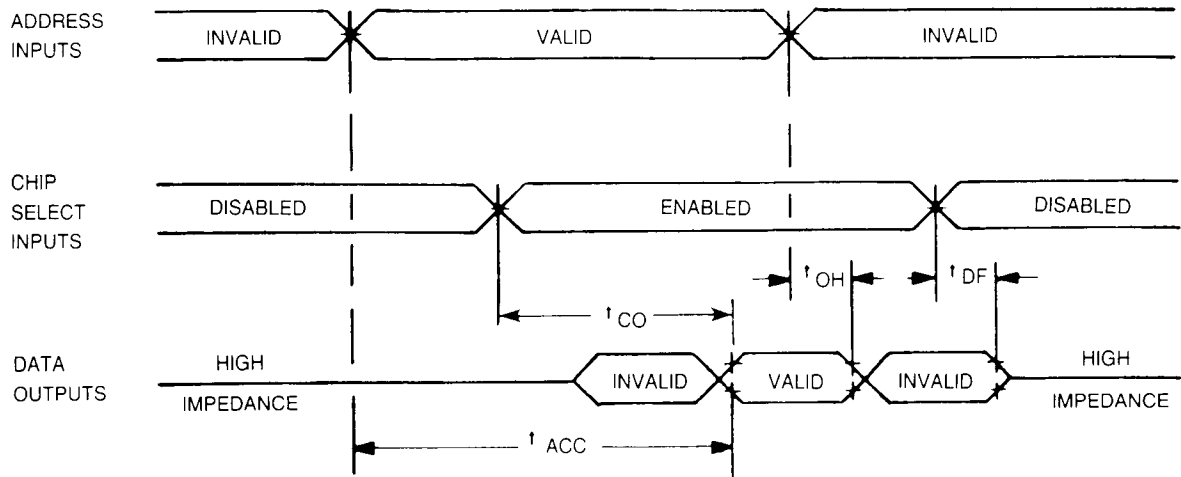
| Symbol | Parameter | Min. | Max. | Units | Test Conditions |
|-----------|--------------------|------|------|-------|---------------------------|
| C_{IN} | Input Capacitance | | 8 | pF | All Pins except Pin under |
| C_{OUT} | Output Capacitance | | 10 | pF | Test Tied to AC Ground |

Note 1: Input levels that swing more negative than -0.5V will be clamped and may cause damage to the device.

Note 2: Loading 1 TTL + 100 pF, input transition time: 20 ns
Timing measurement levels: input 1.5V, output 0.8V and 2.0V.

Note 3: This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAMS



BLOCK DIAGRAM

