2364 - 901226 01 901486-01
27-03
325302 - 29-05 901486-02

COMMODORE SEMICONDUCTOR GROUP
a division of Commodore Business Machines, Inc.
950 Rittenhouse Rd., Norristown, PA 19403 • Tel.: 215/666-7950 • TWX: 510/660-4168

ORIGINAL

HMOS

2364 STATIC READ ONLY MEMORY (8192x8)

DESCRIPTION

The 2364 high performance read only memory is organized 8192 words by 8 bits with a wide range of access times. This ROM is designed to be compatible with all microprocessor and similar applications where high performance, large bit storage and simple interfacing are important design considerations. This device offers TTL input and output levels.

The 2364 operates totally asynchronously. No clock input is required. The two programmable chip select inputs allow four 64K ROMS to be OR-tied without external decoding.

Designed to replace two 2732 32K EPROMS, the 2364 can eliminate the need to redesign printed circuit boards for volume mask programmed ROMS after prototyping with EPROMS.

- 8192 x 8 Bit Organization
- Single +5 Volt Supply
- Access Time — 450 ns, 300 ns, 250 ns
- Completely TTL Compatible
- Totally Static Operation
- Three-State Outputs for Wire-OR Expansion
- One Programmable Chip Select
- Pin Compatible with 2716 & 2732 EPROM
- Replacement for Two 2732s
- 2716/2732 EPROMS Accepted as Program Data Inputs
- 400mV Noise Immunity on Inputs

ORDERING INFORMATION

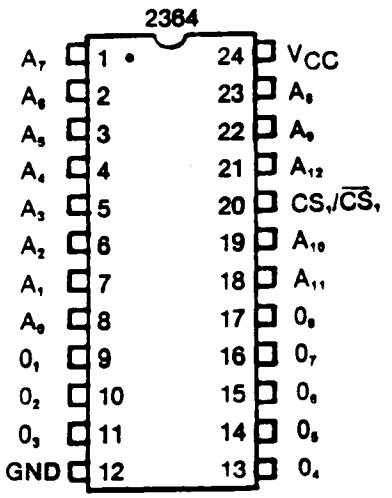
MXS 2364

FREQUENCY RANGE
NO SUFFIX = 450 ns
A = 300 ns
B = 250 ns
C = 200 ns (1)

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

(1) = 200 ns available in 1987

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	°C to + 70 °C
Storage Temperature	− 65 °C to + 150 °C
Supply Voltage to Ground Potential	− 0.5V to + 7.0V
Applied Output Voltage	− 0.5V to + 7.0V
Applied Input Voltage	− 0.5V to + 7.0V
Power Dissipation	1.0W

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS

T_A = 0 °C to + 70 °C, V_{CC} = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
I_{CC1}	Power Supply Current		100	mA	V_{IN} = V_{CC}, VO = Open, T_A = 0 °C
I_{CC2}	Power Supply Current		95	mA	V_{IN} = V_{CC}, V_O = Open, T_A = 25 °C
I_O	Output Leakage Current		10	uA	Chip Deselected, V_O = O to V_{CC}
I_I	Input Load Current		10	uA	V_{CC} = Max. V_{IN} = O to V_{CC}
V_{OL}	Output Low Voltage		0.4	Volts	V_{CC} = Min. I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4		Volts	V_{CC} = Min. I_{OH} = − 400uA
V_{IL}	Input Low Voltage	− 0.5	0.8	Volts	See note 1
V_{IH}	Input High Voltage	2.0	V_{CC} + 1	Volts	

A.C. CHARACTERISTICS

T_A = 0 °C to + 70 °C, V_{CC} = 5.0V ± 5% (unless otherwise specified)

Symbol	Parameter	2364		2364A		2364B		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
T_{ACC}	Address Access Time	—	450	—	300	—	250	ns
T_{CO}	Chip Select Access Time	—	200	—	100	—	100	ns
T_{DF}	Chip Deselect Delay		175		75		75	ns
T_{OH}	Previous Data Valid After Address Change	40	—	40	—	40	—	ns

Test Conditions See Note 2

CAPACITANCE

T_A = 25 °C, f = 1.0MHz, See Note 3

Symbol	Parameter	Min.	Max.	Units	Test Conditions
C_{IN}	Input Capacitance		8	pF	All Pins except Pin under
C_{OUT}	Output Capacitance		10	pF	Test Tied to AC Ground

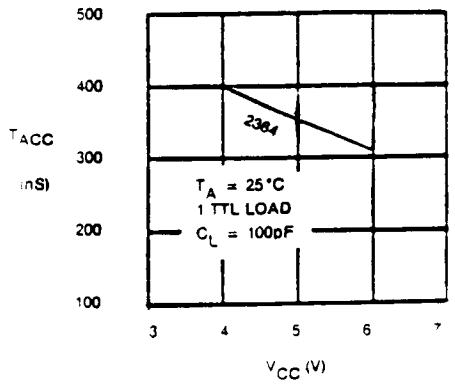
Note 1: Input levels that swing more negative than − 0.5V will be clamped and may cause damage to the device.

Note 2: Loading 1 TTL + 100 pF, input transition time: 20 ns.
Timing measurement levels: input 1.5V, output 0.8V and 2.0V. C_L = 100 pF.

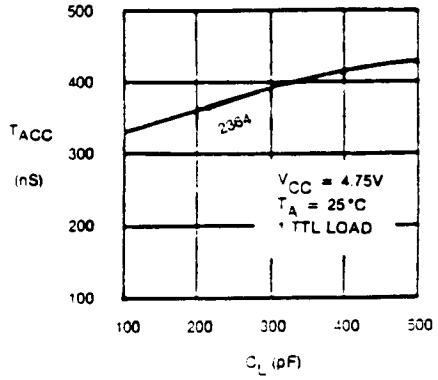
Note 3: This parameter is periodically sampled and is not 100% tested.

TYPICAL CHARACTERISTICS

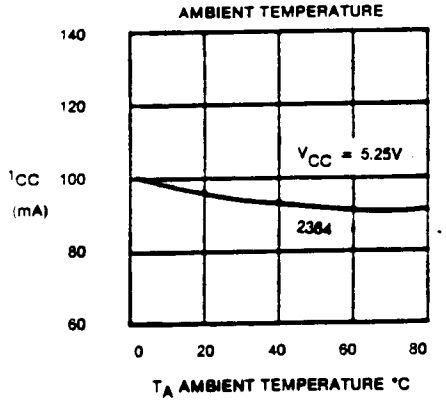
ACCESS TIME VS.
SUPPLY VOLTAGE



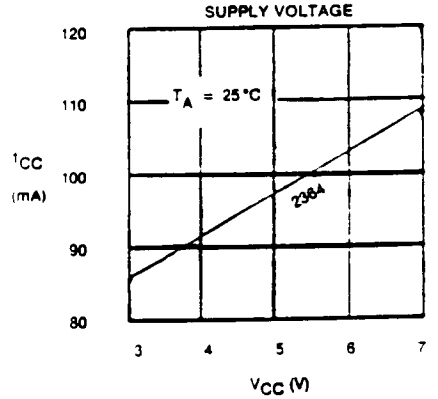
ACCESS TIME VS.
CAPACITIVE LOAD



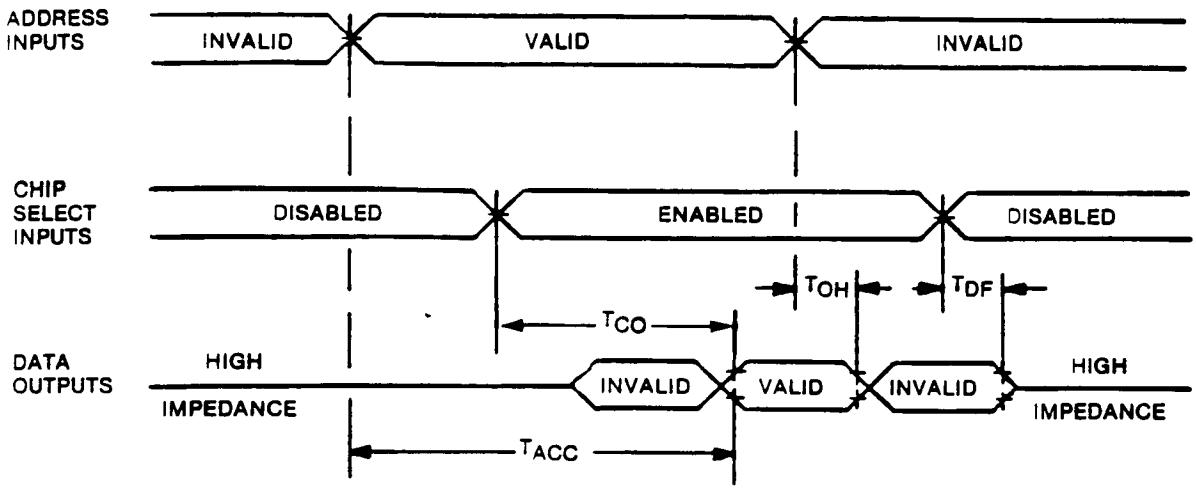
SUPPLY CURRENT VS.
AMBIENT TEMPERATURE



SUPPLY CURRENT VS.
SUPPLY VOLTAGE



TIMING DIAGRAM



BLOCK DIAGRAM