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6560/6561 VIDEO INTERFACE CHIP

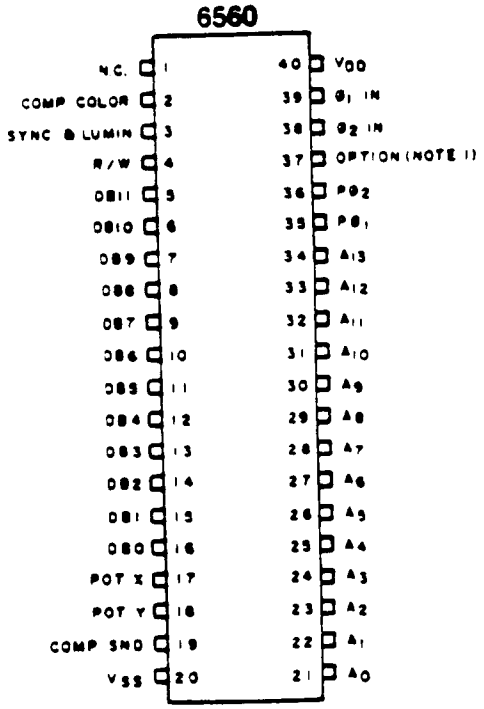
GENERAL DESCRIPTION

The 6560 Video Interface Chip (VIC) is designed for color video graphics applications such as low cost CRT terminals, biomedical monitors, control system displays and arcade or home video games. It provides all of the circuitry necessary for generating color programmable character graphics with high screen resolution. VIC also incorporates sound effects and A/D converters for use in a video game environment.

FEATURES

- Fully expandable system with a 16K byte address space
- System uses industry standard 8 bit wide ROMS and 4 bit wide RAMS
- Mask programmable sync. generation, NTSC-6560, PAL-6561
- On-chip color generation (16 colors)
- Up to 600 independently programmable and movable background locations on a standard TV
- Screen centering capability
- Screen grid size up to 192 Horizontal by 200 Vertical dots
- Two selectable graphic character sizes
- On-chip sound system including:
  a) Three independent, programmable tone generators
  b) White noise generator
  c) Amplitude modulator
- Two on-chip 8 bit A/D converters
- On-chip DMA and address generation
- No CPU wait states or screen hash during screen refresh
- Interlaced/Non-Interlaced switch
- 16 addressable control registers
- Light gun/pen for target games
- 2 modes of color operation

PIN CONFIGURATION
6560

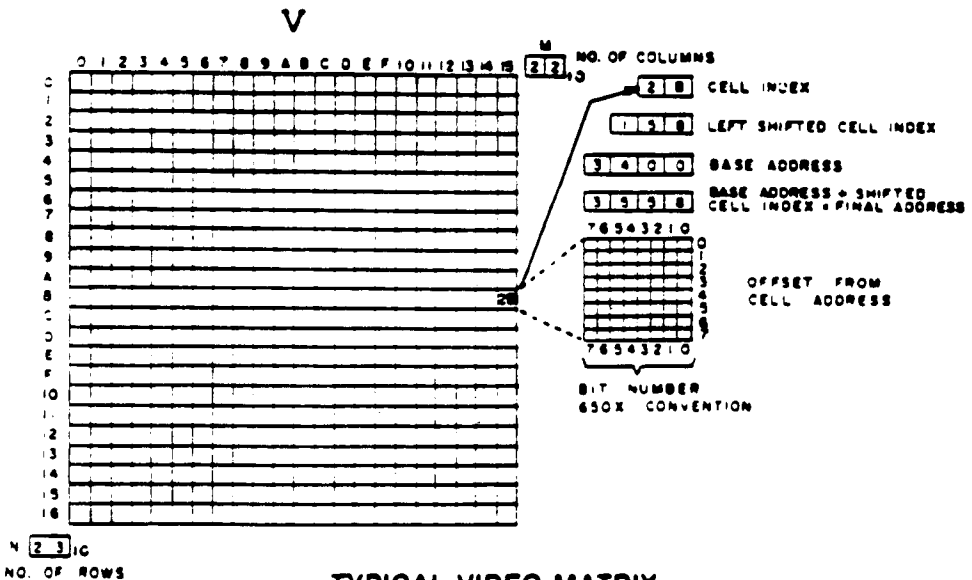


THEORY OF OPERATION

In order to produce programmable color characters, VIC accesses external memory which can be divided into three areas: character pointers, display characters and color pointers. The character pointer area is a block of bytes in RAM (typically 506 bytes called the Video Matrix) in which each byte points to a particular character to be displayed. The character area consists of a set of 8 or 16 byte blocks (usually called cells) which contain the actual dot patterns to be displayed. These character cells can be located in either RAM or ROM depending on how the objects are to be displayed or moved on the screen. The color pointer area is a block of nybbles in RAM (typically 506-4 bit nybbles called the Color Matrix). The 4 bit color pointers are used to define the color of any character which is to be displayed and to select one of the two color modes.

It is the task of an external microprocessor to organize the Video Matrix, Color Matrix and Character Cells into the proper format to display the data desired on-screen.

To understand the operation of VIC more completely, consider the diagram shown in Figure 1. This is a typical Video Matrix, in which 22 characters horizontally by 23 characters vertically are to be displayed, yielding a total of 506 character display locations, with a screen resolution of 176 horizontal by 184 vertical dots. Each one of these character display locations has a corresponding character pointer, or index, which specifies (points at) a character to be displayed in that particular location. In the example shown, rectangle (B,15) has a character index of 2B. This means character number 2B is to be displayed in that rectangle. VIC will fetch the character index value 2B and perform an address computation to locate the desired character to be displayed. The computation is quite simple. If 8 x 8 character cells are selected, the index is left shifted 3 times (multiply by 8) and the starting address of the character cells, found in VIC Control Register CR_5, is added to the left shifted value. In this case, the character cell starting address is 3400 (in HEX) which is added to the left shifted value of the character index to yield the actual character location in memory of 3558 (in HEX). Note here that the actual character displayed is an eight dot by eight dot matrix which can be stored in either ROM or RAM. Also, the number of times that any particular character can be displayed is unlimited. By using the same character index (2B for example) elsewhere on the grid, the character data will be displayed again. Alternately, through the use of a simple software driver, VIC can be used as a bit-mapped display system provided enough RAM is available (approximately 4K bytes of cell RAM).



TYPICAL VIDEO MATRIX
(23 x 22)
FIGURE 1

1000 ORIGIN

		7	6	5	4	3	2	1	0	(bit number)
CR_0	1000	I	S_X^6	S_X^5	S_X^4	S_X^3	S_X^2	S_X^1	S_X^0	SCREEN ORIGIN X-COORDINATE
CR_1	1001	S_Y^7	S_Y^6	S_Y^5	S_Y^4	S_Y^3	S_Y^2	S_Y^1	S_Y^0	SCREEN ORIGIN Y-COORDINATE
CR_2	1002	B_V^9	M_6	M_5	M_4	M_3	M_2	M_1	M_0	NO. OF VIDEO MATRIX COLUMNS
CR_3	1003	R_0	N_5	N_4	N_3	N_2	N_1	N_0	D	NO. OF VIDEO MATRIX ROWS
CR_4	1004	R_8	R_7	R_6	R_5	R_4	R_3	R_2	R_1	RASTER VALUE
CR_5	1005	B_V^{13}	B_V^{12}	B_V^{11}	B_V^{10}	B_C^{13}	B_C^{12}	B_C^{11}	B_C^{10}	BASE ADDRESS CONTROL
CR_6	1006	L_H^7	L_H^6	L_H^5	L_H^4	L_H^3	L_H^2	L_H^1	L_H^0	LIGHT PEN HORIZONTAL
CR_7	1007	L_V^7	L_V^6	L_V^5	L_V^4	L_V^3	L_V^2	L_V^1	L_V^0	LIGHT PEN VERTICAL
CR_8	1008	P_X^7	P_X^6	P_X^5	P_X^4	P_X^3	P_X^2	P_X^1	P_X^0	POT X
CR_9	1009	P_Y^7	P_Y^6	P_Y^5	P_Y^4	P_Y^3	P_Y^2	P_Y^1	P_Y^0	POT Y
CR_A	100A	S_1	F_1^6	F_1^5	F_1^4	F_1^3	F_1^2	F_1^1	F_1^0	$F_{IN}^{(1)}$
CR_B	100B	S_2	F_2^6	F_2^5	F_2^4	F_2^3	F_2^2	F_2^1	F_2^0	$F_{IN}^{(2)}$
CR_C	100C	S_3	F_3^6	F_3^5	F_3^4	F_3^3	F_3^2	F_3^1	F_3^0	$F_{IN}^{(3)}$
CR_D	100D	S_4	F_4^6	F_4^5	F_4^4	F_4^3	F_4^2	F_4^1	F_4^0	$F_{IN}^{(4)}$
CR_E	100E	C_A^3	C_A^2	C_A^1	C_A^0	A_3	A_2	A_1	A_0	AMPLITUDE
CR_F	100F	C_B^3	C_B^2	C_B^1	C_B^0	R	C_E^2	C_E^1	C_E^0	COLOR CONTROL

NU = NOT USED

VIC CONTROL REGISTERS

REGISTER DESCRIPTION

There are sixteen eight-bit control registers within the 6560 which enable the microprocessor to control all the operating modes of VIC. The control registers and their functions are tabulated and explained below.

EXPLANATION OF CONTROL REGISTER FUNCTIONS

CR_0: Bits 0-6 determine how far from the left-hand side of the T.V. screen the first column of characters will appear. It is used to Horizontally center various sizes of video matrices on-screen. Bit 7 selects interlaced scan mode (I = 1).

CR_1: Determines how far from the top of the T.V. screen the first row of characters will appear. It is similarly used to vertically center various sizes of video matrices on-screen.

CR_2: Bits 0-6 set the number of columns in the Video Matrix. Bit 7 is part of the Video Matrix address found in CR_5.

CR_3: Bits 1-6 set the number of rows in the Video Matrix. Bit 0 is used to select either 8 x 8 character matrices (D = 0) or 16 x 8 character matrices (D = 1). Bit 7 is part of the RASTER value found in CR_4.

CR_4: Contains the number of the line currently being scanned by the T.V. raster beam.

CR_5: Bits 0-3 determine the starting address of the character cell space. (Note that these bits form bits A13 through A10 of the actual address.) Bits 4-7 (along with Bit 7 of CR_2) determine the starting address of the Video Matrix (these bits form bits A13 through A9 of the actual address).

CR_6: Contains the latched horizontal position of the light gun/pen.

CR_7: Contains the latched vertical position of the light gun/pen.

CR_8: Contains the digitized value of POTX.

CR_9: Contains the digitized value of POTY.

CR_A: Bits 0-6 set the frequency of the first audio oscillator. Bit 7 turns the oscillator on (= 1) or off (= 0).

CR_B: Same as CR_A for second audio oscillator.

CR_C: Same as CR_A for third audio oscillator.

CR_D: Same as CR_A, but sets frequency of noise source.

CR_E: Bits 0-3 set the volume of the composite audio signal (Note that at least one sound generator must be turned on for any sound to be produced). Bits 4-7 contain the Auxiliary color code used in conjunction with the "Multicolor" mode of operation.

CR_F: Bits 4-7 select 1 of 16 colors for the background common to all characters. (Essentially, they set the color of the background area within the Video Matrix.) Bits 0-2 select 1 of 8 colors for the exterior border area of the screen (all area outside the Video Matrix). Bit 3 determines whether the Video Matrix will be displayed as different colored characters on a common background color (R = 1) or inverted (R = 0), that is, all characters will be the same color (the background color in CR_F) while each character's background will now be a different color, determined by the code in the Color RAM. Note that the R bit has no effect when Multicolor mode is selected and that CR_F also functions differently in this mode. Refer to the section called "Operating Modes" for complete information.

COLOR OPERATING MODES

VIC incorporates two modes of color operation. HI-RES (high resolution) mode and Multicolor mode. Basically, the operating mode affects how the Character Cell information will be translated into dots on the TV screen. The operating mode is determined by the MSB of the color pointer associated with each character location in the Video Matrix. If the MSB of a character's color pointer is zero, then that character will be displayed in HI-RES mode. Alternately, if the MSB is one, the character will be displayed in Multicolor mode.

With HI-RES mode selected, there is a one-to-one correspondence between Character Cell bits and the dots displayed on-screen. That is, all one bits of a character will be displayed in one color, and all zero bits in another color. The foreground color of the character is specified by the remaining 3 bits of the character's color pointer, while the character's background color is specified by Register F (CR_F).

With Multicolor mode selected, each TWO bits of a character cell correspond to ONE dot on-screen and the color of that dot is determined by the two-bit code. Unlike HI-RES mode, in which only two colors can be displayed in a single character, Multicolor mode allows four colors per character; however, since two bits of cell data now correspond to a single dot on-screen, the horizontal resolution is half that of the HI-RES mode. That is, each 8x8 Character Cell in memory maps onto an 8x4 character on-screen (8 lines of 4 dots each). Note that the amount of memory required for these 8x4 Multicolor characters is the same as that for 8x8 HI-RES characters, the data is simply mapped differently on-screen.

In Multicolor mode, the two bits which make up a dot select one of four colors for that dot. The four codes created by these two bits tell VIC where to find the color information for the dot. The color of the dot can be either the Background color (in CR_F), the Exterior Border color in (CR_F), the Auxiliary color (in CR_E) or the Foreground color (bits 0 thru 2 of the character's color pointer).

The Multicolor mode color select codes are:

00—Background color (CR_F)
01—Exterior Border color (CR_F)
10—Foreground color (Color RAM)
11—Auxiliary color (CR_E)

Note that the two-bit code is NOT itself a color code, rather it is a pointer to four different color codes, allowing greater color flexibility, as each code pointed to has either 3 or 4-bit resolution.

EXAMPLE:

Given CR_F = 1F Character Background color is WHITE (1)
Exterior Border color is YELLOW (7)
Invert is not selected (8 = 1)

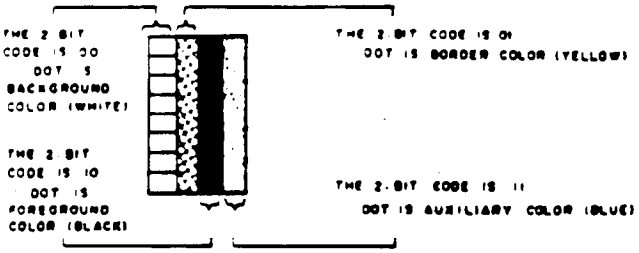
CR_E = 6X Auxiliary color is BLUE (6)

and a character definition of:

	Bit 76543210	=HEX
byte 0	00011011	1B
1	00011011	1B
2	00011011	1B
3	00011011	1B
4	00011011	1B
5	00011011	1B
6	00011011	1B
7	00011011	1B

If the color pointer nybble for that character is 0 (0000) then the Foreground color is BLACK (0) and HI-RES mode is selected (MSB = 0). The character will then appear on-screen as

If the color pointer nybble for that character is 8 (1000) then the Foreground color is BLACK (0) and Multicolor mode is selected (MSB = 1). The character will then appear on-screen as



(Note that this is given solely as an example and due to color translation limitations of most TV sets closely spaced dots of different colors will not appear sharply defined on-screen.)

Since the mode of display for a character is selected by the character's color pointer and each character location on-screen has a unique color pointer it is possible to freely intermix HI-RES and Multicolor characters. This provides great display flexibility allowing HI-RES characters for alphanumerics etc. and Multicolor characters for a wider array of colors available simultaneously.

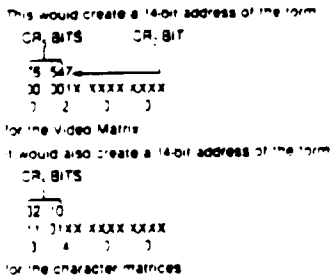
EXAMPLE OF VIC CONTROL REGISTER USE:

For simplicity, assume all characters are in the HI-RES mode and the VIC Registers are loaded with the following values:

REG	CONTENTS (HEX)	BINARY	RESULTS
CR_0	03	0/000 0011	Moves Video Matrix over 3(x4) dot widths from the left side of the screen. Interlace is not selected (I = 0).
CR_1	19	0001 1001	Moves Video Matrix down HEX 19 (x2) dot heights from top of screen.
CR_2	96	1/001 0110	Sets HEX 16 (= 22 base 10) columns in Video Matrix. (Bit 7 is used with CR_3.)
CR_3	2E	X/010 111/0	Sets 010111 (= 23 base 10) rows in Video Matrix. 8 x 8 character matrices are selected (D = 0).

EXAMPLE OF VIC CONTROL REGISTER USE: (Continued)

REG	CONTENTS (HEX)	BINARY	RESULTS
CR_5	Should be set to access the proper memory locations of the specific system. Suppose it is desired to locate the Video Matrix starting at address HEX 0200, and the character matrices starting at address HEX 3400. In order to accomplish this, CR_5 is set:		
CR_5	0D	0000 1101	and bit 7 of CR_2 is set to 1.



CR_A	00	0/000 0000	Oscillator 1 is OFF.
CR_B	9A	1/001 1010	Oscillator 2 is ON, with a relative frequency of 1A.
CR_C	00	0/000 0000	Oscillator 3 is OFF.
CR_D	A5	1/010 0101	Noise generator is ON with a relative frequency of 25.
CR_E	XF	XXXX 1111	Sound effects are set for loudest volume.
CR_F	0E	0000/1/110	The background color common to all characters is black (0), the border color is dark blue (6) and each character is displayed in its own color on the black background (R = 1).

These register values will produce a screen with a properly centered Video Matrix of 23x22 characters, each character appearing in color on a black background, with a dark blue border surrounding the Video Matrix area. Additionally, the sound effects generator will be producing a pitched oscillation, along with white noise.

All of these registers can be modified to produca different effects.

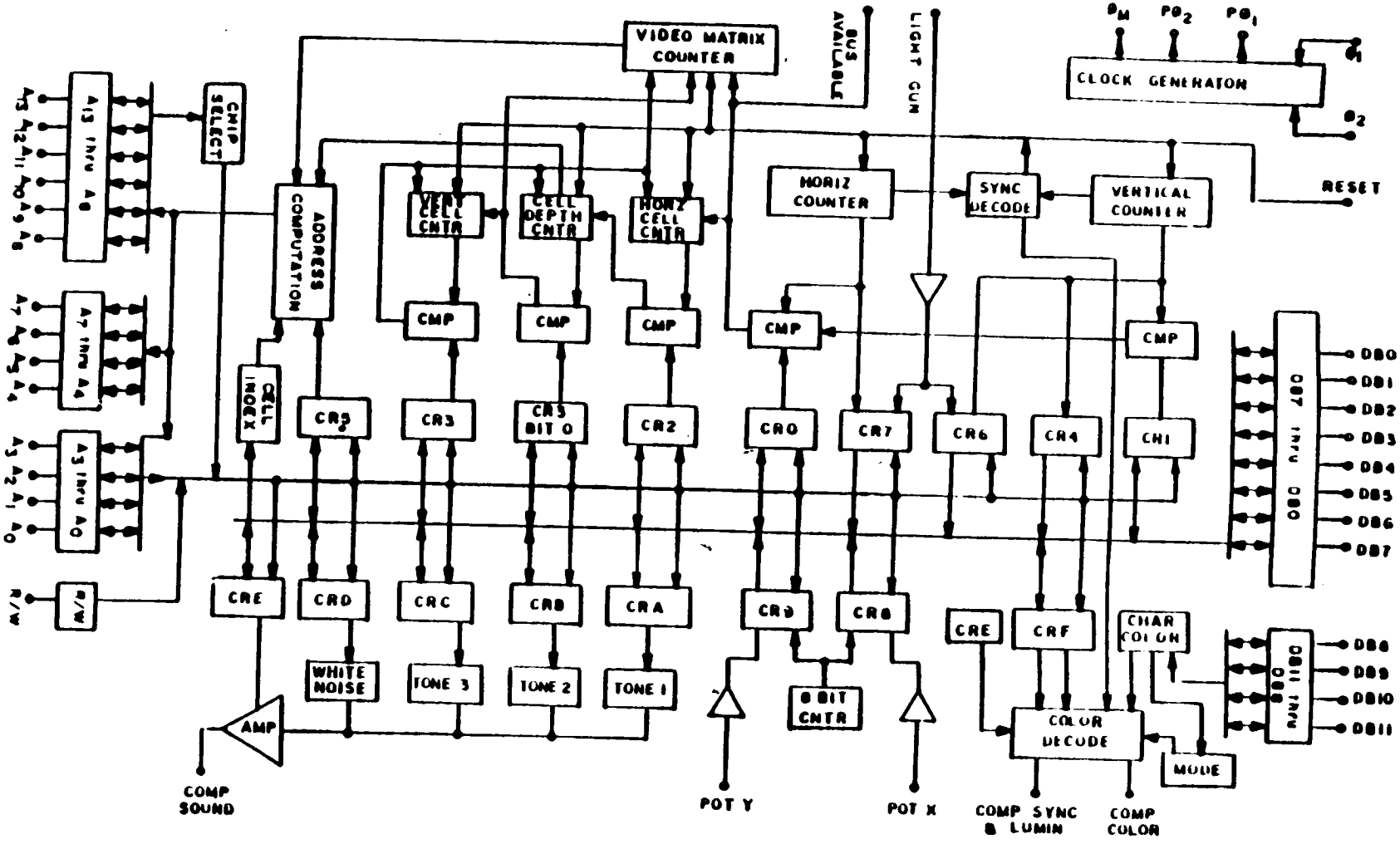
For example:

If the number in CR_0 is increased, the Video Matrix region will shift farther to the right.

If the number in CR_B is reduced (leaving bit 7 a one) the frequency of oscillator 2 will go down.

If CR_E is changed to 06 (turning R OFF), the border will remain dark blue, but now the Video Matrix will appear as black characters on different colored backgrounds.

In order for VIC to produce a picture on-screen, the number of rows and columns and appropriate centering values must be loaded into the proper registers.



6560 BLOCK DIAGRAM

6560 PIN SIGNAL DESCRIPTION

- **Address Bus—Pins 21 thru 34**

The 14 bit address bus (A_0 thru A_{13}) is bidirectional. During $P\varnothing_2 = 1$, the address pins are in the input mode. In this mode the microprocessor can access any of the sixteen VIC Control Registers. The high order pins of the Address Bus (A_8 thru A_{13}) act as Chip Select pins in this input mode. A true chip select condition occurs when $A_{13} = A_{11} = A_{10} = A_9 = A_8 = 0$ and $A_{12} = 1$. which equates to a VIC chip select address of 1000 in HEX. The lower order 4 bits of the address bus (A_0 thru A_3) are used as the control register select portion of the input address.

During $P\varnothing_1 = 1$, the VIC address pins will be in the output mode if data (either Character Pointer or Character Cell) is to be fetched. In this mode, VIC will put out the address of the memory location to be fetched. The address from VIC will be valid 50ns after the rising edge of $P\varnothing_1$ and remain valid until the rising edge of $P\varnothing_2$.

- **Read/Write—Pin 4**

This signal is an input only on the 6560 and controls the flow of data between VIC and the microprocessor. When the R/W signal is low and the VIC chip select conditions have been satisfied, the microprocessor can write data into the selected VIC Control Register. If the R/W signal is high and the chip select conditions have been met, the microprocessor can read data from the selected VIC Control Register.

It is important to note that all VIC/microprocessor data transfers can only occur when $P\varnothing_2 = 1$. During $P\varnothing_1$, the VIC will be fetching data from memory for display and the R/W signal must be held high to insure that VIC will not write into any memory location.

- **Data Bus—Pins 5 thru 16**

The 12 bit data bus of the 6560. DB_0 thru DB_{11}, is divided into two sections. The lower order eight bits, DB_0 thru DB_7, are used both to interface to the microprocessor and fetch data needed for display, while the higher order 4 bits are used exclusively for retrieving color and mode information. The operation of the lower order eight bits (DB_0 thru DB_7) can also be separated into two categories: microprocessor interface and video data interface. During $P\varnothing_2 = 1$, DB_7 thru DB_0 are used exclusively for data transmission between the microprocessor and VIC. During $P\varnothing_1 = 1$, DB_7 thru DB_0 are used for fetching display data.

CLOCKS

1) **Master Oscillator Clock Inputs**—$\varnothing_1$ and $\varnothing_2$, Pins 39 and 38

The 6560 requires a 14.31818 MHz (NTSC), TWO Phase Clock. The clock signals must be five (5) volts and non-overlapping. The 6561 requires a 4.436187 MHz clock for PAL standard.

2) **System Clocks**—$P\varnothing_1$ and $P\varnothing_2$, Pins 35 and 36

These clocks are the master timing generator for the VIC System. They are five volt, non-overlapping 1.02 MHz clocks capable of driving the capacitance of the 6512 microprocessor.

3) **Memory Clock**—$\varnothing_M$ (Option), Pin 37

This is a single phase 2.04 MHz clock used when memories in the VIC System require a strobe after the address bus is valid.

- **Analog to Digital Converters**—POTX and POTY, Pins 17 and 18

These input pins are used to convert potentiometer position into a microprocessor readable 8 bit HEX number. This is accomplished by a simple RC time constant integration technique. The potentiometer is used to charge an external capacitor tied to the pot pin. Refer to application note No.1 (insert).

- **Composite Sound**—Pin 19

This pin provides the output of the sound synthesizer portion of the 6560 shown in the VIC Block Diagram. It is a high impedance output (approximately 1KΩ) and must be buffered and amplified externally to drive a speaker.

- **Composite Sync and Luminance**—Pin 3

This pin is an open drain output which provides all the necessary video synchronization and luminance information required by a standard television. Refer to application note No. 1 (insert).

- **Composite Color**—Pin 2

This signal provides the necessary color information required by a standard television to receive a full color picture. The composite color pin is a high impedance output buffer which provides the reference burst signal plus the color encoded phase and amplitude information at the proper 3.579545 MHz frequency. Refer to application note No. 1 (insert).

- **Reset—(Option), Pin 37**

This input signal is used to synchronize the horizontal and vertical sync counter to an external signal.

- **Bus Available**—(Option), Pin 37

This output signal indicates the state of VIC with respect to the video memory fetch. The pin will go low 2 μsec. before VIC performs any memory access and will remain low until the entire screen has been refreshed.

- **Light Gun/Pen**—(Option), Pin 37

This input signal causes the current dot position being scanned onto the screen to be latched into control registers 6 and 7, upon a negative going edge. This pin would be used in conjunction with a photo detector for use in a "target shoot" type game or for light pen applications. Refer to application note No. 1 (insert).

NOTE 1

OPTION ALTERNATIVES

1) ϕ_M—2.0 MHz Clock for Clocked Memories/6560-001
2) RESET—Reset Horizontal and Vertical counters to Vertical Sync./6560-201
3) LIGHT PEN—Negative edge triggered latch of raster position 6560-101
4) BUS AVAILABLE—Pin is low when VIC is displaying data/6560-301

NOTE 2

AVAILABLE AUXILIARY/BACKGROUND COLORS

0 BLACK	8 ORANGE
1 WHITE	9 LIGHT ORANGE
2 RED	A PINK
3 CYAN	B LIGHT CYAN
4 MAGENTA	C LIGHT MAGENTA
5 GREEN	D LIGHT GREEN
6 BLUE	E LIGHT BLUE
7 YELLOW	F LIGHT YELLOW

AVAILABLE BORDER/ CHARACTER COLORS

0 BLACK
1 WHITE
2 RED
3 CYAN
4 MAGENTA
5 GREEN
6 BLUE
7 YELLOW

6560 ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias	– 10° to 80°C
Storage Temperature	– 65°C to 150°C
Voltage on any Pin*	– 0.5v to + 7v
Power Dissipation	1.0W

*With respect to Ground

COMMENT

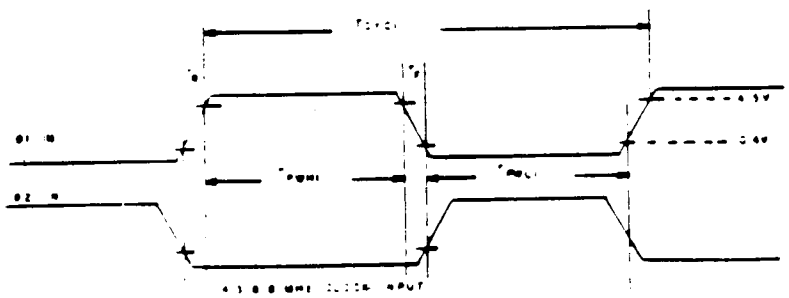
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS $T_A = 0°C$ to $+50°C$, $V_{DD} = 5v \pm 5\%$ (unless otherwise specified)

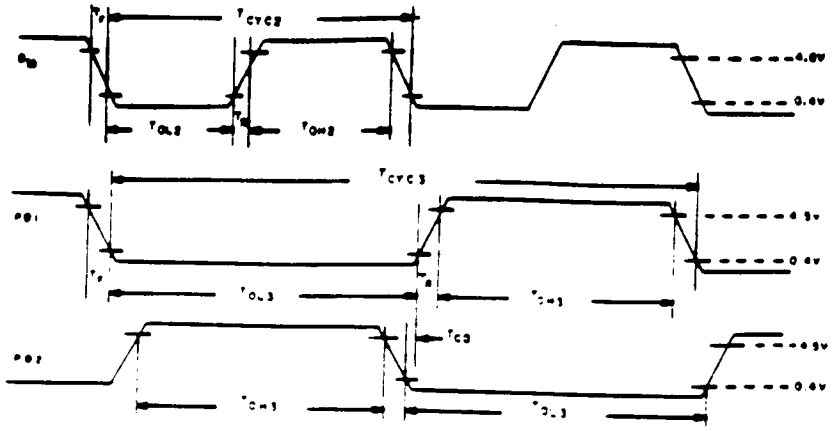
CHARACTERISTIC	MIN.	MAX.	TYP.	UNITS
Read/Write, Reset (Option)				
Address and Data-Input State				
V_{IL}	– 0.2	0.4	—	Volts
V_{IH}	2.4	5.6	—	Volts
Input Capacitance	—	8.0	5.0	pF
Input Leakage	—	10.0	1.0	μA
(all outputs in high impedance state)				
Address and Data-Output State				
V_{OL}	—	0.4	—	Volts
V_{OH}	2.4	—	—	Volts
I_{OL}—Sink current $V_{OL} = 0.4$	2.4	—	—	mA
I_{OH}—Source current $V_{OH} = 2.4$	200	—	—	μA
Impedance in Three State Condition	1×10^6	—	—	Ohms
Clock Input (ϕ_1 and ϕ_2 Input)				
Frequency	—	—	14.31818	MHz
Capacitance	—	10.0	—	pF
V_{IL}	– 0.2	0.3	—	Volts
V_{IH}	4.5	—	5.0	Volts
Clock Outputs ($P\phi_1$, $P\phi_2$)				
V_{OL}	—	0.3v	—	Volts
I_{OL} @ 0.3 Volts V_{OL}	1.6	—	—	mA
V_{OH}	$V_{DD} - 2$	—	—	Volts
I_{OH} @ 4.7 Volts V_{OH}	200	—	—	μA
Loading	—	120.0	—	pF
Frequency	—	—	1.02	MHz

6560 ELECTRICAL SPECIFICATIONS (Continued)

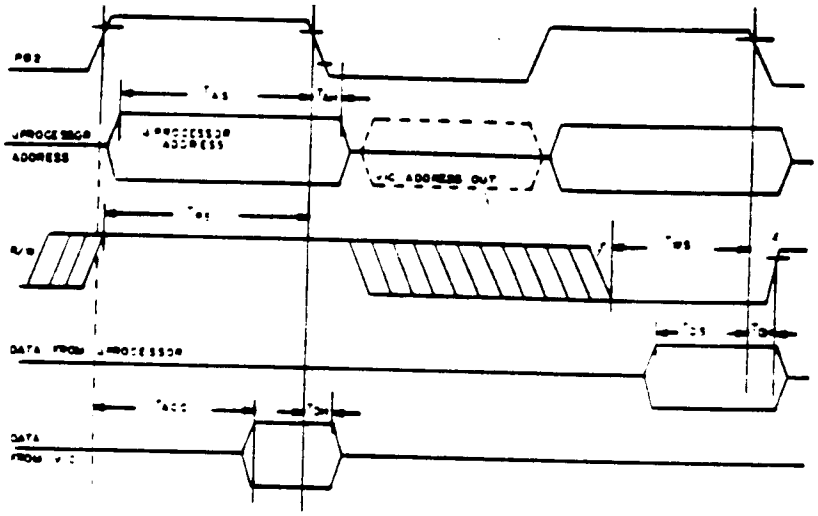
CHARACTERISTIC	MIN.	MAX.	TYP.	UNITS
Composite Sound				
Output Impedance	—	2000	1000	Ω
Max. Current (Sink or Source)	—	500	—	μA
Output Offset Voltage	2.2	2.8	2.5	Volts
V_{OH} (Max. Amplitude)	3.2	—	3.5	Volts
V_{OL} (Max. Amplitude)	—	1.8	1.5	Volts
V_{OH} (Min. Amplitude)	2.55	—	2.6	Volts
V_{OL} (Min. Amplitude)	—	2.45	2.4	Volts
Pot Inputs				
$V_{TRIGGER}$ (Rising Edge)	2.2	2.8	2.5	Volts
Pot Reset				
V_{OL}	—	0.2	—	Volts
I_{OL} @ V_{OL} = 0.2	500	—	—	μA
Light Pen Input (Option)				
$V_{TRIGGER}$ (Falling Edge)	2.8	2.2	2.5	Volts
ϕ_M (Option)				
V_{OL}	—	0.4	—	Volts
I_{OL} @ 0.3 Volts V_{OL}	1.6	—	—	mA
V_{OH}	V_{DD} - .7	—	—	Volts
I_{OH} @ 4.7 Volts V_{OH}	100	—	—	μA
Loading	—	60	—	pF
Frequency	—	—	2.04	MHz
Bus Available (Option)				
V_{OL}	—	0.3	—	Volts
I_{OL}	1.6	—	—	mA
V_{OH}	2.4	—	—	Volts
I_{OH}	100	—	—	μA
V_{DD}	4.75	5.25	5.00	Volts
I_{DD}	—	150	120	mA



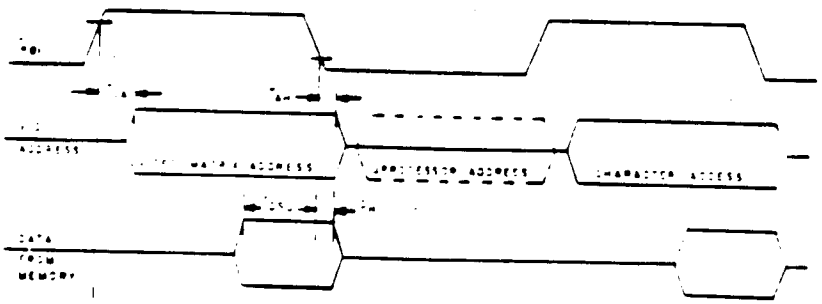
VIC INPUT CLOCKS



VIC OUTPUT CLOCKS



MICROPROCESSOR READ/WRITE TIMING TO VIC



VIC READ TIMING FROM MEMORY

VIC SYSTEM TIMING

VIC INPUT CLOCK TIMING

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
Input Clock Cycle Time	T_{CYC1}	69.82	—	69.84	ns
Clock High	T_{PWH1}	20	—	—	ns
Clock Low	T_{PWL1}	20	—	—	ns
Rise and Fall Time	T_R, T_F	—	—	10	ns

VIC OUTPUT CLOCK TIMING

Two MHz Clock Cycle Time	T_{CYC2}	480	—	500	ns
ϕ_M Clock Output Low	T_{OL2}	200	—	260	ns
ϕ_M Clock Output High	T_{OH2}	180	—	250	ns
1MHz μProcessor Clocks Cycle Time	T_{CYC3}	960	—	990	ns
$P\phi_1$, $P\phi_2$ Clocks Low	T_{OL3}	380	—	500	ns
$P\phi_1$, $P\phi_2$ Clocks High	T_{OH3}	380	—	500	ns
Delay Time Between Clocks At .4v	T_{CD}	5	—	20	ns
Rise Time. Max. C_L	T_R	—	—	80	ns
Fall Time. Max. C_L	T_F	—	—	40	ns

MICROPROCESSOR READ/WRITE TIMING TO VIC

Address Set Up Time	T_{AS}	375	—	—	ns
Address Hold Time	T_{AH}	5	—	—	ns
Read Set Up Time	T_{RS}	375	—	—	ns
Write Set Up Time	T_{WS}	275	—	—	ns
Data In Set Up Time	T_{DS}	200	—	—	ns
Data Access Time	T_{ACC}	350	—	—	ns
Data Hold Time	T_{DH}	30	—	—	ns

VIC READ TIMING FROM MEMORY

Time To Valid Address From $P\phi_1$	T_{VA}	—	—	70	ns
Address Hold Time	T_{AH}	10	—	40	ns
Data Set Up Time	T_{DSU}	60	—	—	ns
Data Hold Time	D_H	20	—	—	ns

COMPOSITE SYNC, COLOR AND LUMINANCE TIMING

Blanking Period (No Video)	BLANKING	10.0	11.0	12.0	μs
Breeze Way	B_S	3	.5	7	μs
Color Burst Reference Signal	BURST	4.0	5.0	6.0	μs

Note 1: The color burst signal is the 3.579545 MHz color phase reference from which all other color information is measured.

For Example: Full intensity blue is a 3.579545 MHz signal which has a relative delay of 135ns from burst if the burst signal was available throughout the entire H_L period

COMPOSITE SYNC OUTPUT TIMING

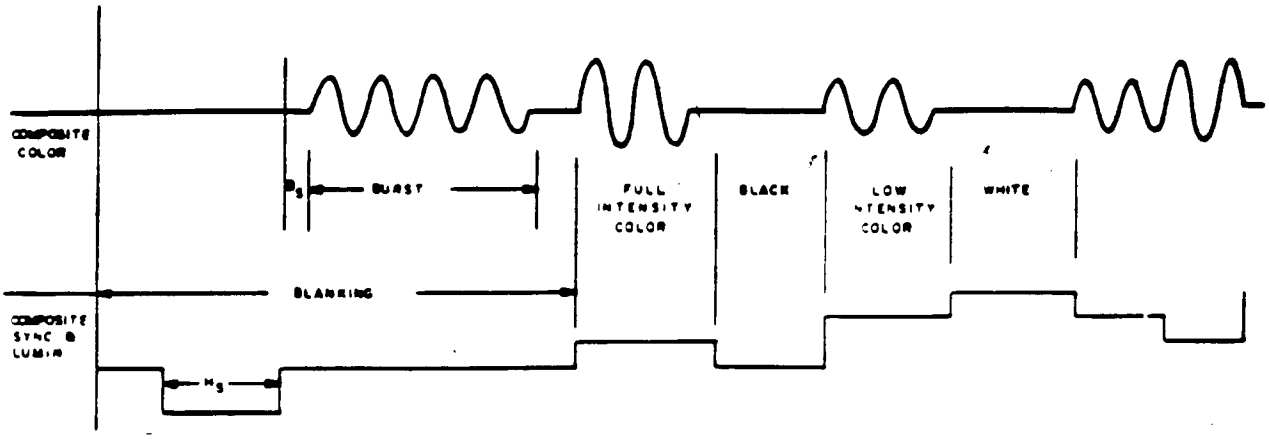
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
Horizontal Sync Pulse	H_S	4.0	5.0	6.0	µs
Horizontal Line Period	H_L	63.0	63.5	64.0	µs
One Half Horizontal Line Period	$H_{L/2}$	30.0	31.5	32.5	µs
Equalization Pulse	E	2.0	2.5	3.0	µs
Equalization Time Period	E_L	188.0	190.5	192.0	µs
Vertical Sync Period	V_S	188.0	190.5	192.0	µs
Vertical Sync to Vertical Sync Time Period	V_S to V_S	—	16.66	—	ms

Notes:

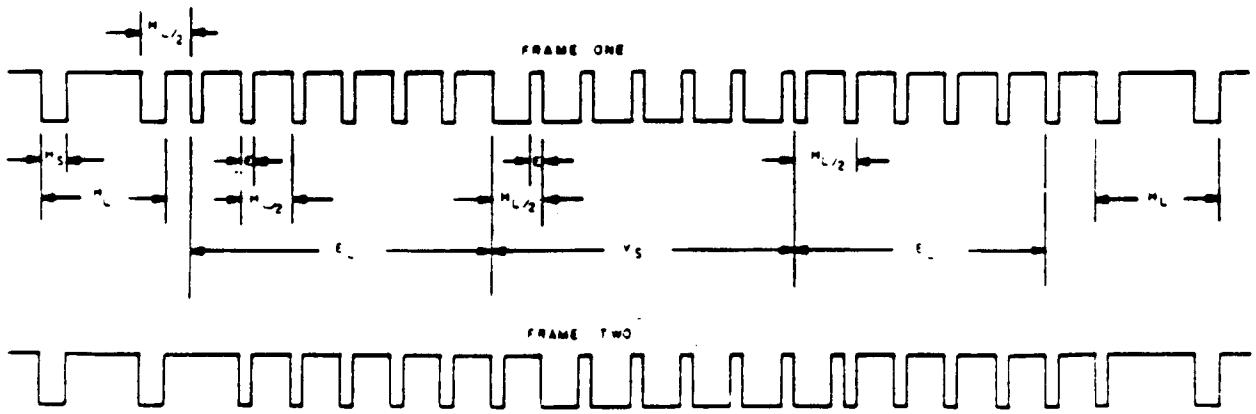
a) The number of H_L periods between V_S periods is 262.5 in the interlace mode.

b) The number of H_L periods between V_S periods in the non-interlace mode is 262 per frame.

c) NTSC only.



COMPOSITE SYNC, COLOR AND LUMINANCE



COMPOSITE SYNC OUTPUT

MINIMUM SYSTEM DESCRIPTION

A minimum VIC System would consist of a microprocessor, VIC, ROM, RAM and I/O. The basic system includes one μP (6512), one Video Interface Chip (VIC/6560), one PIA (6520), two 1K x 4 static RAMS, two 256 x 4 static RAMS, and one or more program/graphics ROMS (2K x 8 or 4K x 8).

The tasks involved in a complete game are divided between the μP and VIC. The μP controls the game logic and VIC controls the video display as well as the sound generation.

SYSTEM COMPONENTS:

- **6512 Microprocessor**

The 6512 is a member of the 6500 microprocessor family, which has gained wide acceptance in the video game industry. The 6512 architecture and addressing capability are well suited to graphic data manipulation. Details concerning the 6512 may be found in the 6500 Hardware Manual. Alternately, a 6502 processor can be used by feeding VIC ϕ_2 OUT into the 6502 ϕ_2 IN; however, tri-state buffers must then be added to the data bus as well as the address bus.

- **6560 Video Interface Chip**

The 6560 is a video display device which reads data that has been formatted by the μP and supplies the appropriate color graphic signals to the RF modulator. To accomplish this, the 6560 does a transparent D.M.A. of the μP's memory space accessing ROM and/or RAM.

- **6520 Peripheral Interface Adapter**

This chip is used for keyboard scanning and joystick multiplexing.

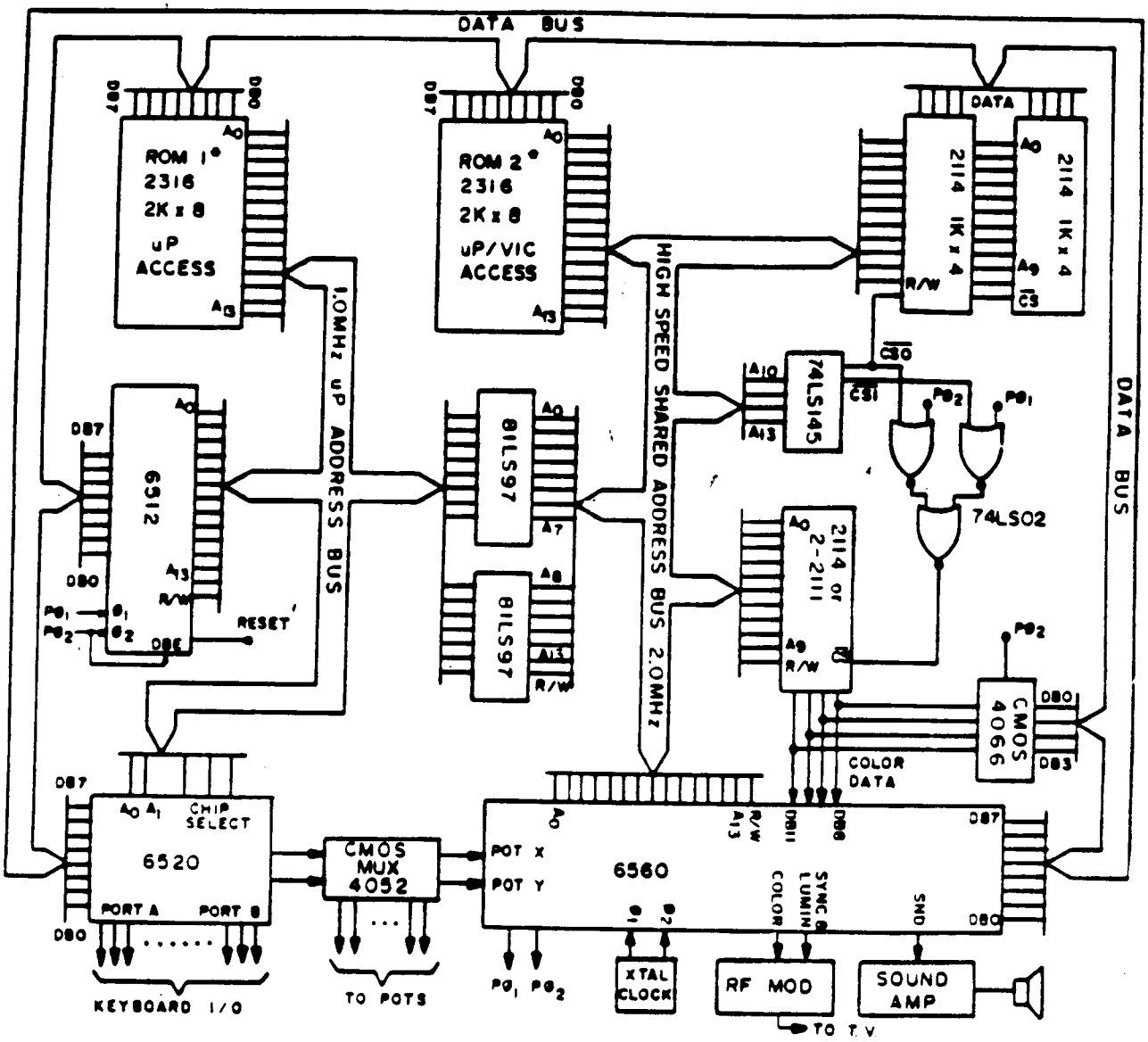
- **Resident RAM = 2 (2114) and 2 (2111)**

These RAM chips are used as working storage by the μP and for holding the screen organization and color matrices. They may be modified by the μP at any time. Note that in order to achieve a full bit-map display, a minimum of 4K bytes of character RAM are necessary.

- **Program/Graphics ROM(s)**

These chips normally contain the game logic and/or coded graphic data. There is no need for a resident ROM in a minimum system. A cartridge ROM can contain all the relevant information.

VIC MINIMUM SYSTEM



*Note: ROM 1 or ROM 2 is optional, since either can be cartridge loaded. ROM 1 is accessed by the processor only. ROM 2 can be accessed by the processor or VIC.