APPLICATION		REVISIONS			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
		3	REVISED PER ECO # 30016	7/17/?1	BFK

FUNCTIONAL DESCRIPTION

This specification describes an integrated circuit to be used as a control and timing element in a microcomputer. All aspects of this IC are defined including electrical characteristics and mechanical packaging.

The control and timing integrated circuit as shown in the block diagram of Figure 2 consists of six major parts:

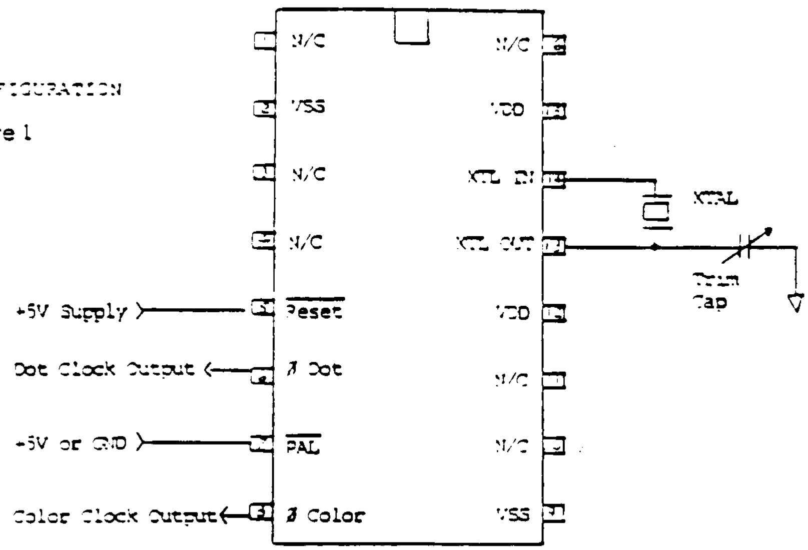
1. Crystal oscillator
2. Color frequency output buffer
3. Frequency doubler and internal clock generator
4. Frequency divider
5. Pulse shaper
6. Dot frequency output buffer

The oscillator circuit uses an external crystal to generate a precise frequency, compatible with either PAL or NTSC video systems. This frequency can be fine-adjusted using an external trimmer capacitor (See Figure 1). The output of this oscillator is buffered and becomes the color clock output. It also goes to the frequency doubler circuit. From there a pair of non-overlapping clocks are generated (PHI1 and PHI2). These go to the frequency divider which in turn generate a pair of signals, ÷3 pulse and ÷3 pulse. Their frequency is determined by the state of the PAL/NTSC input pin. These two pulses go through some digital delays, and with the help of PHI1 and PHI2 are re-combined to form the dot clock frequency. This signal is then buffered and sent out via the dot clock pin.

For test purposes a reset input pin is provided. When held low the frequency divider is reset to a known state and frozen. Upon its subsequent release, the frequency divider resumes its normal function. This input has a weak pullup device and during normal operation can either be tied high or left open. SCICARD # IS M00164

PIN CONFIGURATION

Figure 1



SHEET						
REV STATUS OF SHEETS	REV	B	B	B	B	3
	SHEET	1	2	3	4	5

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCES
ANGLES ±1°
2 PLACE DECIMALS ±.02
3 PLACE DECIMALS ±.010

DRWN	D Charles	5/2/84
SYSTEMS ENG	[illegible]	7/9/84
TEST ENG	[illegible]	7/11/84
CIRCUIT ENG	[illegible]	5/3/84
COMP ENG	[illegible]	5/3/84

COMMODORE

TITLE

IC, CLOCK GENERATOR

8701 / 8701N

SIZE A | DRAWING NO. 251527-01

SCALE — | SHEET 1 OF 5

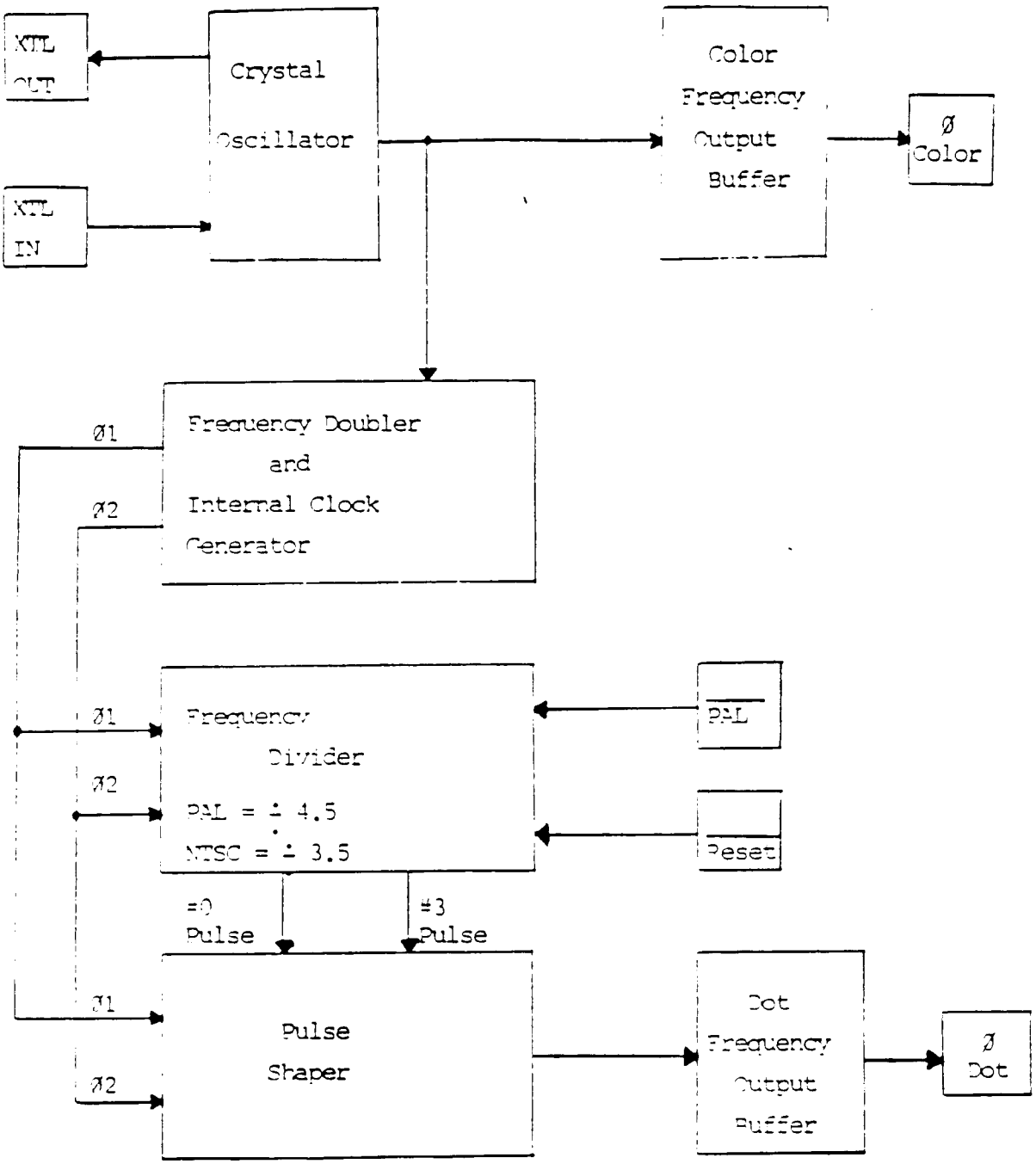


Figure 2: Block Diagram

COMMODORE	TITLE: IC, CLOCK GENERATOR	
SIZE A	DRAWING NO. 25/512-01	REV B
SCALE	SHEET 2 OF 5	

PAL/NTSC OPERATION

When this component is used by a PAL type system, the crystal will have a frequency of 17.734475 MHZ. The frequency doubler takes this to approximately 35.5 MHZ and the divider circuit divides it by 4.5 resulting in a dot clock frequency of 7.881989 MHZ. On the other hand, in a NTSC type system the crystal will have a frequency of 14.318180 MHZ. The frequency doubler circuit raises this to approximately 28.6 MHZ and it is divided by 3.5 to yield a dot clock rate of 8.181817 MHZ. Divider operation is determined by the PAL/NTSC input pin. A high at this pin establishes NTSC operation, a low sets up PAL operation. A pullup device is provided on this input, so that this pin can be left open for NTSC operation.

PINOUT

1.	N/C	16.	N/C
2.	VSS	15.	VDD
3.	N/C	14.	XTL IN
4.	N/C	13.	XTL OUT
5.	RESET	12.	VDD
6.	Ø DOT	11.	N/C
7.	PAL	10.	N/C
8.	Ø COLOR	9.	VSS

DC CHARACTERISTICS

Absolute Maximum Ratings

	MIN	TYP	MAX	UNITS
Supply voltage, VDD-VSS	0	- -	7.0	V
Input voltage	-2.0	- -	7.0	V
Operating free air temperature, TA	0	- -	70	°C

Electrical Characteristics (VCC = 5.0V ± 5%, VSS = 0V, TA = 0° to 70°C)

Power Supply Current			50	MA
Input Leakage			±10	uA
Color and Dot Clock Outputs				
High level output voltage, VOH	2.4	- -	- -	V
Low level output voltage, VOL	- -	- -	0.4	V
High level output current, IOH	80	- -	- -	uA
Low level output current, IOL	3.2	- -	- -	mA
Reset and PAL Inputs				
High level input voltage, VIH	VCC	- -	- -	V
Low level input voltage, VIL	- -	- -	VSS	V

AC Characteristics: (VCC = 5.0V ± 5%, VSS = 0V, T_A = 0° to 70° C)
See Figure 3 for Timing Diagrams

8701F6

	MIN	TYP	MAX	UNITS
Output clock loading	- -	- -	20.0	PF
Output clock transition time	- -	- -	15.0	NS
NTSC timing (oscillator operating frequency = 14.318 MHz)				
Ø color cycle time	- -	- -	69.8	NS
Ø dot cycle time	116.0	- -	139.2	NS
Color clock low pulse width	27.9	34.9	41.9	NS
Color clock high pulse width	27.9	34.9	41.9	NS
Dot clock low pulse width	45.0	61.1	77.2	NS
Dot clock high pulse width	45.0	61.1	77.2	NS
PAL timing (oscillator operating frequency = 17.734 MHz)				
Ø color cycle time	- -	- -	56.4	NS
Ø dot cycle time	116.0	- -	126.9	NS
Color clock low pulse width	22.6	28.2	33.8	NS
Color clock high pulse width	22.6	28.2	33.8	NS
Dot clock low pulse width	45.0	61.1	77.2	NS
Dot clock high pulse width	45.0	61.1	77.2	NS

MECHANICAL REQUIREMENTS:

1. Marking -

   Parts shall be marked with Commodore Part Number, Manufacturers Identification, and EIA Date Code. Pin 1 shall be identified.

2. Packaging -

   Parts shall come in a standard dual-in-line ceramic or plastic package.

AC Characteristics: (VCC = 5.0V ± 5%, VSS = 0V, T_A = 0° to 70° C)
See Figure 3 for Timing Diagrams

8701M6.

	MIN	TYP	MAX	UNITS
Output clock loading	- -	- -	20.0	PF
Output clock transition time	- -	- -	15.0	NS
NTSC timing (oscillator operating frequency = 14.318 MHz)				
Ø color cycle time	- -	- -	69.8	NS
Ø dot cycle time	- -	- -	122.2	NS
Color clock low pulse width	27.9	34.9	41.9	NS
Color clock high pulse width	27.9	34.9	41.9	NS
Dot clock low pulse width	45.0	61.1	77.2	NS
Dot clock high pulse width	45.0	61.1	77.2	NS
PAL timing (oscillator operating frequency = 17.734 MHz)				
Ø color cycle time	- -	- -	56.4	NS
Ø dot cycle time	- -	- -	126.9	NS
Color clock low pulse width	22.6	28.2	33.8	NS
Color clock high pulse width	22.6	28.2	33.8	NS
Dot clock low pulse width	45.0	61.1	77.2	NS
Dot clock high pulse width	45.0	61.1	77.2	NS

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AC Characteristics: (VCC = 5.0V ± 5%, VSS = 0V, T_A = 0° to 70° C)
8701K6™ See Figure 3 for Timing Diagrams

	MIN	TYP	MAX	UNITS
Output clock loading	- -	- -	20.0	PF
Output clock transition time	- -	- -	15.0	NS
NTSC timing (oscillator operating frequency = 14.318 MHz)				
Ø color cycle time	- -	- -	69.8	NS
Ø dot cycle time	116.0	- -	139.2	NS
Color clock low pulse width	27.9	34.9	41.9	NS
Color clock high pulse width	27.9	34.9	41.9	NS
Dot clock low pulse width	45.0	61.1	77.2	NS
Dot clock high pulse width	45.0	61.1	77.2	NS

MECHANICAL REQUIREMENTS:

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2. Packaging -

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AC Characteristics: (VCC = 5.0V ± 5%, VSS = 0V, T_A = 0° to 70° C)
870126 See Figure 3 for Timing Diagrams

	MIN	TYP	MAX	UNITS
Output clock loading	- -	- -	30.0	PF
Output clock transition time	- -	- -	15.0	NS
NTSC timing (oscillator operating frequency = 14.318 MHz)				
3 color cycle time	- -	- -	69.8	NS
8 dot cycle time	- -	- -	139.2	NS
Color clock low pulse width	37.9	34.9	41.9	NS
Color clock high pulse width	37.9	34.9	41.9	NS
Dot clock low pulse width	45.0	61.1	77.2	NS
Dot clock high pulse width	45.0	61.1	77.2	NS

MECHANICAL REQUIREMENTS:

1. Marking -

   Parts shall be marked with Commodore Part Number, Manufacturers Identification, and EIA Date Code. Pin 1 shall be identified.

2. Packaging -

   Parts shall come in a standard dual-in-line ceramic or plastic package.

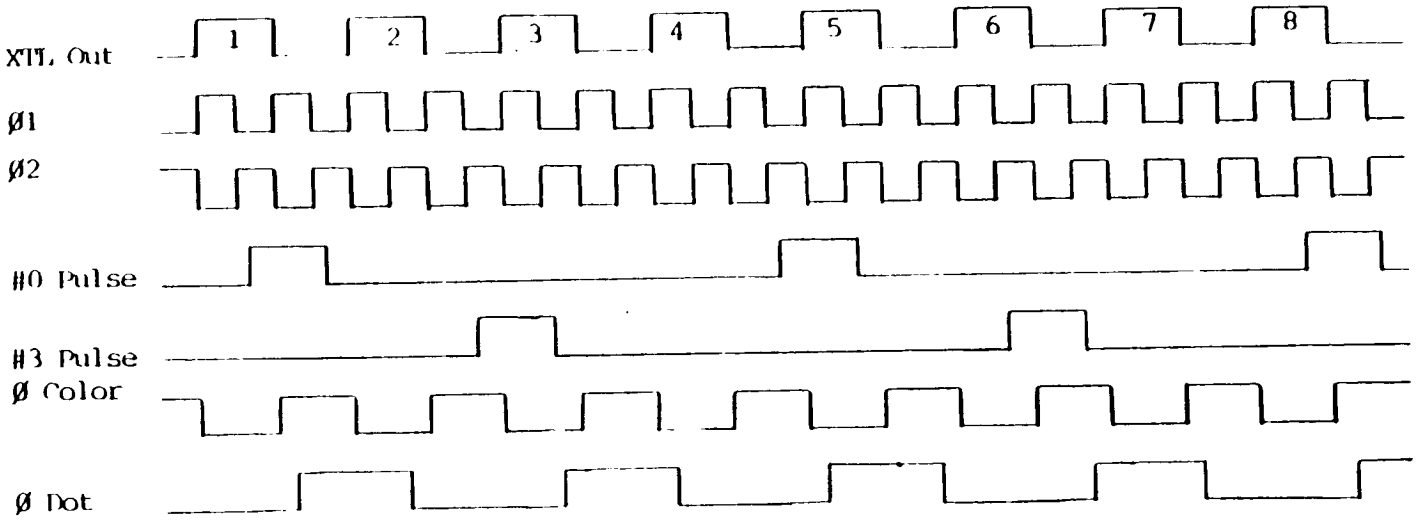
SIZE A | DRAWING NO. 25/327-01 | REV B

COMMODORE

TITLE: IC, CLOCK GENERATOR

SCALE | SHEET 5 OF 5

NTSC Timing



PAL Timing

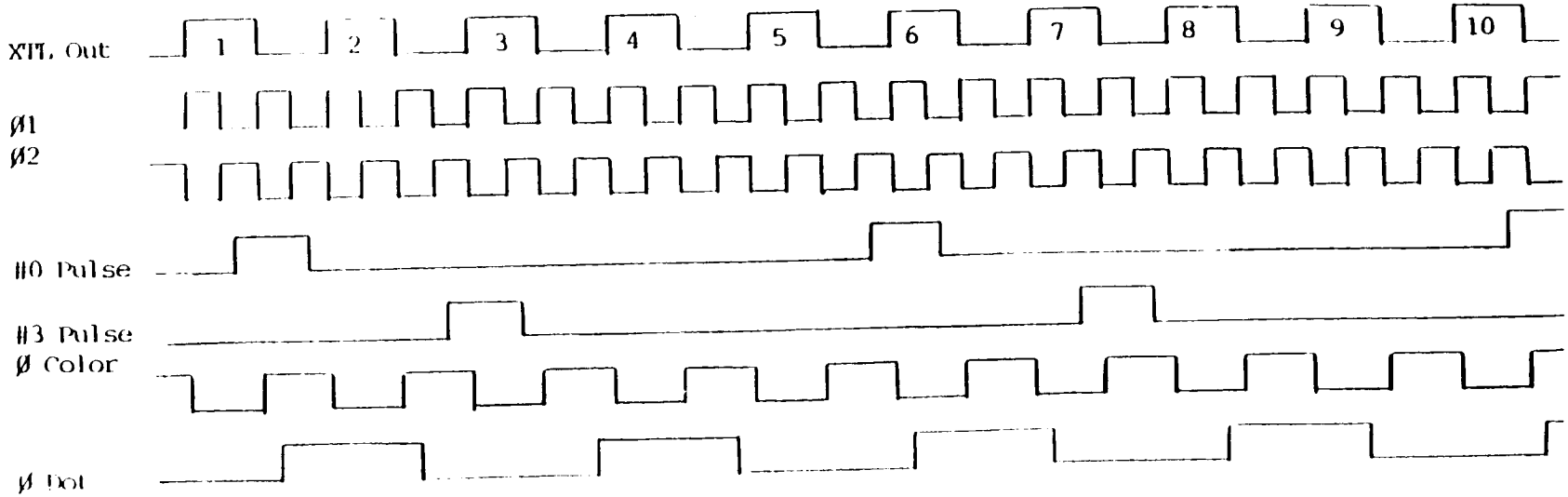


Figure 3: Clock Timing Diagram