COMMODORE SEMICONDUCTOR GROUP

a division of Commodore Business Machines, Inc.

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NMOS

6500 MICROPROCESSORS

THE 6500 MICROPROCESSOR FAMILY CONCEPT —

The 6500 Series Microprocessors represent the first totally software compatible microprocessor family. This family of products includes a range of software compatible microprocessors which provide a selection of addressable memory range, interrupt input options and on-chip clock oscillators and drivers. All of the microprocessors in the 6500 group are software compatible within the group and are bus compatible with the M6800 product offering.

The family includes six microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs, crystal or RC inputs provide the time base. The external clock versions are geared for the multi processor system applications where maximum timing control is mandatory. All versions of the microprocessors are available in 1 MHz, 2 MHz ("A" suffix on product numbers), 3 MHz ("B" suffix on product numbers), and 4 MHz ("C" suffix on product numbers) maximum operating frequencies.

FEATURES OF THE 6500 FAMILY

- Single +5 volt supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- Use with any type or speed memory
- 8 BIT Bi-directional Data Bus
- Addressable memory range of up to 65K bytes
- "Ready" input (for single cycle execution)
- Direct memory access capability
- Bus compatible with M6800
- Choice of external or on-board clocks
- 1 MHz, 2 MHz, 3 MHz and 4 MHz operation
- On-the-chip clock options
  - External single clock input
  - RC time base input
  - Crystal time base input
- Pipeline architecture

MEMBERS OF THE 6500 MICROPROCESSOR (CPU) FAMILY

Microprocessors with On-Chip Clock Oscillator

Model	Addressable Memory
R6502	65K Bytes
R6503	4K Bytes
R6504	8K Bytes
R6505	4K Bytes
R6506	4K Bytes
R6507	8K Bytes

Microprocessors with External Two Phase Clock Inputs

Model	Addressable Memory
R6512	65K Bytes
R6513	4K Bytes
R6514	8 Bytes
R6515	4K Bytes

ORDER NUMBER

MXS 65SS __

FREQUENCY RANGE
NO SUFFIX = 1 MHz
A = 2 MHz
B = 3 MHz
C = 4 MHz

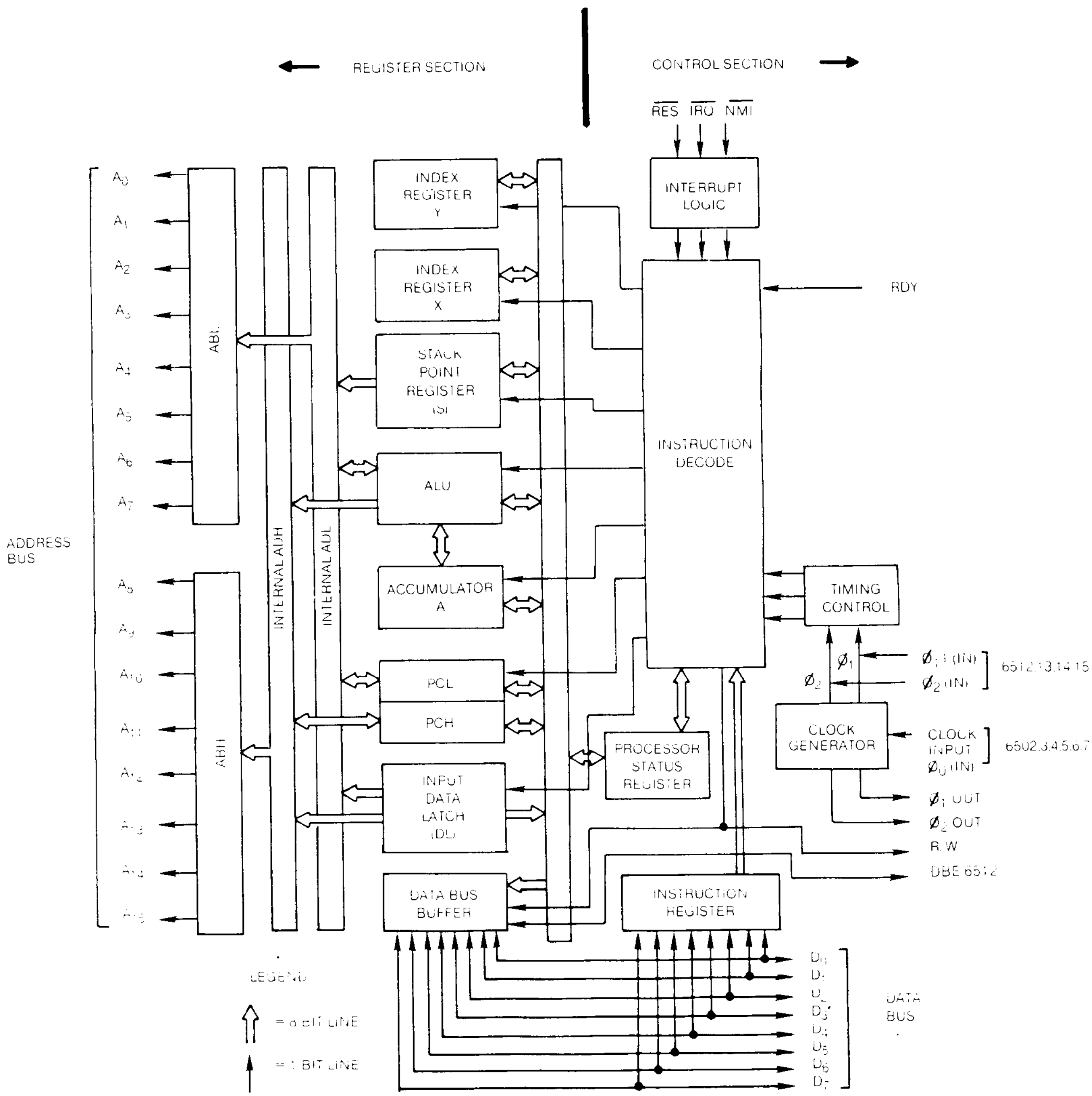
MODEL DESIGNATOR
XX = 02, 03, 04, . . . 15

PACKAGE DESIGNATOR
C = CERAMIC
P = PLASTIC

COMMENTS ON THE DATA SHEET

The data sheet is constructed to review first the basic "Common Characteristics" — those features which are common to the general family of microprocessors. Subsequent to a review of the family characteristics will be sections devoted to each member of the group with specific features of each.

COMMON CHARACTERISTICS



Note: 1. Clock Generator is not included on 6512,13,14,15
2. Addressing Capability and control options vary with each of the 6500 Products.

6500 Internal Architecture

COMMON CHARACTERISTICS

MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	V_{CC}	−0.3 to + 7.0	Vdc
INPUT VOLTAGE	Vin	−0.3 to + 7.0	Vdc
OPERATING TEMPERATURE	T_A	0 to + 70	C
STORAGE TEMPERATURE	T_{STG}	−55 to + 150	C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 5%, Vss = 0, T_A = 0° to + 70°C)

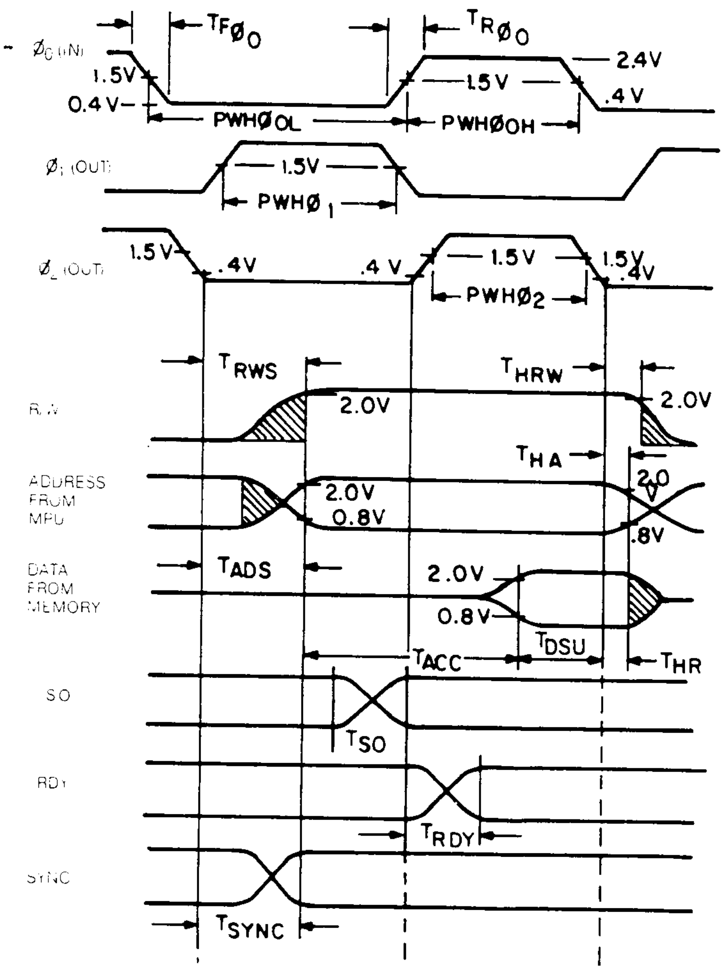
$Ø_1$, $Ø_2$ (in) applies to 6512, 13, 14, 15; O (in) applies to 6502, 03, 04, 05, 06 and 07

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage Logic, $Ø_0$ (in) $Ø_1$, $Ø_2$ (in)	VIH	 Vss + 2.4 Vcc − 0.2	 — —	 Vcc Vcc + 1.0V	 Vdc Vdc
Input High Voltage $\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O.		Vss + 2.0	—	—	Vdc
Input Low Voltage Logic, $Ø_0$ (in) $Ø_1$, $Ø_2$ (in) $\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, Data, S.O.	VIL	 Vss − 0.3 Vss − 0.3 —	 — — —	 Vss + 0.4 Vss + 0.2 Vss + 0.8	 Vdc Vdc Vdc
Input Leakage Current (V_{in} = 0 to 5.25V, Vcc = 5.25V) Logic (Excl. RDY, S.O.) $Ø_1$, $Ø_2$ (in) $Ø_0$ (in)	Iin	 — — —	 — — —	 2.5 100 10.0	 μA μA μA
Three State (Off State) Input Current (V_{in} = 0.4 to 2.4V, Vcc = 5.25V) Data Lines	ITSI	—	—	10	μA
Output High Voltage (I_{OH} = −100μAdc, Vcc = 4.75V) SYNC, Data, A0-A15, R/W	VOH	Vss + 2.4	—	—	Vdc
Out Low Voltage (I_{OL} = 1.6mAdc, Vcc = 4.75V) SYNC, Data, A0-A15, R/W	VOL	—	—	Vss + 0.4	Vdc
Power Supply Current	I_{CC}	—	70	160	mA
Capacitance (V_{in} = 0, T_A = 25°C, f = 1MHz)	C				pF
Logic	C_{in}	—	—	10	
Data		—	—	15	
A0-A15, R/W, SYNC	C_{out}	—	—	12	
$Ø_0$ (in)	$CØ_0$ (in)	—	—	15	
$Ø_1$	$CØ_1$	—	30	50	
$Ø_2$	$CØ_2$	—	50	80	

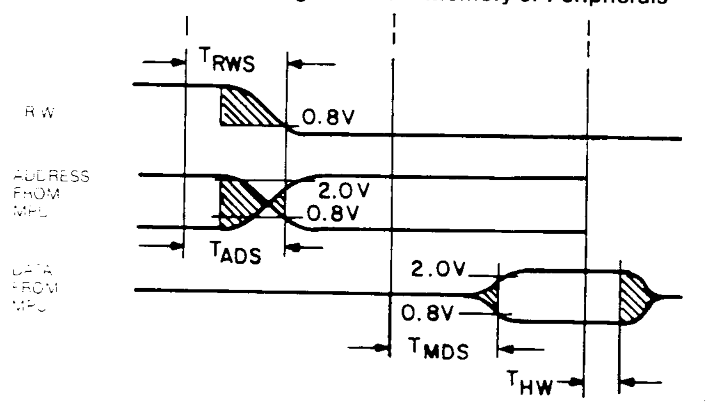
Note: $\overline{IRQ}$ and $\overline{NMI}$ requires 3K pull-up resistors.

COMMON CHARACTERISTICS

Clock Timing — 6502, 03, 04, 05, 06, 07

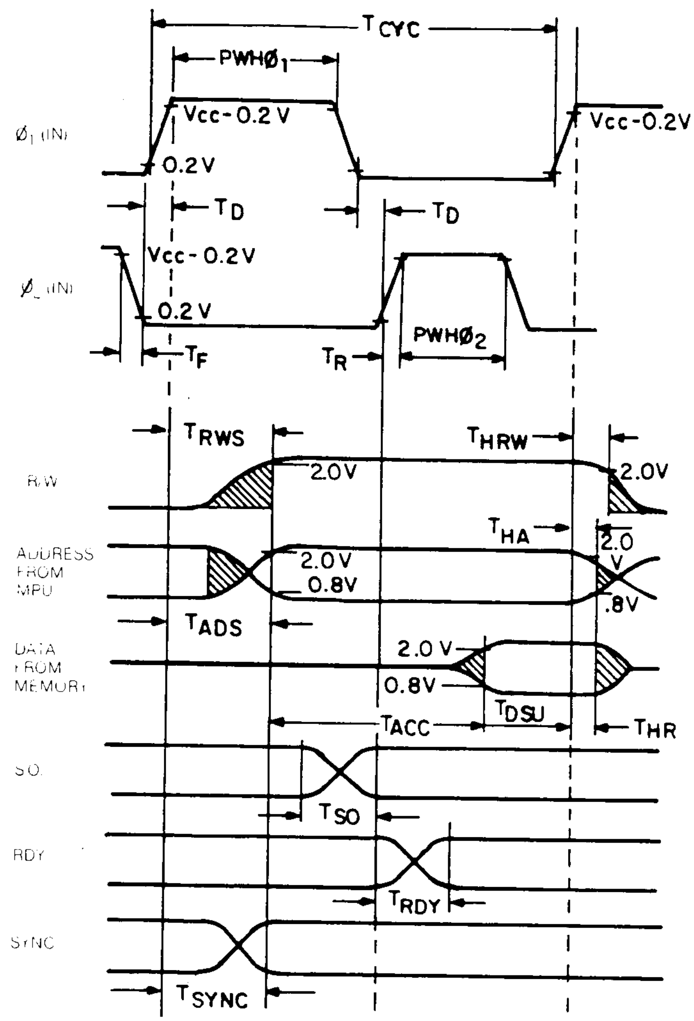


Timing for Reading Data from Memory or Peripherals

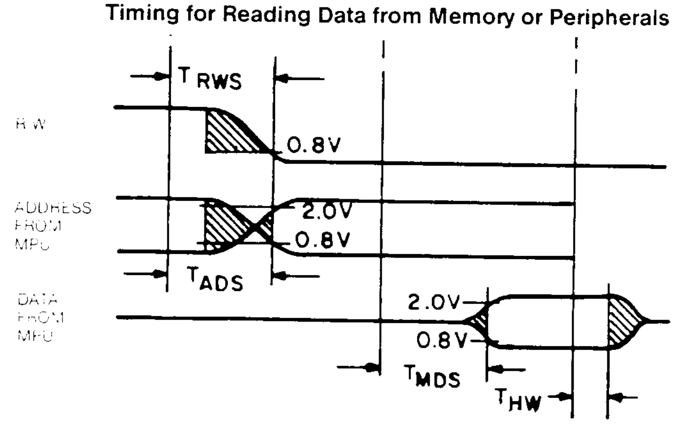


Timing for Writing Data to Memory or Peripherals

Clock Timing — 6512, 13, 14, 15



Timing for Reading Data from Memory or Peripherals



COMMON CHARACTERISTICS

Electrical Characteristics: (Vcc = 5V ± 5%, Vss = 0 V, T_A = 0°-70°C)
Minimum clock frequency = 50 KHz

CLOCK TIMING — 6502, 03, 04, 05, 06, 07

CHARACTERISTIC	SYMBOL	1 MHz TIMING MIN.	TYP.	MAX.	2 MHz TIMING MIN.	TYP.	MAX.	UNITS
Cycle Time	T_{CYC}	1000	—	—	500	—	—	ns
Ø0 (IN) Pulse Width (measured at 1.5v)	PWHØ0	460	—	520	240	—	260	ns
Ø0 (IN) Rise, Fall Time	TRØ0, TFØ0	—	—	10	—	—	10	ns
Delay Time between Clocks (measured at 1.5v)	T_D	5	—	—	5	—	—	ns
Ø1 (OUT) Pulse Width (measured at 1.5v)	PWHØ1	PWHØOL-20	—	PWHØOL	PWHØOL-20	—	PWHØOL	ns
Ø2 (OUT) Pulse Width (measured at 1.5v)	PWHØ2	PWHØOH-40	—	PWHØOH-10	PWHØOH-40	—	PWHØOH-10	ns
Ø1 (OUT), Ø2 (OUT) Rise, Fall Time (measured .0v to 2.0v) (load ½ 30 pf ½ 1 TTL)	T_R, T_F	—	—	25	—	—	25	ns

CLOCK TIMING — 6512, 13, 14, 15

CHARACTERISTIC	SYMBOL	1 MHz TIMING MIN	TYP.	MAX.	2 MHz TIMING MIN.	TYP.	MAX.	UNITS
Cycle Time	T_{CYC}	1000	—	—	500	—	—	ns
Clock Pulse Width Ø1 (Measured at V_{CC}-02V) Ø2	PWH Ø1 PWH Ø2	430 470	—	—	215 235	—	—	ns
Fall Time, Rise Time (Measured from 0.2v to V_{CC}-0.2V)	T_F, T_R	—	—	25	—	—	15	ns
Delay Time between Clocks (Measured at 0.2 V)	T_D	0	—	—	0	—	—	ns

READWRITE TIMING (LOAD = ITTL)

CHARACTERISTIC	SYMBOL	1 MHz TIMING MIN.	TYP.	MAX.	2 MHz TIMING MIN.	TYP.	MAX.	UNITS
Read/Write Setup Time from 6500	T_{RWS}	—	100	300	—	100	150	ns
Address Setup Time from 6500	T_{ADS}	—	100	300	—	100	150	ns
Memory Read Access Time	T_{ACC}	—	—	575	—	—	300	ns
Data Stability Time Period	T_{DSU}	100	—	—	50	—	—	ns
Data Hold Time — Read	T_{HR}	10	—	—	10	—	—	ns
Data Hold Time — Write	T_{HW}	30	60	—	30	60	—	ns
Data Setup Time from 6500	T_{MDS}	—	150	200	—	75	100	ns
S.O. Setup Time	$T_{S.O.}$	100	—	—	50	—	—	ns
SYNC Setup Time from 6500	T_{SYNC}	—	—	360	—	—	175	ns
Address Hold Time	T_{HA}	30	60	—	30	60	—	ns
R/W Hold Time	T_{HRW}	30	60	—	30	60	—	ns
RDY Setup Time	T_{RDY}	100	—	—	50	—	—	ns

COMMON CHARACTERISTICS

Electrical Characteristics: (Vcc = 5V ± 5%, Vss = 0 V, T_A = 0-70 C)
Minimum clock frequency = 50 KHz

CLOCK TIMING — 6502, 03, 04, 05, 06, 07

CHARACTERISTIC	SYMBOL	3 MHz TIMING MIN.	TYP.	MAX.	4 MHz TIMING (1) MIN.	TYP.	MAX.	UNITS
Cycle Time	T_{CYC}	333	—	—	250	—	—	ns
$Ø_{0\ (IN)}$ Pulse Width (measured at 1.5v)	$PWHØ_0$	180	—	170	123	—	127	ns
$Ø_{0\ (IN)}$ Rise, Fall Time	$TRØ_0$, $TFØ_0$	—	—	10	—	—	10	ns
Delay Time between Clocks (measured at 1.5v)	T_D	5	—	—	5	—	—	ns
$Ø_{1\ (OUT)}$ Pulse Width (measured at 1.5v)	$PWHØ_1$	$PWHØ_{OL}$-20	—	$PWHØ_{OL}$	$PWHØ_{OL}$-20	—	$PWHØ_{OL}$	ns
$Ø_{2\ (OUT)}$ Pulse Width (measured at 1.5v)	$PWHØ_2$	$PWHØ_{OH}$-40	—	$PWHØ_{OH}$-10	$PWHØ_{OH}$-40	—	$PWHØ_{OH}$-10	ns
$Ø_{1\ (OUT)}$, $Ø_{2\ (OUT)}$ Rise, Fall Time (measured .8v to 2.0v) (Load ½ 30pf ½ 1 TTL)	T_R, T_F	—	—	25	—	—	25	ns

CLOCK TIMING — 6512, 13, 14, 15

CHARACTERISTIC	SYMBOL	3 MHz TIMING MIN.	TYP.	MAX.	4 MHz TIMING (1) MIN.	TYP.	MAX.	UNITS
Cycle Time	T_{CYC}	333	—	—	250	—	—	ns
Clock Pulse Width Ø1 (Measured at V_{CC}-0.2v) Ø2	PWH Ø1 PWH Ø2	150 160	—	—	120 125	—	—	ns
Fall Time, Rise Time (Measured from 0.2v to V_{CC}-0.2v)	T_F, T_R	—	—	15	—	—	15	ns
Delay Time between Clocks (Measured at 0.2v)	T_D	0	—	—	0	—	—	ns

READ/WRITE TIMING (LOAD = ITTL)

CHARACTERISTIC	SYMBOL	3 MHz TIMING MIN.	TYP.	MAX.	4 MHz TIMING (1) MIN.	TYP.	MAX.	UNITS
Read/Write Setup Time from 6500	T_{RWS}	—	80	110	—	80	85	ns
Address Setup Time from 6500	T_{ADS}	—	80	125	—	80	85	ns
Memory Read Access Time	T_{ACC}	—	—	170	—	—	115	ns
Data Stability Time Period	T_{DSU}	50	—	—	40	—	—	ns
Data Hold Time — Read	T_{HR}	10	—	—	5	—	—	ns
Data Hold Time — Write	T_{HW}	10	—	—	10	—	—	ns
Data Setup Time from 6500	T_{MDS}	—	70	100	—	70	90	ns
S.O. Setup Time	$T_{S.O.}$	50	—	—	40	—	—	ns
SYNC Setup Time from 6500	T_{SYNC}	—	—	120	—	—	100	ns
Address Hold Time	T_{HA}	10	30	—	10	30	—	ns
R/W Hold Time	T_{HRW}	10	30	—	10	30	—	ns
RDY Setup Time	T_{RDY}	—	—	15	—	—	15	ns

(1) 4 MHz timing for 6503-6515 is preliminary.

COMMON CHARACTERISTICS

6500 SIGNAL DESCRIPTION

Clocks ($\emptyset_1$, $\emptyset_2$)
The 651X requires a two phase non-overlapping clock that runs at the Vcc voltage level. The 650X clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled.

Address Bus (A_0-A_{15})
These outputs are TTL compatible, capable of driving one standard TTL load and 130 pf.

Data Bus (D_0-D_7)
Eight pins are used for the data bus. This is a bi-directional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130 pf.

Data Bus Enable(DBE)
This TTL compatible input allows external control of the tri-state data output buffers and will enabel the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two ($\emptyset_2$) clock, thus allowing data output from microprocessor only during $\emptyset_2$. During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low.

Ready (RDY)
This input signal allows the user to single cycle the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one ($\emptyset_1$) and up to 100ns after phase two ($\emptyset_2$) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two ($\emptyset_2$) in which the Ready signal is low. This feature allows microprocessor interfacing with low speed PROMS as well as fast (max. 2 cycle) Direct Memory Access (DMA). If Ready is low during a write cycle, it is ignored until the following read operation.

Interrupt Request ($\overline{IRQ}$)
This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3K external resistor should be used for proper wire-OR operation.

Non-Maskable Interrupt ($\overline{NMI}$)
A negative going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor. $\overline{NMI}$ is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for $\overline{IRQ}$ will be performed, regardless of the interrupt mask flag status. The vector address loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ also requires an external 3K register to Vcc for proper wire-OR operations.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupt lines that are sampled during $\emptyset_2$ (phase 2) and will begin the appropriate interrupt routine on the $\emptyset_1$ (phase 1) following the completion of the current instruction.

Set Overflow Flag (S.O.)
A NEGATIVE going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of $\emptyset_1$.

SYNC
This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during $\emptyset_1$ of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the $\emptyset_1$ clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

Reset
This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control. After Vcc reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W and (SYNC) signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

ADDRESSING MODES

ACCUMULATOR ADDRESSING — This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING — In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING — In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

ZERO PAGE ADDRESSING — The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING — (X, Y indexing) — This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

INDEX ABSOLUTE ADDRESSING — (X, Y indexing) — This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X and Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING — In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING — Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is — 128 to + 127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING — In indexed indirect addressing (referred to as [Indirect, X]), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING — In indirect indexed addressing (referred to as [Indirect, Y]), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

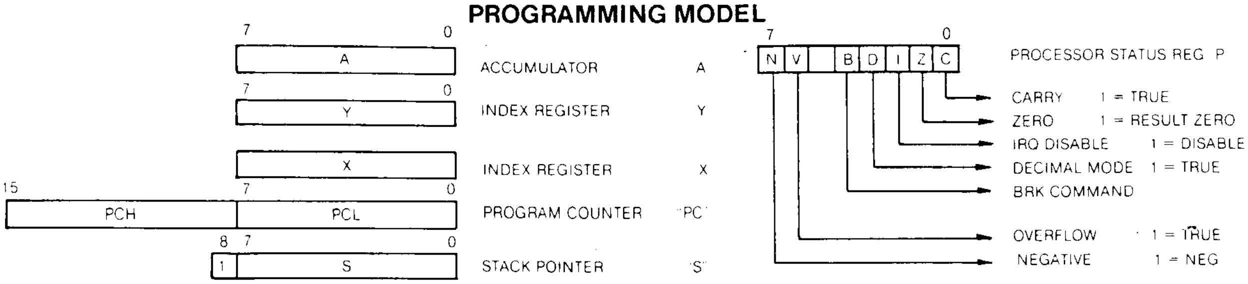
ABSOLUTE INDIRECT — The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

INSTRUCTION SET — ALPHABETIC SEQUENCE

ADS	Add Memory to Accumulator with Carry
AND	"AND" Memory with Accumulator
ASL	Shift left One Bit (Memory or Accumulator)
BCC	Branch on Carry Clear
BCS	Branch on Carry Set
BEQ	Branch on Result Zero
BIT	Test Bits in Memory with Accumulator
BMI	Branch on Result Minus
BNE	Branch on Result not Zero
BPL	Branch on Result Plus
BRK	Force Break
BVC	Branch on Overflow Clear
BVS	Branch on Overflow Set
CLC	Clear Carry Flag
CLD	Clear Decimal Mode
CLI	Clear Interrupt Disable Bit
CLV	Clear Overflow Flag
CMP	Compare Memory and Accumulator
CPX	Compare Memory and Index X
CPY	Compare Memory and Index Y
DEC	Decrement Memory by One
DEX	Decrement Index X by One
DEY	Decrement Index Y by One
EOR	"Exclusive or" Memory with Accumulator
INC	Increment Memory by One
INX	Increment Index X by One
INY	Increment Index Y by One
JMP	Jump to New Location
JSR	Jump to New Location Saving Return Address
LDA	Load Accumulator with Memory
LDX	Load Index X with Memory
LDY	Load Index Y with Memory
LSR	Shift One Bit Right (Memory or Accumulator)
NOP	No Operation
ORA	"OR" Memory with Accumulator
PHA	Push Accumulator on Stack
PHP	Push Processor Status on Stack
PLA	Pull Accumulator from Stack
PLP	Pull Processor Status from Stack
ROL	Rotate One Bit Left (Memory or Accumulator)
ROR	Rotate One Bit Right (Memory or Accumulator)
RTI	Return from Interrupt
RTS	Return from Subroutine
SBC	Subtract Memory from Accumulator with Borrow
SEC	Set Carry Flag
SED	Set Decimal Mode
SEI	Set Interrupt Disable Status
STA	Store Accumulator in Memory
STX	Store Index X in Memory
STY	Store Index Y in Memory
TAX	Transfer Accumulator to Index X
TAY	Transfer Accumulator to Index Y
TSX	Transfer Stack Pointer to Index X
TXA	Transfer Index X to Accumulator
TXS	Transfer Index X to Stack Register
TYA	Transfer Index Y to Accumulator

COMMON CHARACTERISTICS

PROGRAMMING MODEL



INSTRUCTION SET—OP CODES, Execution Time, Memory Requirements

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND. X)			(IND). Y			Z. PAGE. X			ABS. X			ABS. Y			RELATIVE			INDIRECT			Z. PAGE. Y			CONDITION CODES
MNEMONIC	OPERATION	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	N Z C I D V
ADC	A + M + C → A (4)(1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										• • • — — •
AND	A ∧ M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										• • — — — —
ASL	C ← [7 0] ← 0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													• • • — — —
BCC	BRANCH ON C = 0 (2)																															90	2	2							— — — — — —
BCS	BRANCH ON C = 1 (2)																															B0	2	2							— — — — — —
BEQ	BRANCH ON Z = 1 (2)																															F0	2	2							— — — — — —
BIT	A ∧ M				2C	4	3	24	3	2																															M_7 • — — — M_6
BMI	BRANCH ON N = 1 (2)																															30	2	2							— — — — — —
BNE	BRANCH ON Z = 0 (2)																															D0	2	2							— — — — — —
BPL	BRANCH ON N = 0 (2)																															10	2	2							— — — — — —
BRK														00	7	1																									— — — 1 — —
BVC	BRANCH ON V = 0 (2)																															50	2	2							— — — — — —
BVS	BRANCH ON V = 1 (2)																															70	2	2							— — — — — —
CLC	0 → C													18	2	1																									— — 0 — — —
CLD	0 → D													D8	2	1																									— — — — 0 —
CLI	0 → I													58	2	1																									— — — 0 — —
CLV	0 → V													B8	2	1																									— — — — — 0
CMP	A − M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										• • • — — —
CPX	X − M	E0	2	2	EC	4	3	E4	3	2																															• • • — — —
CPY	Y − M	C0	2	2	CC	4	3	C4	3	2																															• • • — — —
DEC	M − 1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													• • — — — —
DEX	X − 1 → X													CA	2	1																									• • — — — —
DEY	Y − 1 → Y													88	2	1																									• • — — — —
EOR	A ⊻ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										• • — — — —
INC	M + 1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													• • — — — —
INX	X + 1 → X													E8	2	1																									• • — — — —
INY	Y + 1 → Y													C8	2	1																									• • — — — —
JMP	JUMP TO NEW LOC				4C	3	3																												6C	5	3				— — — — — —
JSR	JUMP SUB				20	6	3																																		— — — — — —
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										• • — — — —

		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM			IMPLIED			(IND. X)			(IND). Y			Z. PAGE. X			ABS. X			ABS. Y			RELATIVE			INDIRECT			Z. PAGE. Y			CONDITION CODES
MNEMONIC	OPERATION	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	N Z C I D V
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2	• • — — — —
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3													• • — — — —
LSR	0 → [7 0] → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0 • • — — —
NOP	NO OPERATION													EA	2	1																									— — — — — —
ORA	A ∨ M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										• • — — — —
PHA	A → M_s S − 1 → S													48	3	1																									— — — — — —
PHP	P → M_s S − 1 → S													08	3	1																									— — — — — —
PLA	S + 1 → S M_s → A													68	4	1																									• • — — — —
PLP	S + 1 → S M_s → P													28	4	1																									(RESTORED)
ROL	← [7 0] ← [C] ←				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													• • • — — —
ROR	→ [C] → [7 0] →				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3													• • • — — —
RTI	RTRN INT													40	6	1																									(RESTORED)
RTS	RTRN SUB													60	6	1																									— — — — — —
SBC	A − M − C̄ → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										• • (3) — — •
SEC	1 → C													38	2	1																									— — 1 — — —
SED	1 → D													F8	2	1																									— — — — 1 —
SEI	1 → I													78	2	1																									— — — 1 — —
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										— — — — — —
STX	X → M				8E	4	3	86	3	2																												96	4	2	— — — — — —
STY	Y → M				8C	4	3	84	3	2													94	4	2																— — — — — —
TAX	A → X													AA	2	1																									• • — — — —
TAY	A → Y													A8	2	1																									• • — — — —
TSX	S → X													BA	2	1																									• • — — — —
TXA	X → A													8A	2	1																									• • — — — —
TXS	X → S													9A	2	1																									— — — — — —
TYA	Y → A													98	2	1																									• • — — — —

(1) ADD 1 TO "N" IF PAGE BOUNDRY IS CROSSED
(2) ADD 1 TO "N" IF BRANCH OCCURS TO SAME PAGE
ADD 2 TO "N" IF BRANCH OCCURS TO DIFFERENT PAGE
(3) CARRY NOT—BORROW
(4) IF IN DECIMAL MODE Z FLAG IS INVALID
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

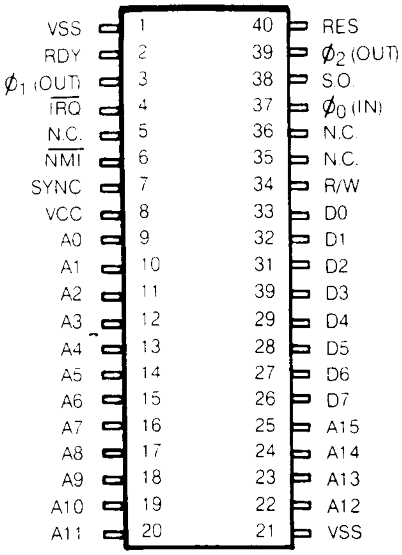
X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
M_s MEMORY PER STACK POINTER

\+ ADD
− SUBTRACT
∧ AND
∨ OR

⊻ EXCLUSIVE OR
• MODIFIED
— NOT MODIFIED
M_7 MEMORY BIT 7
M_6 MEMORY BIT 6

N NO CYCLES
\# NO BYTES

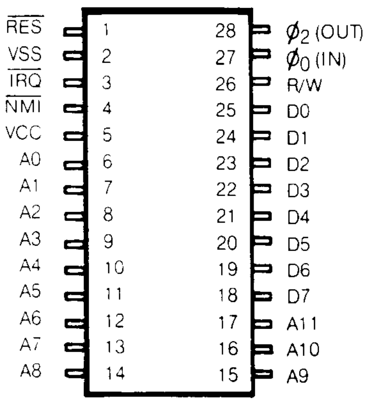
Note: Commodore Semiconductor Group cannot assume liability for the use of undefined OP Codes



6502—40 Pin Package

Features of 6502

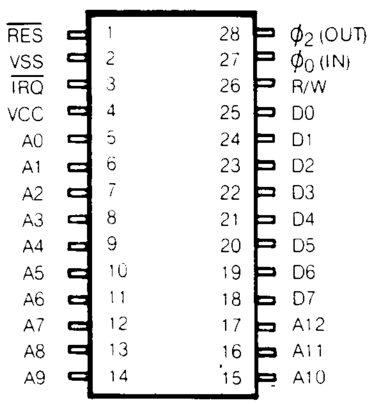
- 65K Addressable Bytes of Memory (A0-A15)
- $\overline{IRQ}$ Interrupt
- On-the-chip Clock
  TTL Level Single Phase Input
  RC Time Base Input
  Crystal Time Base Input
- SYNC Signal
  (can be used for single instruction execution)
- RDY Signal
  (can be used to halt or single cycle execution)
- Two Phase Output Clock for Timing of Support Chips
- $\overline{NMI}$ Interrupt



6503—28 Pin Package

Features of 6503

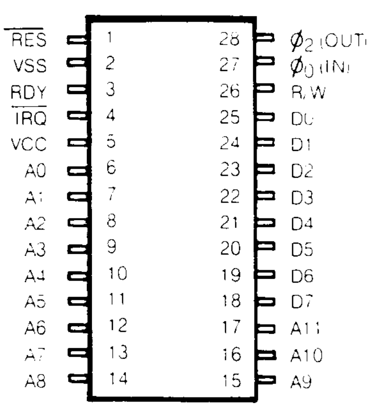
- 4K Addressable Bytes of Memory (A0-A11)
- On-the-chip Clock
- $\overline{IRQ}$ Interrupt
- $\overline{NMI}$ Interrupt
- 8 Bit Bidirectional Data Bus



6504—28 Pin Package

Features of 6504

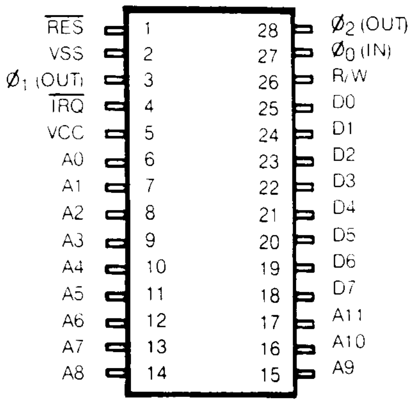
- 8K Addressable Bytes of Memory (A0-A12)
- On-the-chip Clock
- $\overline{IRQ}$ Interrupt
- 8 Bit Bidirectional Data Bus



6505—28 pin Package

Features of 6505

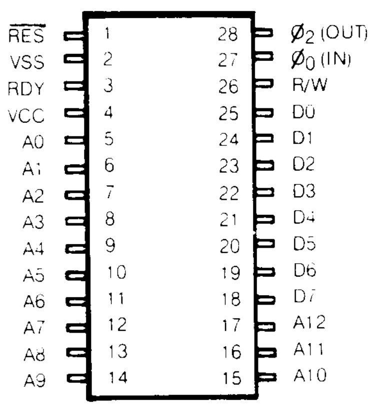
- 4K Addressable Bytes of Memory (A0-A11)
- On-the-chip Clock
- $\overline{IRQ}$ Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus



6506—28 Pin Package

Features of 6506

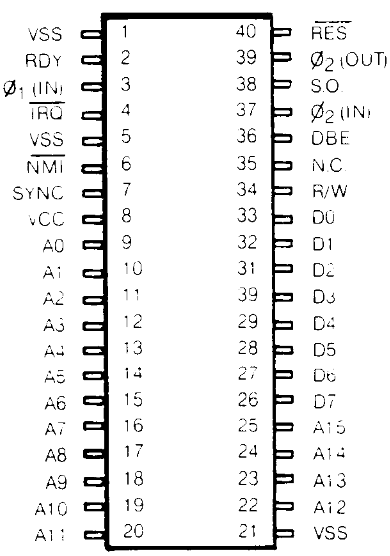
- 4K Addressable Bytes of Memory (A0-A11)
- On-the-chip Clock
- $\overline{IRQ}$ Interrupt
- Two phase output clock for timing of support chips
- 8 Bit Bidirectional Data Bus



6507—28 Pin Package

Features of 6507

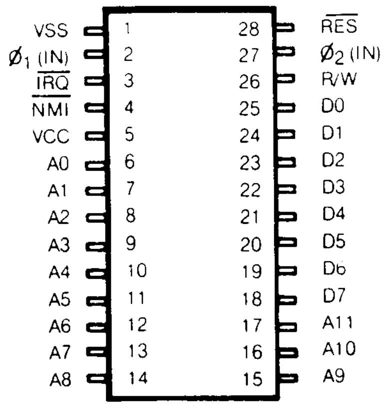
- 8K Addressable Bytes of Memory (A0-A12)
- On-the-chip Clock
- RDY Signal
- 8 Bit Bidirectional Data Bus



6512—40 Pin Package

Features of 6512

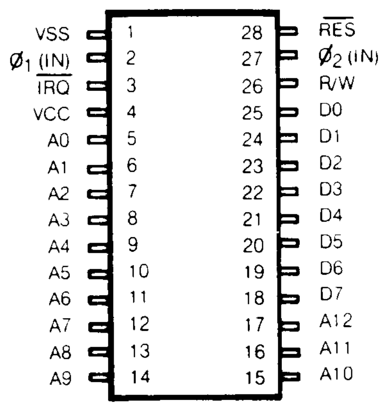
- 65K Addressable Bytes of Memory (A0-A15)
- $\overline{IRQ}$ Interrupt
- $\overline{NMI}$ Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus
- SYNC Signal
- Two phase clock input
- Data Bus Enable



6513—28 Pin Package

Features of 6513

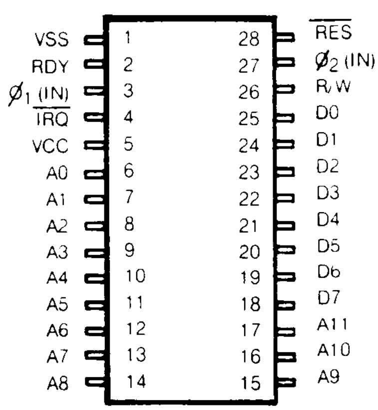
- 4K Addressable Bytes of Memory (A0-A11)
- Two phase clock input
- IRQ Interrupt
- NMI Interrupt
- 8 Bit Bidirectional Data Bus



6514—28 Pin Package

Features of 6514

- 8K Addressable Bytes of Memory (A0-A12)
- Two phase clock input
- IRQ Interrupt
- 8 Bit Bidirectional Data Bus



6515—28 Pin Package

Features of 6515

- 4K Addressable Bytes of Memory (A0-A11)
- Two phase clock input
- IRQ Interrupt
- RDY Signal
- 8 Bit Bidirectional Data Bus