CHAPTER 3
INTERFACE

3.1 GENERAL

The flexibility achieved with the address select logic and the eight-position address select switch permits the RK05 Disk Drive to be connected to a variety of computer systems. In the RK11-C and RK8/E systems, up to four drives can be serially connected to a single bus; in the RK11-D system, up to eight drives can be serially connected.

Interface cable connection of the RK05 Disk Drive is made to card position 7 or 8 of the electronic module. These card positions are parallel-wired so that several drives may be daisy-chained in a multidrive configuration; that is, card position 7 or 8 of the first drive is connected to card position 7 or 8 of the succeeding drive, etc. (By convention, card position 7 is used for input signals; card position 8 is used for output signals.) If there is only one drive in the system, an M930 terminator card must be installed in the unused interface card position; if there is more than one drive in the system, only the last drive on the bus must have the M930 terminator card in the unused interface card position. The interface signal levels are determined by the M930 terminator card. An assertion, or logic 1, is approximately +0.5 Vdc, and a negation, or logic 0, is approximately +3.5 Vdc.

Figure 3-1 illustrates and the following paragraphs describe the function of each interface line. The signals listed, being bus signals, operate according to negative logic; they are asserted low. Appendix A contains a glossary of RK05 backplane connections.

3.2 INPUT INTERFACE LINES

3.2.1 RK11-D

This line (BUS RK11-D L) transmits a signal that configures the address select logic to operate with a particular controller type. A logical 0 on this line indicates that the controller is not an RK11-D (thus, the controller is either an RK11-C or an RK8/E, both of which control only four drives on a single bus), while a logical 1 indicates that the controller is an RK11-D.

3.2.2 Select (4 lines)

BUS SEL DR 0/A/E, 1/B/F, 2/C/H, and 3/D/J L operate in conjunction with the RK11-D interface line and an eight-position address select switch on the M7700 card to determine the drive address assignment and selection by one of the following two methods:

a. With a logical 0 on the RK11-D line, the M7700 selection circuit is configured to decode the four selection lines as a linear set. In a particular drive, only one of the four lines is internally connected (via positions 0 through 3 of the address select switch) to the drive control logic. To select a drive, the controller places a logical 1 on the desired select line. This line remains at logical 1 throughout the entire data transfer or control operation.

b. With a logical 1 on the RK11-D line, the M7700 selection is configured to decode the four selection lines as a binary-encoded set. To select a drive, the controller places a 3-bit binary code, which corresponds to the drive address, on these select lines. This binary code is then translated by a three-line-to-eight-line decoder to activate only one of the eight address select switch positions.

3.2.3 Cylinder Address (8 lines)

BUS CYL ADD 0 L through BUS CYL ADD 7 L determine the cylinder position of the read/write heads. In order to move the heads to a desired cylinder, the controller places a corresponding 8-bit binary code on the lines (valid codes=0 through 202_{10}). These lines are gated by the Strobe signal to position the heads at the selected cylinder. The binary code remains on the lines until either the Address Acknowledged or the Address Invalid signal is returned from the drive (Paragraph 3.3.3).

3.2.4 Strobe

BUS STROBE L transmits a signal that gates the Cylinder Address or Restore line. The controller places a logical 1 on the Strobe line, only after the Cylinder Address or the Restore signals are fully settled on their respective lines.

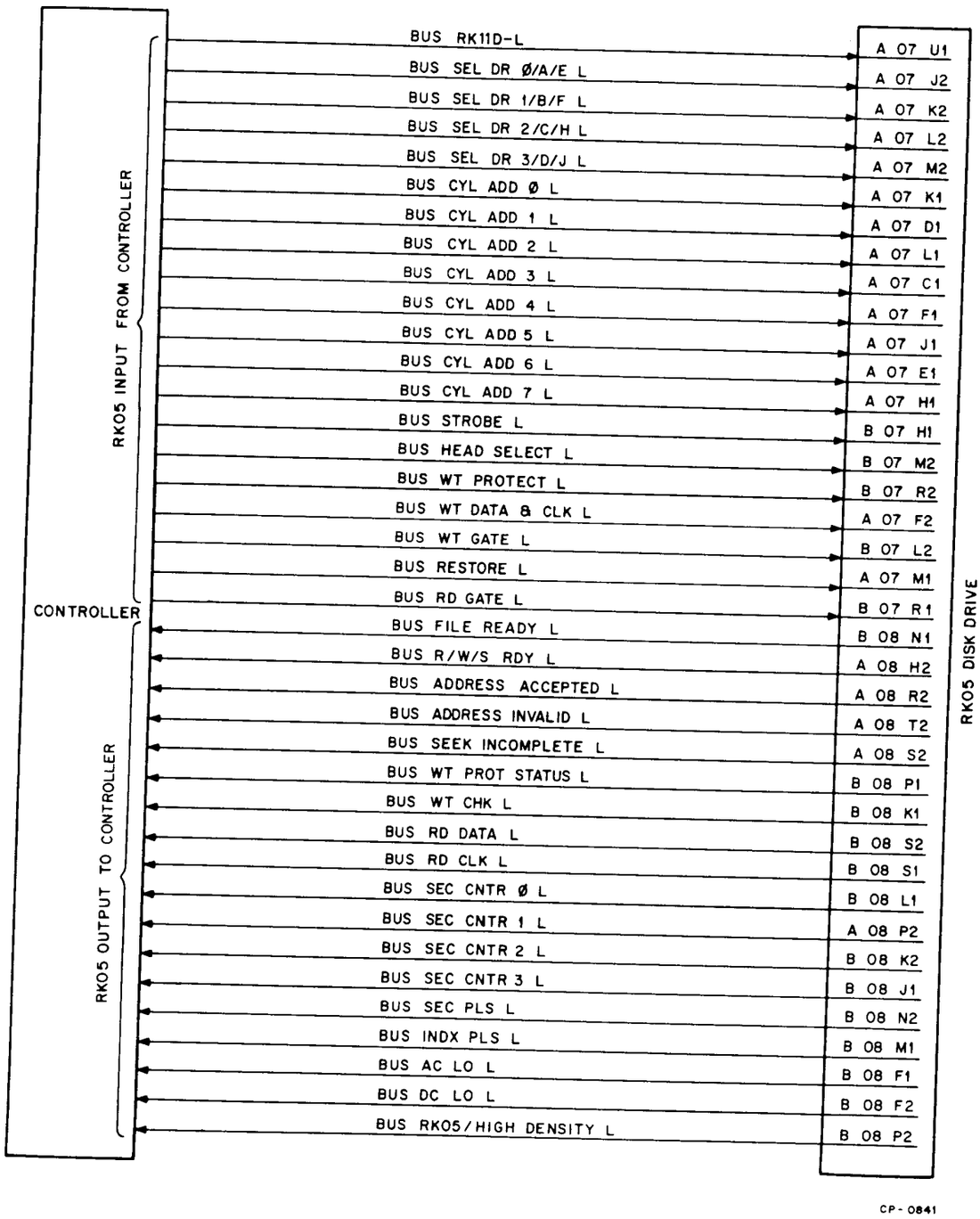

Figure 3-1 Controller/RK05 Disk Drive Interface Lines and Pin Assignments

The Strobe line remains at logical 1 until either the Address Acknowledged or the Address Invalid signal is returned from the drive.

3.2.5 Head Select

BUS SEL UPPER HD L transmits a signal that determines which of the two read/write heads is to be selected. The controller places a logical 1 on this line to select the upper head, and a logical 0 to select the lower head. Either signal remains on the line throughout the entire read or write operation.

3.2.6 Write Protect Set

BUS WT PROTECT L transmits a signal that disables the drive write amplifiers to prevent a write operation. The controller places a logical 1 on this line to set the Write Protect flip-flop and inhibit the write capability of the drive. The Write Protect flip-flop is also set if the WT PROT indicator is off and the operator presses the WT PROT switch (Paragraph 1.4.1).

3.2.7 Write Data and Clock

BUS WT DATA & CLK L transmits multiplexed data and clock pulses to the disk drive.

3.2.8 Write Gate

BUS WT GATE L transmits a signal to simultaneously turn on both the write and erase current in the selected write head. The controller places a logical 1 on this line 1 μs prior to transmitting the write data. This line remains at logical 1 throughout the data transmission time.

3.2.9 Restore (RTZ)

BUS RESTORE L transmits a signal to position the read/write heads at cylinder zero. The controller places a logical 1 on this line prior to issuing the Strobe (BUS STROBE L) signal. About 2 μs after this signal is issued, the drive returns an Address Acknowledged signal, clears the address register, and moves the heads to cylinder zero. The Restore line remains at logical 1 until the Address Acknowledged signal is received by the controller.

3.2.10 Read Gate

BUS RD GATE L transmits a signal that allows data to be read from the drive. The controller places a logical 1 on this line to enable the Read Clock and Read Data output lines. This line remains at logical 1 throughout the entire read operation.

3.3 OUTPUT INTERFACE LINES

3.3.1 File Ready (Drive Ready)

BUS FILE RDY L transmits a logical 1 to indicate the following conditions:

a. Drive operating power is correct.

b. A disk cartridge is properly loaded.

c. The drive front door is closed.

d. RUN/LOAD switch is in the RUN position.

e. Spindle is rotating at the correct speed.

f. Read/write heads are loaded.

g. Write Check is false.

3.3.2 Read, Write, or Seek Ready/On Cylinder

BUS R/W/S RDY L transmits a logical 1 to indicate that the drive is in the File Ready condition (Paragraph 3.3.1) and is not performing a seek operation.

3.3.3 Address Accepted

BUS ADDRESS ACCEPTED L transmits a 5-μs negative pulse to indicate that the drive has accepted a Seek command with a valid address and the command execution has begun. The negative pulse is generated about 2 μs after receipt of the Strobe signal, even if there is no change from the present address.

3.3.4 Address Invalid (Logic Address Interlock)

BUS LOG ADD INT L transmits a 5-μs negative pulse to indicate that the drive has received a nonexecutable Seek command with a cylinder address greater than 202. For this case, the Seek command is suppressed in the drive and the heads are not moved. The pulse generation time is the same as for the Address Acknowledged signal.

3.3.5 Seek Incomplete

BUS SIN L transmits a logical 1 to indicate that some malfunction in the drive did not allow the seek operation to be completed. This line remains low until a Restore command is received or the operator sets the RUN/LOAD switch to LOAD and then back to RUN.

3.3.6 Write Protect Status

BUS WT PROT STATUS L transmits a logical 1 to indicate that the write capability of the drive is inhibited (write protected). When this line is at logical 1, the WT PROT indicator on the drive control panel lights (Paragraph 1.4.1).

3.3.7 Write Check

BUS WT CHK L transmits a logical 1 to indicate the following conditions:

a. Erase or write current without a WRITE GATE.

b. Inoperative linear positioner transducer lamp.

When the Write Check signal is at a logical 1, all external commands to the drive are suppressed and the FAULT indicator on the drive control panel lights. If the fault condition is temporary, the operator may turn off the FAULT indicator by pressing the WT PROT switch. This

action, however, causes the WT PROT indicator to light; the WT PROT switch must be pressed a second time to turn off the WT PROT indicator (Paragraph 1.4.1).

3.3.8 Read Data

BUS RD DATA transmits read data only (160-ns pulses).

3.3.9 Read Clock

BUS RD CLK L transmits read clock pulses only (160-ns pulses).

3.3.10 Sector Address (4 lines)

BUS SEC CNTR 0 through 3 L indicate which sector is passing under the read/write heads. The sector address is a 4-bit binary code derived from the Sector Address counter.

3.3.11 Sector Pulse

BUS SEC PLS L transmits a 2-μs negative pulse each time a sector slot passes the sector transducer. The index slot (unique slot) is suppressed in this line and is transmitted on a separate Index Pulse line.

3.3.12 Index Pulse

BUS INDX PLS L transmits a single 2-μs negative pulse for each revolution of the disk. The Index Pulse occurs 600 μs after the last sector pulse and is generated each time the index slot (unique slot) is detected by the sector transducer.

3.3.13 AC Low

BUS AC LO L transmits a logical 1 when there is a loss (for more than 45 ms) of the 30 Vac within the drive. When AC Low occurs, the drive finishes reading/writing the current sector, then initiates a normal head-retract and unload cycle. If a total power loss occurs before the heads are completely retracted, the safety relay is de-energized to retract the heads under battery power (emergency retract).

3.3.14 DC Low

BUS DC LO L transmits a logical 1 when the ±15 Vdc within the drive drops to 12 Vdc or below. When DC Low is generated, the safety relay is de-energized to retract the heads under battery power (emergency retract). Since the RUN gate of each drive is connected to the DC Low bus, a DC Low signal from any one drive in a multidrive system disables all the drives in the system.

3.3.15 High Density/RK05 L

BUS RK05 L transmits a logical 1 (indicating high density only) whenever the drive is selected. (All RK05s are high density.)

CHAPTER 4
THEORY OF OPERATION

4.1 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the major areas and associated signals of the RK05 Disk Drive. Together they rotate the recording disk, align the heads at a specified cylinder, and perform the read and write functions.

Paragraphs 4.1.1 through 4.1.5 describe the major operations of the disk drive; Paragraphs 4.2.1 through 4.5 describe the detailed logical sequence of each major operation.

4.1.1 Start

During the start cycle, the control and interlock logic controls the spindle motor operation. To energize the spindle motor, the RUN/LOAD switch must be in the RUN position and the following interlock conditions must be present:

a. Operating power must be applied to all drives.

b. The drive front door must be closed.

c. The disk cartridge must be properly installed.

If these interlock conditions are fulfilled, the spindle motor is energized. After an 8-second delay, to allow the spindle to accelerate to operating speed, the control and interlock logic generates an internal LOAD HEADS signal, which loads the read/write heads and positions them at cylinder zero (Paragraph 4.2.5.1). When the heads are loaded and positioned at cylinder zero, the RDY and ON CYL indicators light, and the BUS FILE RDY and R/W/S RDY/ON CYL interface lines go low.

Figure 4-2 illustrates the logical sequence during the start cycle. Paragraph 4.2.2 contains a detailed description of the preceding sequence.

4.1.2 Stop

The disk drive can enter a stop cycle in three ways:

a. Placing the RUN/LOAD switch to LOAD

b. Losing spindle speed

c. Losing operating power in any drive on the bus.

If any of the preceding conditions occur, the control and interlock logic removes the internal LOAD HEADS signal and brings the BUS FILE RDY interface line high. When LOAD HEADS is removed, the positioner control logic retracts the read/write heads. After the heads are fully retracted, the spindle motor is de-energized and the spindle coasts to a stop (about 30 seconds). When the spindle has stopped rotating, the LOAD indicator lights and the drive front door unlocks.

Figure 4-3 illustrates the logical sequence during the stop cycle. Paragraph 4.2.3 contains a detailed logic description of this sequence.

4.1.3 Track Addressing and Head Positioning

To move the read/write heads from a current location to a new location above the disk (a seek operation), a selected drive must first receive an 8-bit binary cylinder address from the controller. If the new address exceeds cylinder 202, the BUS ADDRESS INVALID L (Logic Address Interlock) interface signal is generated and head motion is suppressed. If the new address does not exceed cylinder 202, the BUS ADDRESS ACCEPTED L interface signal is generated and the new address is compared to the current address. The comparison result (difference) is fed to a positioner servo system to move the heads.

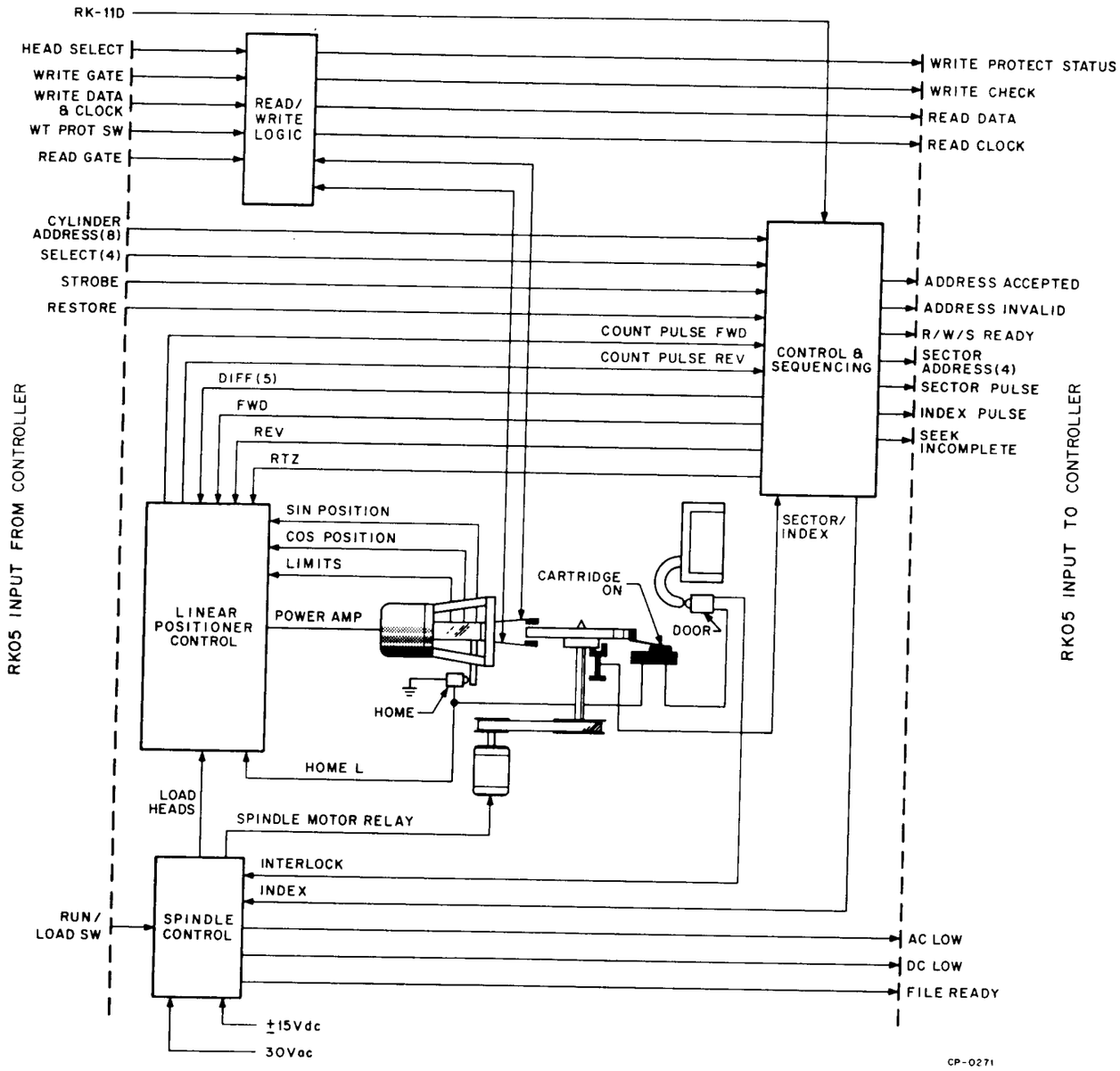

Figure 4-1 Functional Block Diagram

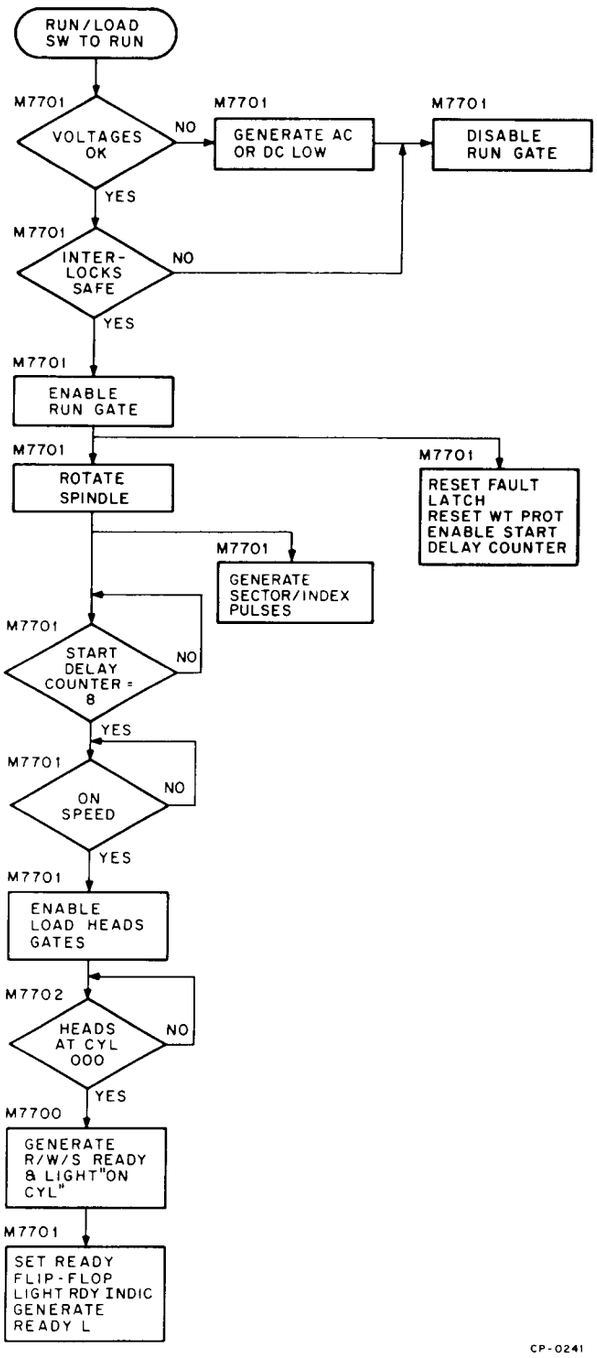

Figure 4-2 Start Flow Chart

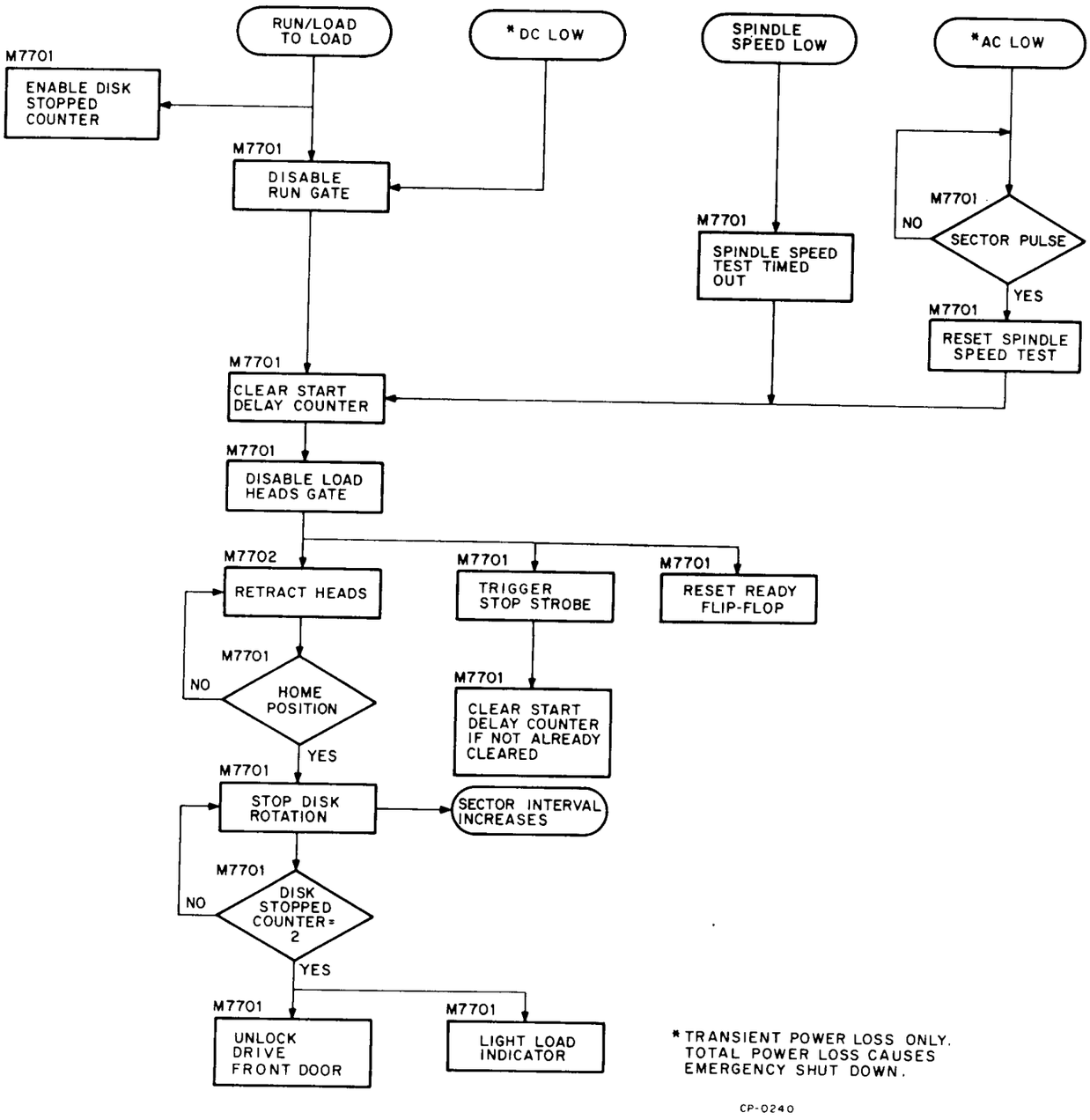

Figure 4-3 Stop Flow Chart

As the heads pass each cylinder, output pulses from the linear positioner transducer trigger a Difference register to control the velocity of head motion (Paragraph 4.3). As the heads approach the destination cylinder, the head positioner decelerates, eventually stopping the heads at the designated cylinder. After a small delay, to allow the heads to settle at the new location, the ON CYL indicator on the control panel lights and the R/W/S READY interface line goes low.

If, at any time during the seek operation, a return-to-zero (Restore) command is received or the heads reach the inner limit of the disk, the seek operation is immediately terminated and the heads are retracted to cylinder zero.

Figures 4-4 and 4-5 illustrate the logical sequence during a seek or return-to-zero operation. Paragraph 4.2.5 contains a detailed logic description of this sequence.

4.1.4 Recording Technique

Each head is a four-terminal, magnetic device containing two coils. A center-tapped coil performs the read or write function, while the other series-connected coil performs the erase function. The head (Figure 4-6) is designed so that the erase coil is electrically connected to the center tap of the read/write coil and is energized (Figure 4-7) whenever a write operation occurs. This head configuration, called "straddle erase", erases most of the residue from previous recording between the .006 in. wide tracks and thus eliminates track "crosstalk" or interference from such recording. During a write operation, current through the write coil automatically overwrites old data.

The RK05 Disk Drive uses a double-frequency, non-return-to-zero (NRZ) method of magnetic recording. In this method, flux reversals (clock pulses) are recorded on the magnetic disk at regularly spaced intervals (Figure 4-8). The time period between these clock pulses is a bit cell, and data storage occurs within these cells. A flux reversal during a bit cell represents a logical 1, while the absence of a flux reversal during a bit cell is a logical 0.

4.2 LOGICAL DESCRIPTION

4.2.1 Power On/Off Sequence

Application of ac power lights the PWR indicator, turns on the blower, energizes the various voltage regulators, and activates the elapsed time indicator. If ac power is removed when the read/write heads are not in the "home" position, the home microswitch applies battery power to the linear motor, retracting the heads to "home".

4.2.2 Start

Figure 4-9 is a block diagram illustrating the control and interlock aspects of the start/stop cycle. Although some logic elements are indicated, this figure is principally intended to simplify the actual gating and signal flow. If any gate-chasing or logic analysis is anticipated, refer to the M7701 circuit schematic.

Placing the RUN/LOAD switch on the front control panel in the RUN position enables the Run gate, provided that:

a. A disk cartridge has been properly installed.

b. The drive front door is closed and locked.

c. The +15 and -15 Vdc are above 12 Vdc and the +5 Vdc is above 4.6 Vdc (Paragraph 4.2.3.4).

With the Run gate enabled, the spindle motor latch is set to energize the spindle motor relay and initiate disk rotation. At the same time, the Start Delay counter begins to count pulses (at a rate of one pulse per second) from the Slow Clock. When a count of eight (8 seconds) is reached, a feedback output from the counter prevents it from incrementing further. By this time, if the spindle has accelerated to the correct operational speed (Paragraph 4.2.3.2), the set output from the On Speed flip-flop is ANDed with the Start Delay counter output to enable the Load Heads gate and produce the LOAD HEADS signal. This signal enables the D input of the Ready flip-flop, and also allows the positioner to move the read/write heads to cylinder zero (Paragraph 4.2.5.1). Once the heads are positioned and settled at cylinder zero, the signal R/W/S READY is produced, lighting the ON CYL indicator (M7700) and clocking the Ready flip-flop set. When the Ready flip-flop sets, the BUS FILE RDY interface signal is produced and the RDY indicator on the control panel lights. The drive is then ready to perform a seek, read, or write operation.

4.2.3 Stop

The following paragraphs describe the ways that the disk drive can enter a stop cycle. Figure 4-9 illustrates some of the logic elements used in a start/stop cycle. These logic elements are located on the M7701 card.

4.2.3.1 Normal Stop – Placing the RUN/LOAD switch in the LOAD position enables the Disk Stopped counter and disables the Run gate, causing RUN L to come high. Once enabled, the Disk Stopped counter begins to increment; however, it is reset repetitively by every SECTOR/INDEX pulse before it reaches a count of two. This counter reset technique keeps the door unlocking solenoid de-energized to prevent the operator from opening the drive front door before the disk has come to a complete halt.

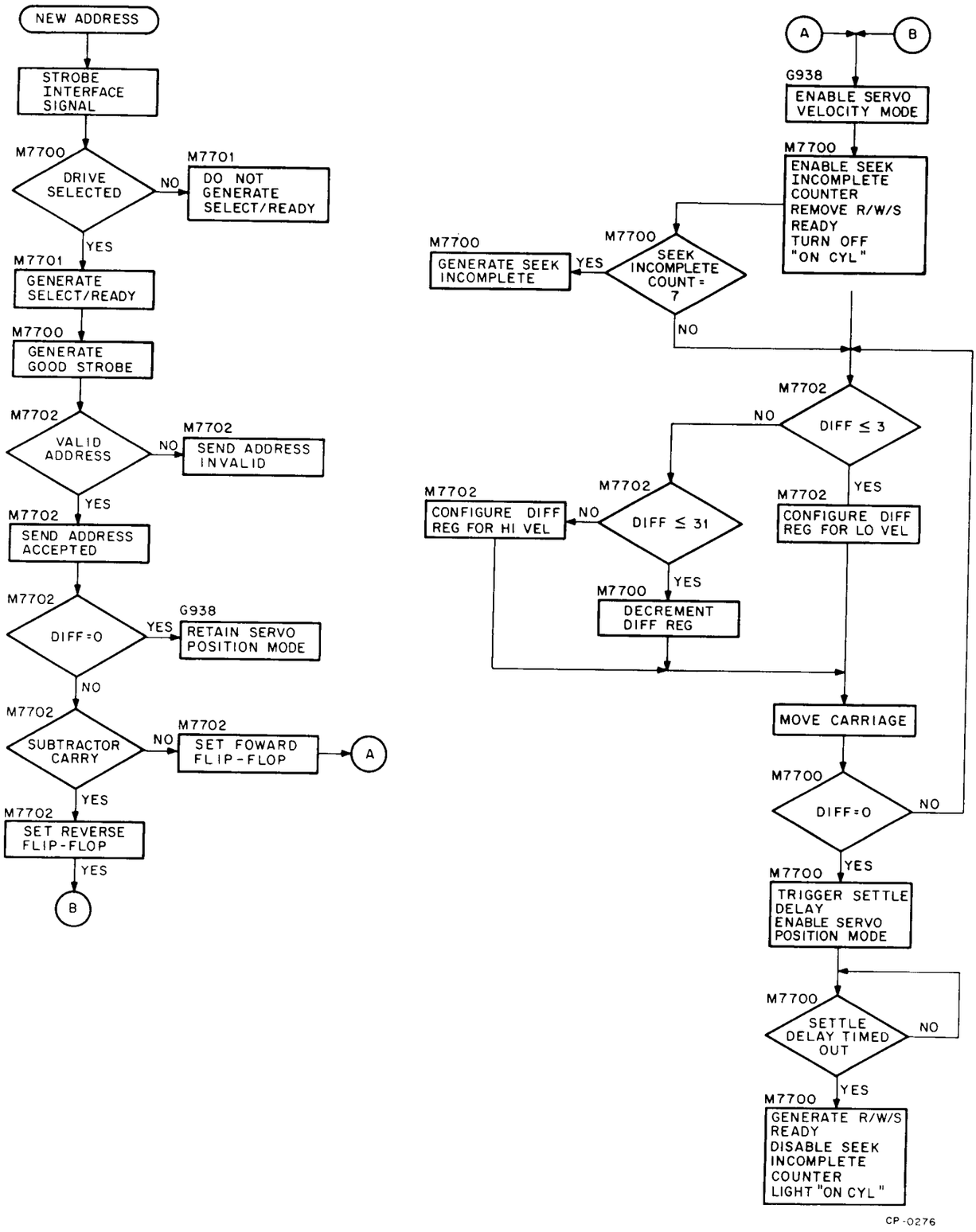

Figure 4-4 Seek Flow Chart

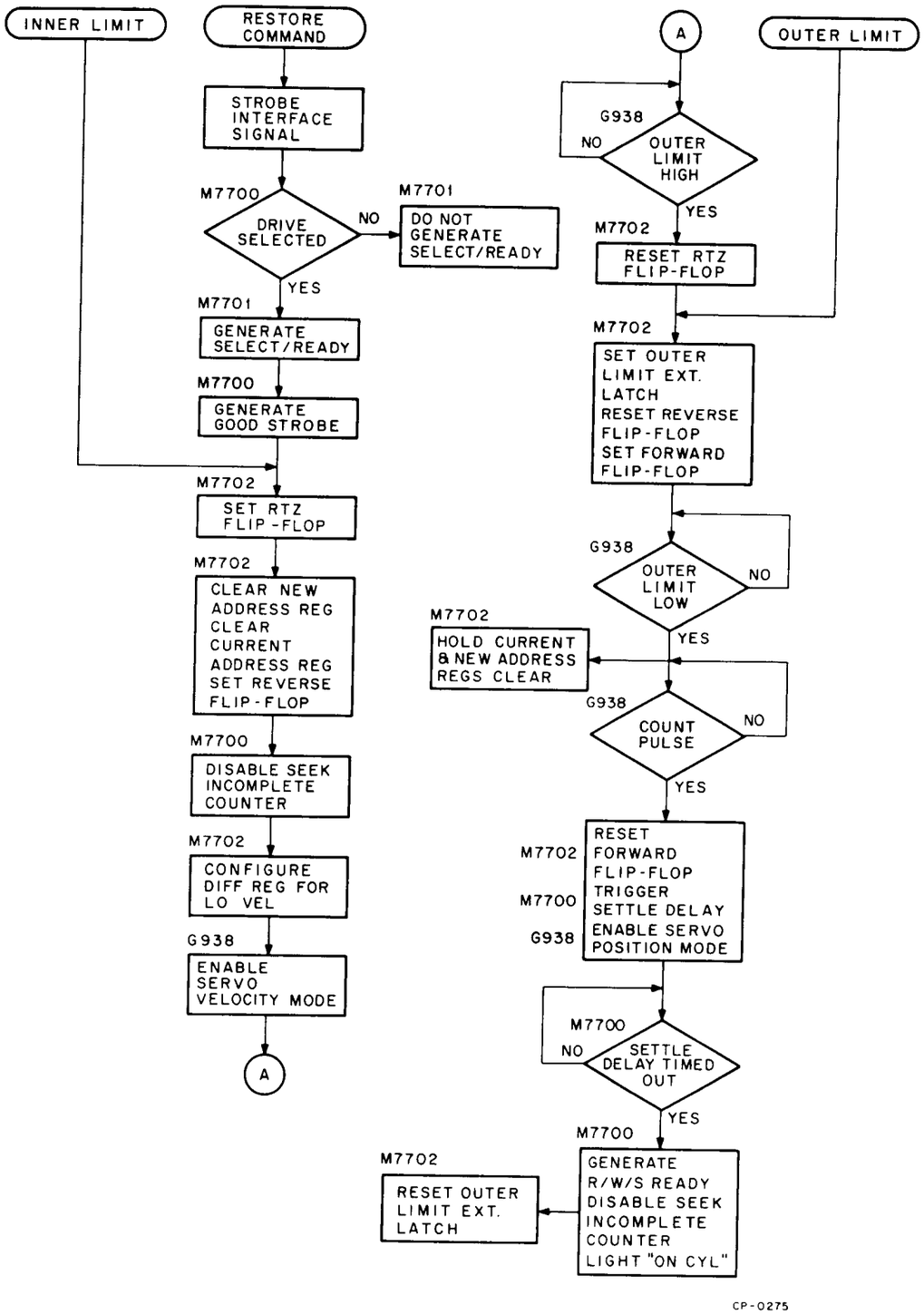

Figure 4-5 Return-to-Zero (Restore) Flow Chart

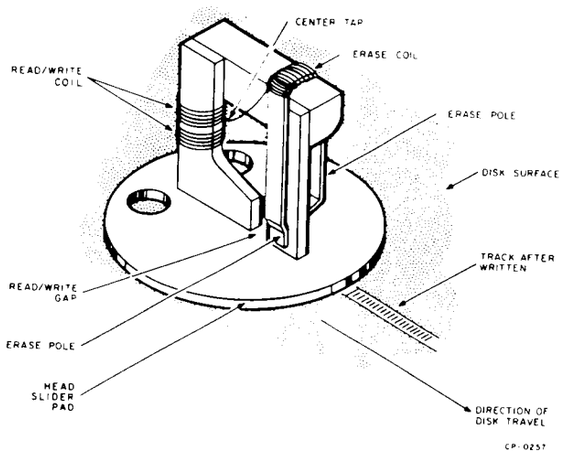

Figure 4-6 Read/Write Head

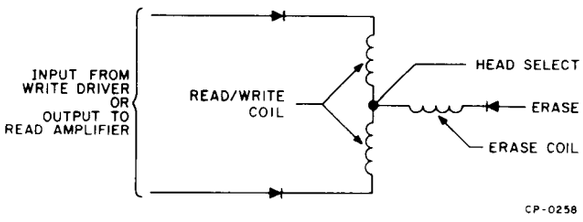

Figure 4-7 Simplified Read/Write Head Circuit

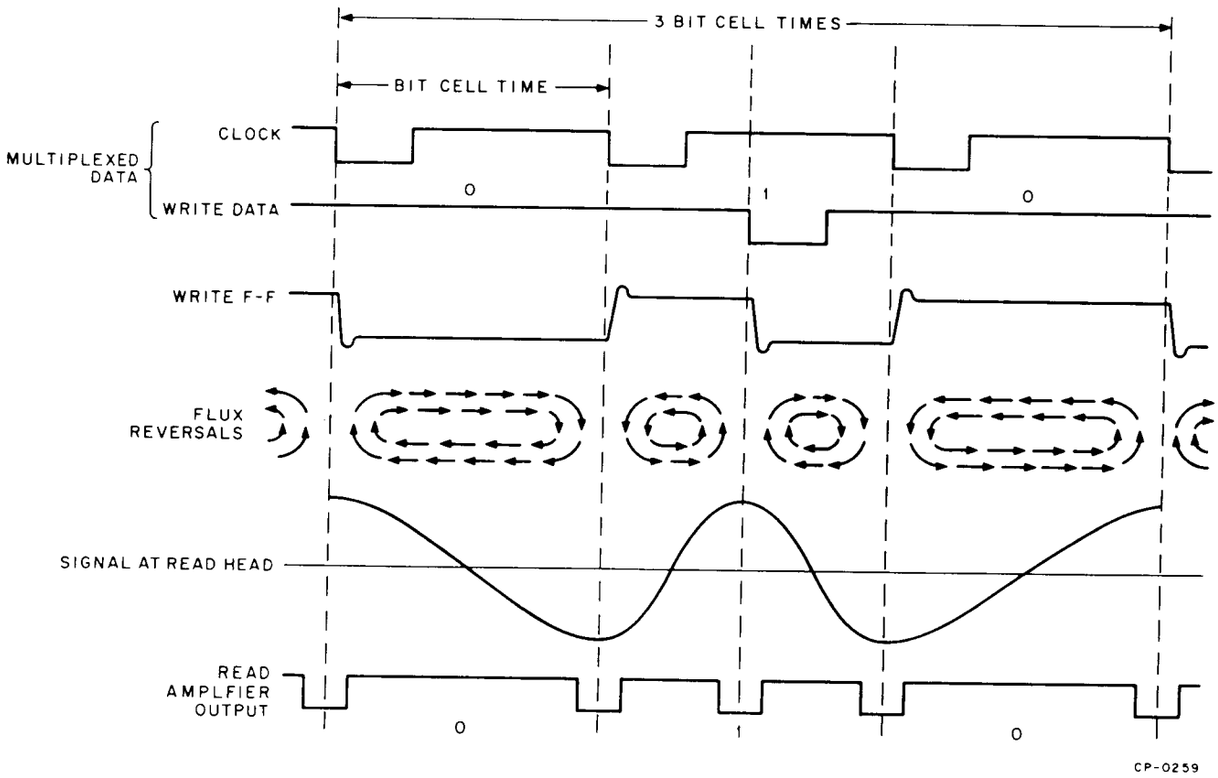

Figure 4-8 Double Frequency Pulse Relationship

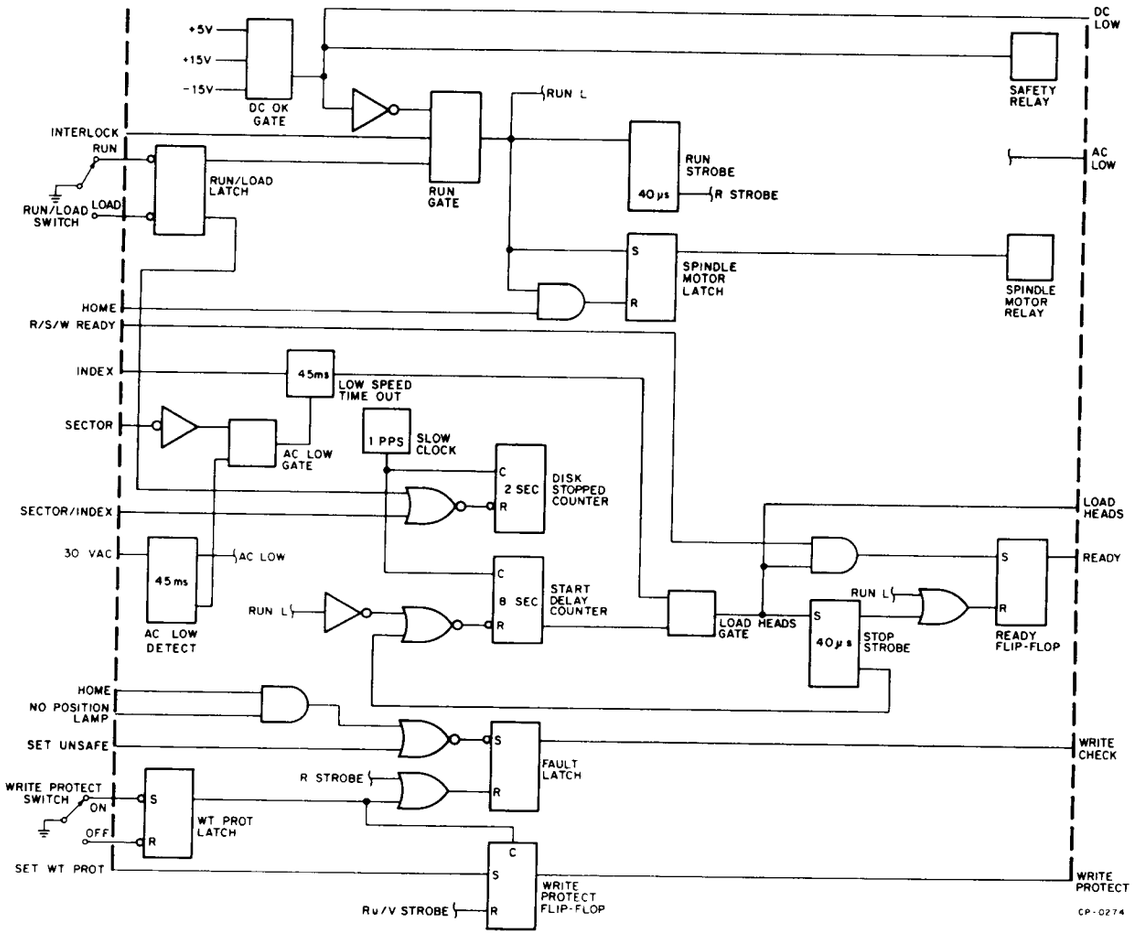

Figure 4-9 Control and Interlock Block Diagram

RUN L high clears the Start Delay counter, disabling the Load Heads gate and thus removing the LOAD HEADS signal. (Once cleared, the Start Delay counter must again increment to eight before the LOAD HEADS signal can be regenerated. This practice allows the heads to fully retract (unload) before they can be loaded again.) Removal of the LOAD HEADS signal resets the Ready flip-flop and also allows the positioner to retract the read/write heads (Paragraph 4.2.5.3). When the heads have fully retracted, the home microswitch closes to generate the HOME L signal. HOME L resets the Spindle Motor latch, de-energizing the spindle motor and allowing the spindle to coast to a stop.

As the spindle decelerates, SECTOR/INDEX pulses occur at a slower rate. Approximately 30 seconds after the Disk Stopped counter is enabled, the disk stops rotating, SECTOR/INDEX pulses cease, and the Disk Stopped counter is incremented by two pulses from the Slow Clock. When the counter reaches two (2 seconds from receipt of the last SECTOR/INDEX pulse), a feedback output from the counter prevents it from incrementing further, while the counter set output energizes the door unlocking solenoid and lights the LOAD indicator on the control panel. The drive front door can now be opened and the cartridge removed.

4.2.3.2 Low Speed Stop – When the disk is rotating at normal speed (1500 rpm), INDEX pulses are generated every 40 ms to trigger the 41–49 ms Low Speed Time Out one-shot. The one-shot output is applied to an associated On Speed flip-flop. As long as the spindle rotation remains above an unsafe speed, successive INDEX pulses keep the On Speed flip-flop set, thus maintaining the LOAD HEADS

signal. If the spindle speed drops below approximately 1200 rpm, the INDEX pulse interval increases beyond 50 ms. If this occurs, the Low Speed Time Out one-shot expires and resets the On Speed flip-flop. With the flip-flop reset, the LOAD HEADS signal is removed, causing the positioner to retract the read/write heads (Paragraph 4.2.5.3). When LOAD HEADS is removed, the 40 μs Stop Strobe one-shot triggers, clearing the Start Delay counter. Once cleared, the Start Delay counter must again increment to eight before the LOAD HEADS signal can be regenerated. This practice allows the heads to fully retract (unload) before they can be loaded again.

The remainder of the low-speed stop cycle is the same as a normal stop (Paragraph 4.2.3.1).

4.2.3.3 AC Low Stop – During normal operation, the 45-ms AC Low Detect one-shot is repeatedly triggered set by the presence of 30 Vac. If this voltage is removed for more than 45 ms, the AC Low Detect one-shot times out. With the one-shot reset, the AC LOW interface signal is generated. Following the AC LOW signal, the drive continues to operate until the next SECTOR pulse to reset the Low Speed Time Out one-shot. Thus, a data transfer in progress continues until the end of the sector before the interface signals are removed.

The remainder of the ac low stop cycle is the same as a low-speed stop (Paragraph 4.2.3.2). However, if a total power loss occurs before the heads are completely retracted, the safety relay closes to retract the heads under battery power (emergency retract) and to maintain the AC LOW interface signal.

4.2.3.4 DC Low Stop – If the +15 or -15 Vdc drops below 12 Vdc or if the +5 Vdc drops below +4.6 Vdc, the DC OK gate is disabled. The output from this gate immediately disables the Run gate, de-energizes the safety relay to retract the heads under battery power, and generates the BUS DC LOW interface signal.

4.2.4 Disk Drive Addressing

For greater flexibility in a multidrive system, a drive address assignment can be changed by changing the position of the Address Select Switch (S1) on the M7700 card. This switch operates in conjunction with the RK11-D interface line plus the address select decoding logic (M7700), as described in the following paragraphs.

4.2.4.1 RK11-D Address Selection – If the operating controller is an RK11-D, the interface signal BUS RK11-D L is present. This signal, applied through an inverter, enables a three-line-to-eight-line binary decoder and disables the linear input gates. Thus, when the binary-encoded (BUS SEL DR 0/A/E L through BUS SEL DR 2/C/H L) drive address is applied through the input gates to the binary decoder, the decoder translates the 3-bit binary code and activates one of the eight Address Select Switch positions. If the Address Select Switch on the M7700 card has been set to this activated position, the signal SELECT H is produced. SELECT H, ANDed with the set output from the Ready flip-flop (M7701) and the reset output from the Fault latch, produces the signal SELECT/READY L. This signal allows the drive to perform the various control and read/write operations.

4.2.4.2 RK11-C or RK8/E Address Selection – If the operating controller is an RK11-C or RK8/E, the interface signal BUS RK11-D L is not present. Hence, the three-line-to-eight-line binary decoder is disabled and the linear input gates are enabled. This circuit configuration connects the BUS SEL DR lines, as a linear set, directly to positions 0 through 3 of the Address Select Switch on the M7700 card. If that switch is set to one of the first four positions and the corresponding BUS SEL DR line is at a logical 1, the signal SELECT/READY L is produced as described in Paragraph 4.2.4.1, above.

4.2.5 Seek

4.2.5.1 Load Heads Seek – Placing the RUN/LOAD switch in the RUN position generates the signal LOAD HEADS L (Paragraph 4.2.2). Because the read/write heads are in the "home" position at this time, the signal OUTER LIMIT H is present (M7702). This signal is ANDed with the inverted LOAD HEADS L signal to set the Forward and reset the Reverse flip-flops. In addition, OUTER LIMIT H sets the Outer Limit Extender latch to hold the New and Current Address registers at 0.

The $\overline{Q}$ outputs from the New Address register and the Q outputs from the Current Address register are applied to the subtractor. Use of the $\overline{Q}$ outputs from the New Address register effectively complements the new address, allowing a 1's complement addition to take place in the subtractor. During this addition, the second stage of the subtractor performs an end-around carry operation. Because the Current Address register and the New Address register are both cleared, the remainder from the 1's complement addition is zero; thus, a no-carry condition is produced. The binary 0 from the subtractor is then applied, through exclusive OR circuits and the "> 3" decoding gate, to set the Difference register to a low-velocity binary output.

NOTE

Low velocity is when all stages of the Difference register are set. High velocity is when all stages are cleared.

When the Forward flip-flop sets, FWD H and MOVE L are generated. FWD H is applied to the servo logic to place it in the velocity mode (Paragraph 4.3.1.1) and initiate forward head motion.

As the heads begin to move at low velocity toward cylinder zero, count pulses are generated by the positioner

transducer (Paragraph 4.2.6). When the heads pass the outer limit of the recording disk, OUTER LIMIT H goes low, applying a low to the D input of the Forward flip-flop. As the heads approach cylinder zero, COUNT PULSE REV H (first count pulse after OUTER LIMIT H goes low) resets the Forward flip-flop. This action removes FWD H and MOVE L, and places the servo logic in the detent mode (Paragraph 4.3.1.2).

MOVE L high triggers the 6-ms Positioner Settle Delay one-shot (M7700). When this one-shot times out, the R/W/S Ready flip-flop sets to disable the Seek Incomplete counter, light the ON CYL indicator, and generate the BUS R/W/S RDY L signal. BUS R/W/S RDY H resets the Outer Limit Extender latch.

4.2.5.2 Forward Seek – To move the read/write heads closer to the disk spindle (forward seek), the controller places an 8-bit binary address on the Cylinder Address interface lines (BUS CYL ADD 0 through 7), transmits a STROBE pulse, and simultaneously addresses the disk drive (Paragraph 4.2.4). Reception of the STROBE pulse (M7700) generates the GOOD STROBE L pulse to clock the cylinder address from the interface lines (M7702) into the New Address register.

The $\overline{Q}$ outputs from the New Address register are applied to both the subtractor and the Invalid Address Detector. Use of the $\overline{Q}$ outputs of the New Address register effectively complements the new address and thus allows a 1's complement addition to take place in the subtractor. During this addition, the second stage of the subtractor performs an end-around carry operation.

If the New Address register output is greater than 202, the BUS ADDRESS INVALID signal is generated. If this is the case, the BUS ADDRESS ACCEPTED L signal remains high, keeping the Forward or Reverse flip-flops reset and preventing the Difference register from changing states.

If the New Address register output is equal to or less than 202, BUS ADDRESS INVALID L remains high. This signal is ANDed with the output of the Strobe Generator one-shot (M7700) to produce the BUS ADDRESS ACCEPTED L signal.

Simultaneously, the complemented New Address register output is added in the subtractor to the output of the Current Address register. If, after this addition process, a carry condition has not occurred, the positioner must either move the heads forward (toward the disk spindle) or retain the heads at their current location. To determine this fact, the subtractor carry output is inverted by the exclusive OR circuits for only a no-carry condition. If the heads are to move forward, the high output from the "not zero" decoding gate is ANDed with the inverted carry output and applied to the D input of the Forward flip-flop.

When BUS ADDRESS ACCEPTED L goes low, the Forward flip-flop clocks, generating MOVE L and FWD H. FWD H is applied to the servo logic to place it in the velocity mode (Paragraph 4.3.1.1) and initiate forward head motion. MOVE L resets the R/W/S Ready flip-flop (M7700) to accomplish the following:

a. Enable the Seek Incomplete counter.

b. Remove the BUS R/W/S READY/ON CYL L interface signal.

c. Turn off the SEEK DONE/ON CYL indicator.

Once enabled, the Seek Incomplete counter begins to count INDEX pulses (40 ms repetition rate). If the counter reaches a count of seven (seek incomplete condition), the Seek Incomplete latch is set to generate the BUS SEEK INCOMPLETE L interface signal. If this occurs, the controller must issue a return-to-zero (Restore) command or the operator must set the RUN/LOAD switch to LOAD and then back to RUN to continue normal operation.

If a seek incomplete has not occurred, and the distance from the present to the destination cylinder is greater than 31, an output from the "$\geqslant 32$" decoding gate clears the Difference register (M7702) to a high-velocity binary output. This binary output is applied to the servo logic to move the heads forward at high velocity.

NOTE

High velocity is when all stages of the Difference register are cleared. Low velocity is when all stages are set.

As the read/write heads move across each track, output pulses (COUNT PULSE FWD H) derived from the positioner transducer are generated. As long as the Reverse flip-flop remains reset, each COUNT PULSE FWD H clocks the Forward flip-flop set and increments the Current Address register. Each time this register increments, the previously described addition process is repeated in the subtractor.

When the heads are 31 cylinders from the destination cylinder, the "$\geqslant 32$" decoding gate is disabled, permitting the Difference register to be decremented directly by the decoded output of the subtractor. When the heads are 3 cylinders from the destination cylinder, the "$\leqslant 3$" decoding gate is enabled to set the Difference register to a low-velocity binary output. The Current Address register continues to increment until the heads are within one-half cylinder of the destination cylinder. At this point, the "not zero" decoding gate is disabled and the Forward flip-flop is reset, thereby removing FWD H and MOVE L.

FWD H low places the servo logic in the detent mode (Paragraph 4.3.1.2), while MOVE L high triggers the 6-ms Positioner Settle Delay one-shot (M7700). When this one-shot times out, the R/W/S Ready flip-flop sets to disable the Seek Incomplete counter, light the SEEK DONE/ON CYL indicator, and generate the BUS R/W/S READY/L interface signal. The drive is now ready to perform a read, write, or another seek operation.

4.2.5.3 Reverse Seek – A reverse seek is similar to a forward seek (Paragraph 4.2.5.2); however, if the current and new addresses are not alike, the subtractor (M7702) addition operation always results in a carry condition. Because of this fact, the "not zero" decoding gate is not used during this operation. The carry output from the subtractor sets the Reverse flip-flop to allow the Current Address register to decrement.

NOTE

Because of unique timing considerations during the reverse seek, inverted count pulses are used to decrement the Current Address register.

If, during the initial power-on cycle, the heads are not fully retracted (unloaded), the "home" microswitch at the rear of the positioner is not depressed and the HOME L signal is high. HOME L is ANDed with LOAD HEADS L (high, because the RUN/LOAD switch is in the RUN position) to generate REV H and MOVE L. Simultaneously, LOAD HEADS L sets the Difference register to a low-velocity binary output, thereby retracting the heads at low speed to the home position. At this position, the carriage contacts the home microswitch, causing the HOME L signal to go low and thus remove REV H and MOVE L.

The heads would not normally be over the disk during the initial power-on cycle. Thus, this operation ensures that the positioner will not move forward until the drive is placed in the run mode.

4.2.5.4 Return-to-Zero (Restore) Seek – To return the read/write heads to cylinder zero, the controller generates a BUS RESTORE L signal, transmits a Strobe pulse, and addresses the disk drive (Paragraph 4.2.4). Reception of the Strobe pulse (M7700) generates the GOOD STROBE H pulse. This pulse, ANDed with BUS RESTORE H, resets the Seek Incomplete latch to remove the BUS SEEK INCOMPLETE L interface signal. BUS RESTORE H also sets the RTZ flip-flop (M7702) to accomplish the following:

a. Clear the New Address register.

b. Clear the Current Address register.

c. Set the Reverse flip-flop.

d. Produce the RTZ L signal.

RTZ L resets the Seek Incomplete counter and prevents it from incrementing.

When the Reverse flip-flop sets, REV H and MOVE L are generated. REV H is applied to the servo logic to place it in the velocity mode and initiate reverse head motion (Paragraph 4.2.6.1). MOVE L resets the R/W/S Ready flip-flop (M7700) to accomplish the following:

a. Reset the RTZ flip-flop.

b. Set the Outer Limit Extender latch, which holds the New and Current registers at zero.

c. Reset the Reverse and set the Forward flip-flops.

When the Forward flip-flop sets, the heads begin to return toward cylinder zero. Just before the heads reach cylinder zero, OUTER LIMIT H goes low. The next output pulse (COUNT PULSE REV H) from the positioner transducer (Paragraph 4.3.2.1) resets the Forward flip-flop and thus removes FWD H and MOVE L.

FWD H low places the servo logic in the detent mode (Paragraph 4.3.1.2), while MOVE L high triggers the 6-ms Positioner Settle Delay one-shot (M7700). When this one-shot times out, the R/W/S Ready flip-flop sets to disable the Seek Incomplete counter, light the ON CYL indicator, and generate the BUS R/W/S READY L interface signal. R/W/S READY H also comes high at this time to clear the Outer Limit Extender latch.

If, at any time during normal operation, the read/write heads reach the inner limit of the recording disk, INNER LIMIT H (M7702) comes high. This signal sets the RTZ and Seek Incomplete flip-flops to initiate a return-to-zero seek automatically.

4.2.6 Sector/Index Pulse Generation

To read or record data with specific formats (e.g., data blocks) as well as to retrieve or store data at designated areas (sectors) on the disk, a timing scheme related to the rotational position of the disk is required. The SECTOR and INDEX pulses are used to accomplish this. These pulses are generated by slots in the recording disk hub that pass through a groove in the sector transducer. There are 12 equally spaced sector slots (16 slots for an RK8/E), which designate the 12 or 16 sectors on the disk. There is also one uniquely spaced index slot on the disk to indicate the last sector (one complete revolution). The sector transducer, located directly in front of the spindle, is an optical device that contains a light-emitting diode and a photosensor. As the recording disk rotates, the slots on the disk pass between the light-emitting diode and the sensor, producing negative SECTOR/INDEX pulses (Figure 4-10). Because both the SECTOR and INDEX pulses are produced from a single transducer, logic elements on the M7700 card are used to separate these two pulses and to encode the sector address.

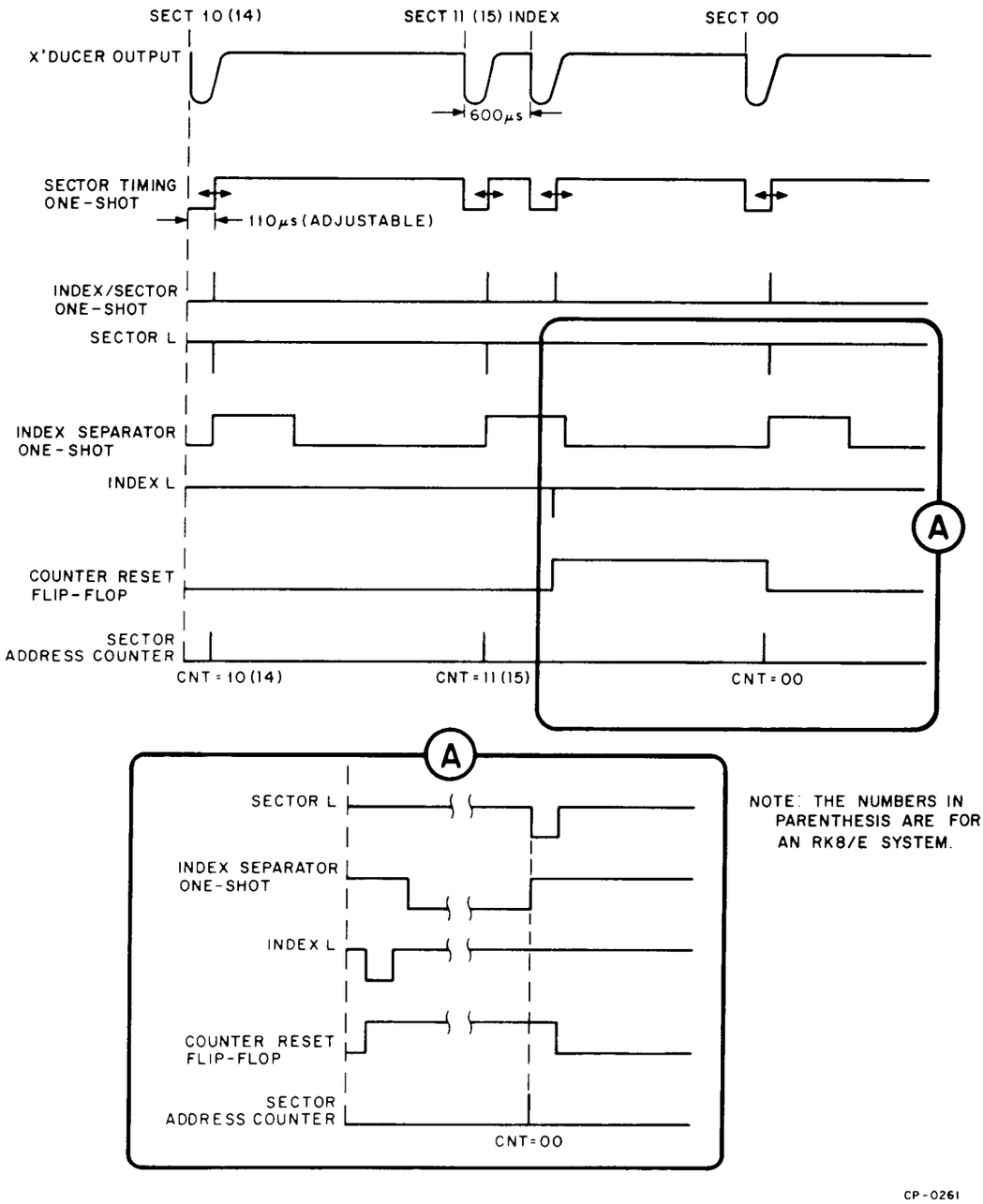

Figure 4-10 Sector/Index Timing

During disk rotation, SECTOR/INDEX pulses from the disk trigger the Sector Timing Delay one-shot. The pulse width of this one-shot can be adjusted to compensate for different sector transducer locations within various disk drives. Thus, when disk cartridges are interchanged, each data record is properly located with respect to the associated SECTOR pulse. The trailing edge from the Sector Timing one-shot triggers the Index/Sector one-shot to generate a 1-μs INDEX/SECTOR L pulse. The trailing edge of this pulse in turn triggers the 1-ms Index Separator one-shot. The output signals from this one-shot are applied to decoding gates to separate the SECTOR pulses from the INDEX pulse. If another slot has not passed the transducer, the SECTOR L signal is produced and the 4-stage Sector Address counter is incremented. This sequence of events is repeated for every sector on the disk hub.

The occurrence of the last SECTOR pulse triggers the Index/Sector one-shot as before; however, 600 μs later the INDEX pulse from the disk hub retriggers this one-shot. The set output from this one-shot is then ANDed with the set output from the Index Separator one-shot (still high from the previous triggering) to generate the INDEX PULSE L signal and to set the Counter Reset flip-flop. The leading edge of the next SECTOR pulse (sector 00) clears the Sector Address counter, and the trailing edge of this pulse resets the Counter Reset flip-flop. Thus, for every revolution of the disk, the counter is cleared to maintain the correct counter-to-disk relationship.

4.3 CARRIAGE POSITIONING

4.3.1 Positioner Servo Description

The positioner servo system (G938) controls the carriage movement. There are two control loops within this system. A velocity loop controls the carriage velocity during a seek operation (velocity mode) and a position loop electronically detents the heads at a fixed cylinder location when a seek operation is not being performed (detent mode). During the velocity mode, velocity and direction commands are obtained from the cylinder address and difference logic (Paragraph 4.2.5). During the detent mode, velocity and position feedback signals are derived from the linear positioner transducer (Paragraph 4.3.2.1).

The servo system (Figure 4-11) is composed of the following functional areas.

- A linear positioner transducer that produces two sinusoidal signals. During the velocity mode, these signals are used to control the rate of carriage movement. During the detent mode, only one of these signals is used to electronically detent the carriage. In addition, the transducer also generates two limit signals that indicate the extremities of carriage travel.

- A velocity function generator that converts the digital difference signal into corresponding analog velocity commands.

- A velocity synthesizer that generates a feedback control signal from the transducer output.

4.3.1.1 Velocity Mode – During a seek operation, the cylinder address and difference logic computes the digital difference between the present cylinder address and the destination cylinder (Paragraph 4.2.5). This digital difference is then converted, by the D/A velocity function generator of the analog, to an analog velocity command. The amplitude of the analog signal depends upon the distance to the destination cylinder. If the distance is less than 31 cylinders, a maximum velocity command is produced and applied to the velocity control loop. As the carriage accelerates, a feedback velocity signal is generated by the velocity synthesizer. When a speed of 35 ips is attained, this feedback signal inhibits further acceleration and maintains a constant 35 ips carriage speed until the heads are 31 cylinders from the destination cylinder. From this point, the carriage decelerates at a controlled rate that is governed by the decrementing digital difference applied to the function generator.

When the heads are 3 cylinders away from the destination cylinder, the velocity generator produces a fixed low-velocity command that continues to move the carriage at low velocity (about 3 ips) until the heads are approximately one-half cylinder from the destination cylinder. At this point, the low velocity command is removed; however, the velocity signal remains to damp the carriage movement and prevent overshoot. Once the destination cylinder is reached, the position loop electronically detents the carriage.

4.3.1.2 Detent Mode – The detent mode of operation electronically retains the read/write heads at a desired cylinder with a force greater than 2000 pounds per inch. During this operational mode, the velocity command from the function generator is zero, allowing the small velocity feedback signal to produce a stable position loop. If the heads tend to deviate from the desired cylinder, an error correction signal (SIN POSITION), which is opposite in polarity from the direction of deviation, is generated by the positioner transducer. This error signal is then directly applied through the loop amplifiers to move the carriage back to the desired cylinder.

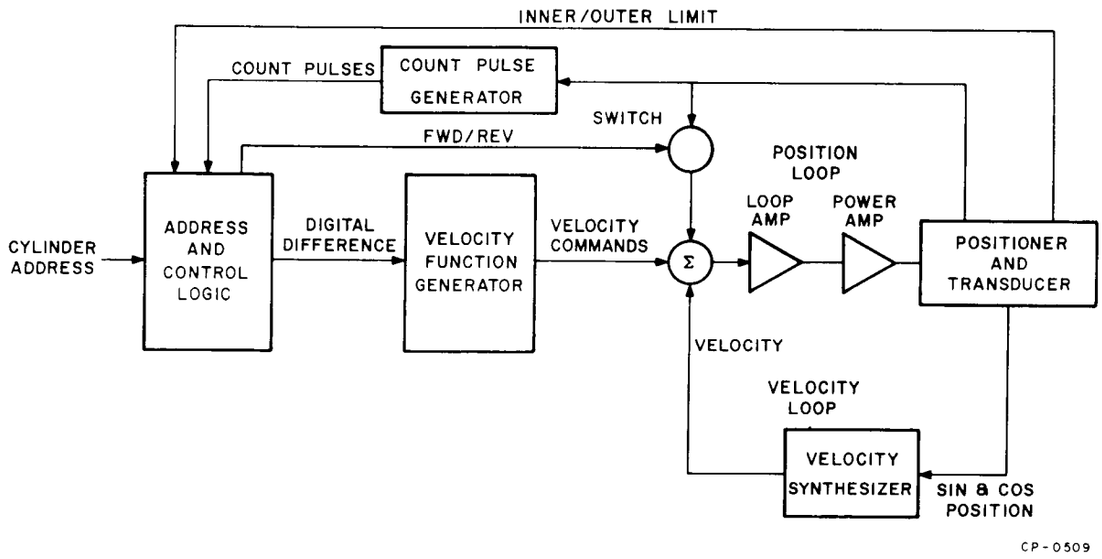

Figure 4-11 Servo System Block Diagram

4.3.2 Servo Circuit Description

4.3.2.1 Linear Positioner Transducer – The positioner transducer (Figure 4-12), located on the underside of the carriage, is an optical device that consists of two parts. The stationary portion (reticle) of the transducer is constructed in a U shape and is attached to the carriage slide. One side of the U contains a lamp; the other side contains a stationary reticle with minute diagonal transparent slots, plus six photosensors located behind the slots. The movable portion (scale) of the transducer contains a similar section of minute vertical transparent slots and is attached to the movable carriage. As the scale moves in the middle of the U-shaped reticle, the vertical and diagonal slots allow varying light patterns to shine onto the photosensors. This action produces two sine wave output signals that occur 90 degrees out of phase. These signals (SIN POSITION and COS POSITION) are used to control the movement of the carriage.

Two dc signals (INNER LIMIT and OUTER LIMIT) are also generated by the transducer. As long as the scale travel remains within the slotted section (cylinder 0 through 202), neither one of these signals is produced; however, when the scale reaches the inner travel extremity (> cylinder 202), the inner limit photosensor is uncovered and the negative INNER LIMIT signal is produced. The positive OUTER LIMIT signal is produced in a similar manner at the outer travel extremity (< cylinder 0). Both of these signals are used during a seek operation (Paragraph 4.2.5).

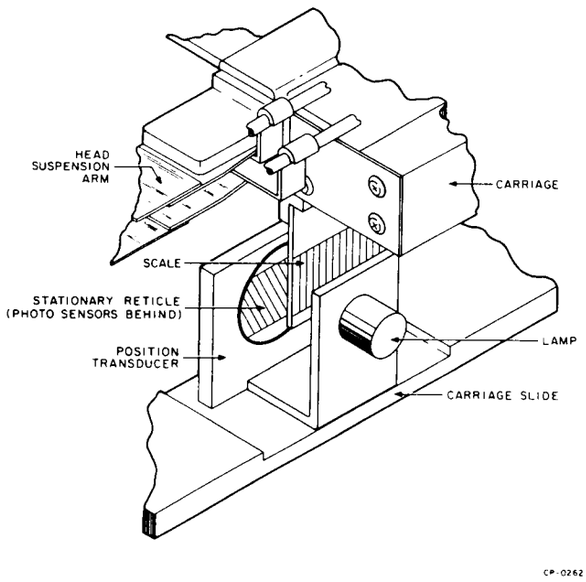

Figure 4-12 Linear Positioner Transducer

4.3.2.2 Velocity Function Generator – The velocity function generator (Figure 4-13) is a 5-bit D/A converter. The generator logic elements are located on the G938 card.

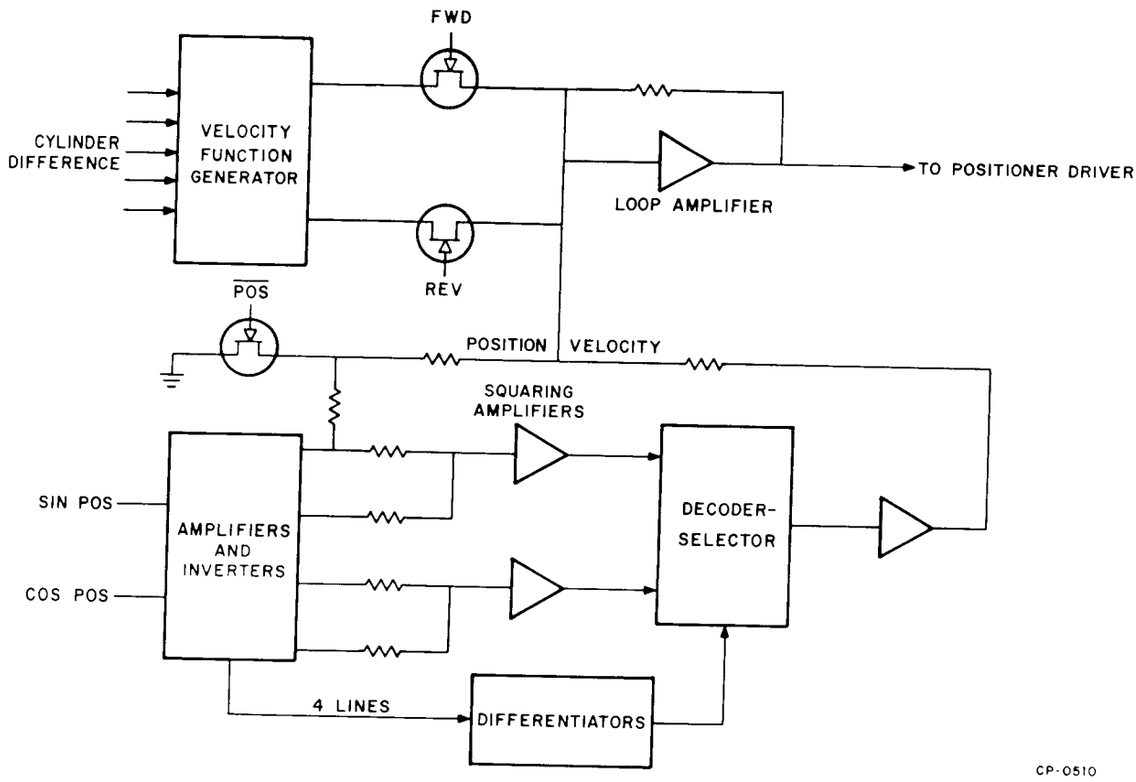

Figure 4-13 Simplified Positioner Servo Logic

The 5-bit digital input to this logic component is derived from the five low order difference bits from the cylinder address and difference logic. During a seek operation, these five bits represent the distance from the present cylinder address to the destination cylinder (Paragraph 4.2.5). If this distance is greater than 31, all 5 input bits are low, producing a maximum amplitude output signal (velocity command). If the travel distance is less than or equal to 3, all 5 input bits are high, producing a minimum velocity command. For differences between 4 and 30, the velocity command is proportional to the 5-bit binary representation. The velocity command is connected by field effect transistors (FETs) to the summing node of the loop amplifier. To initiate carriage motion, the FWD or REV signal turns on the appropriate FET, thereby applying the velocity and direction command to the loop amplifier.

4.3.2.3 Velocity Synthesizer — In a closed-loop servo system, a speed-sensing, feedback control signal is required to prevent uncontrolled velocity within the system. In the RK05, this control or tachometer signal is electronically derived in the velocity synthesizer. These elements are located on the G938 card.

During a seek operation, the SIN POSITION and COS POSITION signals from the positioner transducer are applied to amplifiers and unity gain inverters to provide four phases of position signal at the input of the synthesizer. The inverter/amplifier outputs are also applied to four differentiator networks. Appropriate pairs of amplifier/inverter outputs are applied to the summing junctions of two squaring amplifiers. The resultant square wave signals are displaced 90 degrees from each other and when these signals are gated together in the decoder/selector, they produce four separate selection signals of 90-degree duration. Each selection signal is centered around the peak of the corresponding differentiated signal. The derivative signals are then selectively summed in an operational amplifier to produce the velocity feedback signal. This signal is then applied, through a gain-setting resistor, to the summing node of the loop amplifier. Here, the velocity command from the velocity function generator is summed with the velocity feedback signal to produce a velocity profile signal (Figure 4-14). Thus, for a 202-cylinder seek (full carriage stroke), a maximum velocity profile is produced. The dotted lines on the figure represent the initial portions of shorter seeks; however, the terminating portion of all seeks remains the same.

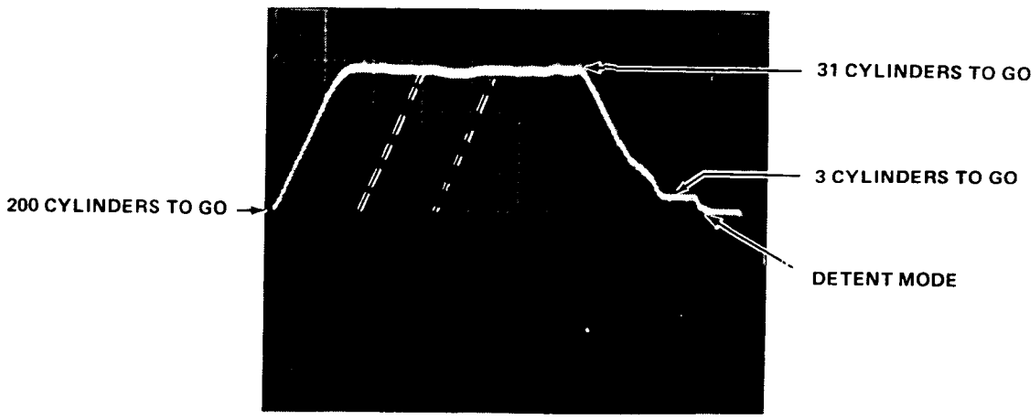

Figure 4-14 Velocity Profile

During the detent mode of operation, the $\overline{POS}$ signal turns on an FET that applies the SIN POSITION signal directly to the summing node of the loop amplifiers. This circuit configuration retains the heads at the desired cylinder location.

4.4 READ/WRITE

All the circuit elements required for head selection, level changing, and waveform shaping during a read/write operation are on the G180 card, which is located in the first position of the electronic module. The read/write head connectors are directly attached, through an opening in the side of the electronic module, to connector pins on this card.

4.4.1 Read Operation

During a read operation, the selected read/write head detects flux reversals from a recorded data track on the rotating disk. Each flux reversal generates a small voltage peak, whose polarity corresponds to the direction of the flux reversal. The read waveform is then amplified, filtered to remove high-frequency noise components, and applied to wave-shaping circuits. These circuits convert each voltage peak to 160-ns logic level pulses and apply this pulse train to the data separator circuits (Figure 4-15). In the separator, the individual data and clock pulses are separated according to the double-frequency recording scheme (Paragraph 4.1.5). The data separator also contains frequency tracking and peak-shift compensating circuits.

Figure 4-16 shows the time relationship and the waveforms for a read operation. The letters in parentheses ( ) in the following text correspond to the lettered waveforms in the figure.

To initiate a read operation, the controller:

a. Addresses a particular drive (Paragraph 4.2.4).

b. Positions the read/write heads at the appropriate cylinder (Paragraph 4.2.5).

c. Selects either the upper or lower read/write head (Paragraph 3.2.5).

For example, if the lower read/write head is to be used, the signal HD SELECT (G180-0-1) is high. This signal is ANDed with UNSAFE L (high, if no fault condition exists, Paragraph 4.5) to apply a ground potential to the center tap of the lower head.

As flux reversals on the disk surface pass under the lower read head, induced current flows through the lower head coil. The direction of this current flow depends upon the polarity of the flux reversal. These small read signals (approximately 5 mV) are then transmitted through the head-select diodes, through the series-isolation diodes, to a differential read preamplifier. The diode, resistor, and capacitive network between the read/write coils and the read preamplifier automatically isolates the preamplifier from the large write signals that occur during a write operation; however, this isolation circuit allows the small read signals that occur during a read operation to pass.

The amplified output from the preamplifier (approximately 300 mV) is then transmitted through a low-pass filter network to the read amplifier. The filter network removes noise and high-frequency disturbance but permits the lower frequency read signals to pass. The approximate 3.0 V read

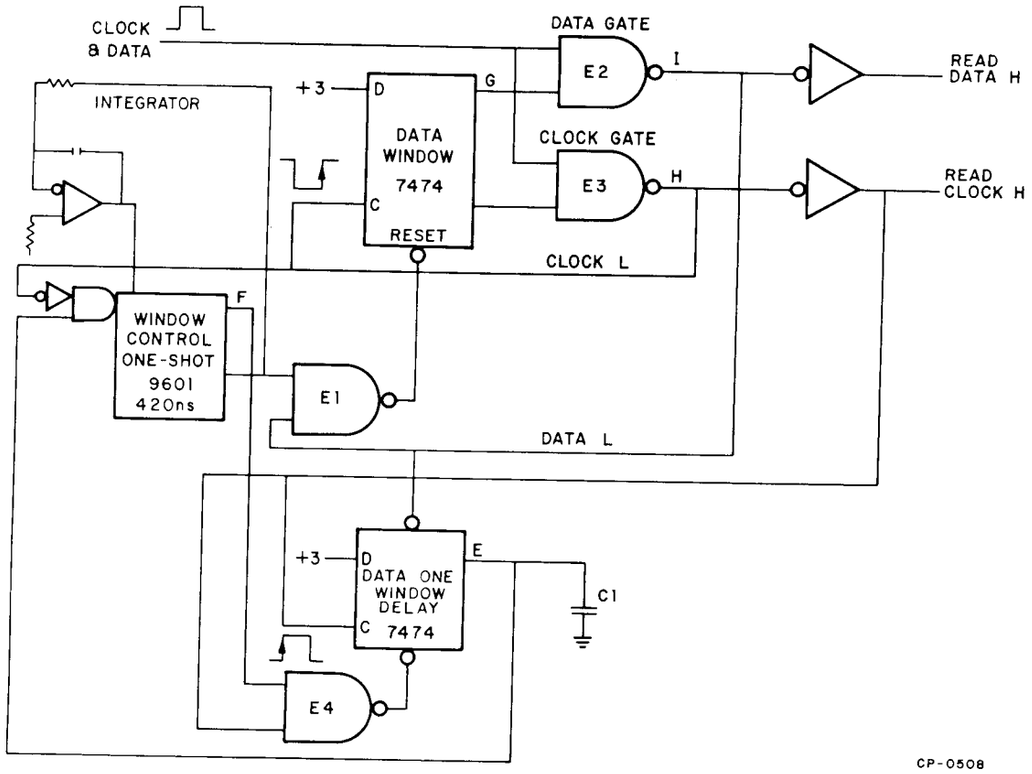

Figure 4-15 Simplified Data Separator Circuit

amplifier output (A) is applied to a balanced delay circuit where the signal is differentiated (B) and the signal peaks converted into zero crossings. The complementary zero crossings are then applied to a pair of high-gain differential comparators that convert the differentiated signal into square waves. Each square wave signal (C) triggers a corresponding one-shot, the outputs of which are combined to produce a composite 150-ns pulse train (D).

At this point, data and clock pulses are separated from the pulse train. Figure 4-15 is a simplified diagram of the data separation circuit. For a basic understanding of the following description, assume that the Data One Window Delay flip-flop remains set, keeping the input gate of the Window Control one-shot enabled.

If the Data Window flip-flop is in the reset state (G) when the leading edge of the first pulse on the pulse train occurs, the clock gate (E3) is enabled to produce the BUS RD CLK L signal (H) and to trigger the Window Control one-shot (F). The reset output from this one-shot is applied to an integrator circuit. After integration, the average voltage output is then applied to the adjustable input of the one-shot. Thus, if data frequency variations occur, this circuit configuration automatically varies the one-shot pulse width and thus maintains a constant duty cycle.

Triggering the Window Control one-shot also removes the reset input of the Data Window flip-flop, so that the trailing edge of the first clock pulse will clock the Data Window flip-flop set. Approximately 290 ns after this sets (slightly more than one-half bit cell), the Window Control one-shot will time out. If another pulse occurs on the pulse train (data 1 bit) before the time out, it will be enabled in the Data Gate (E2) to produce BUS RD DATA L (I), which will also keep the Data Window reset gate (E1) disabled for the duration of the data pulse so that the Data Window flip-flop will not be reset during the data pulse by the one-shot time out.

If another pulse did not occur (data 0 bit), the Data Window flip-flop will be reset by the one-shot time out via the Data Window reset gate.

In some bit sequences (e.g., a data 1 following a data 0), it is desirable to delay the resetting of the Data Window slightly longer than the normal one-shot time out. A magnetic recording phenomenon known as peak shift can cause the data 1 bit to lie beyond the cell center. A delaying circuit is provided so that, whenever a data 0 bit occurs, reset of the following Data Window flip-flop is delayed regardless of what the following data bit may be.

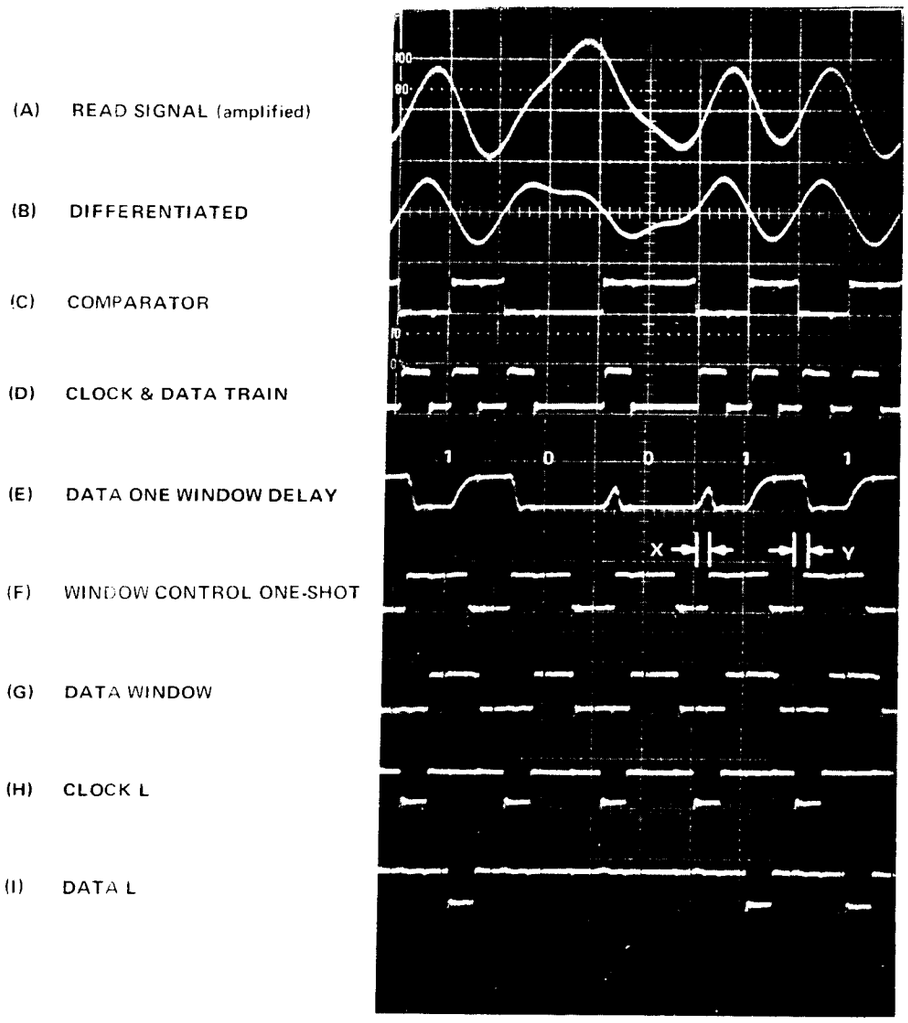

Figure 4-16 Read Waveforms

To accomplish this, a Data One Window Delay flip-flop set output is used to enable the Window Control one-shot.

The occurrence of a data 1 pulse direct-sets the Data One Window Delay flip-flop. The set output (F) then provides an enable signal to the Window Control one-shot so that the next clock pulse triggers the one-shot without delay. If a data bit is 0, the Data One Window Delay is not set until the leading edge of the following clock pulse. The set output rise is slowed by capacitor C1. This slow rise, gated with BUS RD CLK L, prevents the immediate firing of the one-shot, thus delaying the Data Window flip-flop reset. The one-shot firing also resets the Data One Window Delay via its reset gate (E4). This allows the Data One Window Delay flip-flop to be set by a possible data 1 pulse.

4.4.2 Write Operation

During a write operation, multiplexed write data and clock pulses are applied to the complementary Write Encode flip-flop. If the Write Gate signal is present and one of the

read/write heads has been selected, current flows through the erase coil as well as through one-half of the center-tapped write coil. Each pulse on the multiplexed input complements the Write Encode flip-flop and transfers current flow to the opposite half of the write coil; however, current flow through the erase coil remains constant throughout the write operation.

To initiate a write operation, the controller:

a. Addresses a particular drive (Paragraph 4.2.4).

b. Positions the read/write heads at the appropriate cylinder (Paragraph 4.2.5).

c. Selects either the upper or lower read/write head (Paragraph 3.2.5).

For example, if the lower read/write head is to be used, HD SELECT (G180-0-1) is high. This signal is ANDed with UNSAFE L (high, if no fault condition exists, Paragraph 4.5) to apply a ground potential to the center tap of the lower head.

At this point, the controller transmits the BUS WT GATE L signal, which is ANDed with SELECT/READY L to generate the signal SELECTED WRITE GATE H. The multiplexed data to be recorded is then transmitted over the BUS WT DATA & CLK L interface line. If the WT PROT switch is off (drive not write-protected), the signal NO PROTECT L accomplishes the following:

a. ANDs with BUS R/W/S READY/ON CYL L to complete the base current return circuit for the write drivers (Q1 and Q2).

b. ANDs with BUS WT DATA & CLK L to apply the data train to the complementary Write Encode flip-flop.

NOTE

The Write Encode flip-flop operates between +10 V and +15 V instead of the usual ground and +5 V levels.

When the BUS WRITE DATA & CLOCK pulse goes low, the Write Encode flip-flop sets, applying the +10 V reset output to the base of write driver Q2, causing it to conduct. With Q2 conducting, approximately 32 mA of current (adjustable with R13) flows through the upper portion of the lower write coil. In addition, a low voltage is applied to the base of the Erase Current Switch (Q3), causing it to conduct. When Q3 conducts, one leg of the Unsafe gate is enabled (Paragraph 4.5) and erase current flows through the lower erase coil.

When the BUS WRITE DATA & CLOCK pulse goes low again, the Write Encode flip-flop resets, causing write driver Q1 to conduct and Q2 to cut off. This circuit configuration transfers the current path to the lower portion of the lower write coil; however, the current direction in the erase coil remains constant. Thus, with each current transfer in the head coil, a flux reversal is recorded on the rotating disk surface.

4.5 FAULT DETECTION

If, during normal operation, the following three fault conditions are detected, all external commands to the drive are suppressed, and the FAULT indicator on the drive control panel lights. The fault conditions are:

a. Erase of write current without a BUS WT GATE L signal.

b. Linear positioner transducer lamp inoperative.

c. Any or all of +15, -15, or +5 Vdc low (dc low).

4.5.1 Current Fault

During a write operation, write driver Q1 or Q2 (G180-0-1), depending upon the polarity of the input data, is conducting. The low voltage output from either write driver turns on Erase Current Switch Q3 to enable one leg of the Unsafe gate. If BUS WT GATE L is present, the second leg of this gate is disabled; thus, Q4 conducts to keep the signal SET UNSAFE L high.

If, for any reason (e.g., shorted transistor), the Erase Current Switch should conduct without a BUS WT GATE L signal present, the Unsafe gate is enabled. This action turns off Q4 to generate SET UNSAFE L, which accomplishes the following:

a. Sets the Fault latch (M7701).

b. Generates the BUS WT CHK L signal and lights the FAULT indicator (M7701).

c. Deselects both read/write heads (G180-0-1).

4.5.2 Positioner Lamp Fault

This fault condition can only be detected when the read/write heads are in the home position. If the positioner lamp fails at any other time, various other checks will disclose this fact (e.g., BUS SIN L generated or BUS R/W/S READY L never generated, etc.). Therefore, the positioner lamp check is accomplished during the initial power-on cycle, or if the heads drift back to the home position after having once been loaded.

If the lamp fails and the heads are in the home position, HOME H (M7701) is present; however, OUTER LIMIT H (heads are at or beyond the outer portion of the disk) is low. This signal combination sets the Fault latch to light the FAULT indicator and generate the BUS WT CHK L signal.

4.6 POWER SUPPLY DESCRIPTION

The RK05 Disk Drive power supply (H743) and associated electronic cards are located in the left-rear portion of the disk drive. The power supply itself can be operated from a 115 or 230 Vac line voltage input, and consists of a dual transformer, two bridge rectifiers, and three voltage regulators. For 115 Vac operation, jumpers between P2 pins 1 and 2 and P2 pins 3 and 4 connect the dual primaries of transformer T1 in parallel. For 230 Vac operation, one jumper between P2 pins 2 and 3 connects the dual primaries of transformer T1 in series, thus maintaining 115 Vac across each primary. In either configuration, the 115 Vac blower motor is connected across T1 pins 1 and 2, while the 115 Vac spindle motor is connected across T1 pins 3 and 4.

When the power supply is activated, the secondary output of T1 pins 7 and 8 is applied through full-wave bridge rectifier D2, across capacitor C2, to the input of both the +15 V and +5 V regulators. The other T1 secondary output is likewise applied through full-wave bridge rectifier D1, across capacitor C1, to the input of the -15 V regulator. The regulator outputs are maintained within the following specified voltage limits, measured to center value of the peak-to-peak ripple from ground:

a.	+15 ±0.75 Vdc	200 mV peak-to-peak maximum ripple on any of the regulators, and 250 mV peak-to-peak maximum ripple on dc voltage pins of the logic assembly.
b.	-15 ±0.75 Vdc	
c.	+5 ±0.15 Vdc	

All three regulators contain current-limiting circuitry and are further protected against short circuits by a permanent fuse. Only the +5 Vdc regulator (logic power) contains a nonadjustable Zener diode for automatic overvoltage protection.