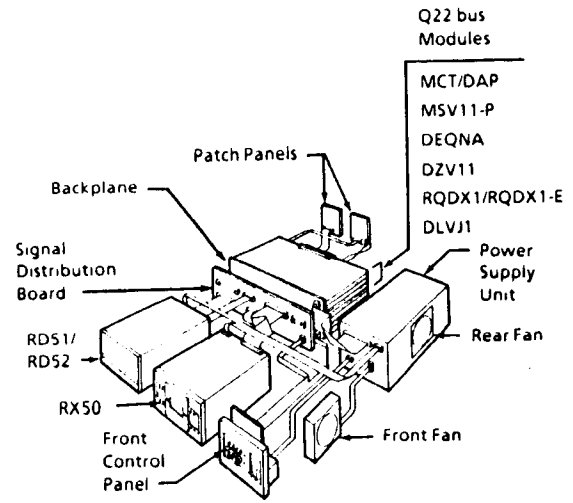


## Field Replaceable Units



### Print Sets

Print Set	Number
MicroVAX I Prints	MP-01896-01
512 Kb Parity Memory	MP-01239-00
RQDX1 Disk Controller	MP-01731-01
RX50 Diskette Drive	MP-01482
RD51 Fixed Disk Drive	MP-01638-01
RD51-A Fixed Disk Drive	MP-01897-01
RD51-D Disk Drive Subsystem	MP-01897
DZV11 Communication Option	MP-00462

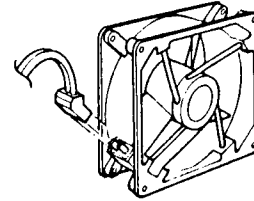
## 4: Removal & Replacement

### FRU Part Numbers

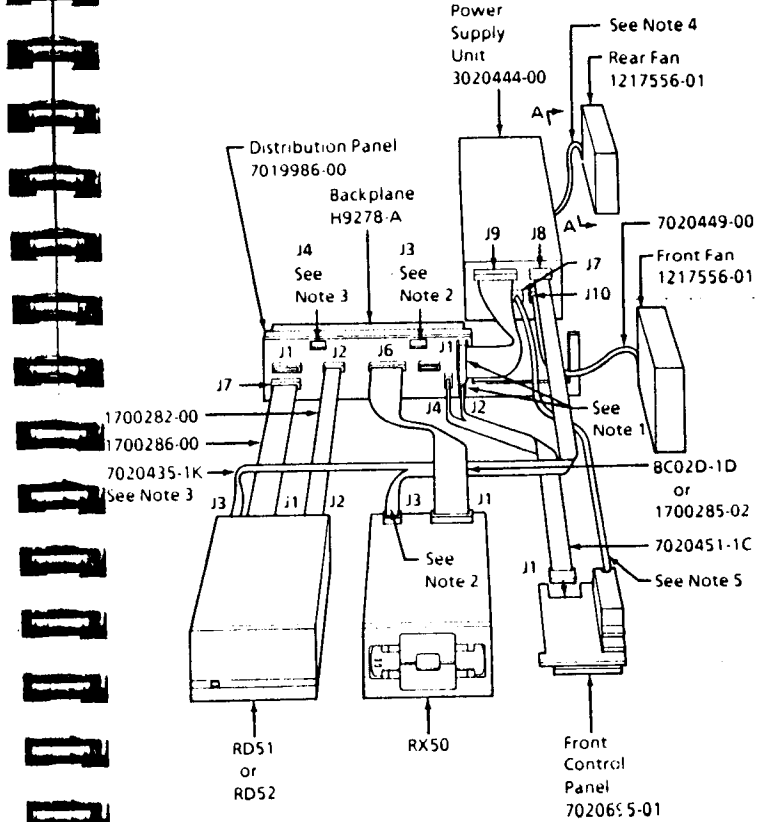
Part	Part Number
5 25 in. diskette drive	RX50-AA *
10 Mb fixed disk drive	RD51-A *
RD51 DIP Jumper Pack	29-24115-00
31 Mb fixed disk drive	RD52-A *
RD52 MPCB	29-24992-00
MCT	M7136
DAP (with G.Floating)	M7135
DAP (with D.Floating)	M7135-YA
MSV11-PL	M8067-LA
MSV11-PK	M8067-KA
DZV11	M7957
DZV11 Patch Panel Kit	CK-DZV11-DB
DLVJ1	M8043
DLVJ1 Patch Panel Kit	CK-DLVJ1-LB
DEQNA	M7054
DEQNA Patch Panel Kit	CK-DEQNA-KB
RQDX1	M8639-YA
RQDX1-E	M7512
RQDX1-E Patch Panel Kit	CK-RQDXE-KA
Grant Card	G7272
Backplane and Signal Dist. Board	70-19986-00
Power Supply Unit	30-21794-01
Rear Cooling Fan	12-17556-00
Front Cooling Fan	12-17556-01
Front Control Panel	70-20695-01
CPU Patch Panel	70-21150-01
SLU Cable	70-11411-1C
LED Cable	17-00563-01
Front Bezel (Rack Mount)	74-29501-01
Front Bezel (Floor/Table)	74-29559-0
Rear Bezel	74-27560-0
Pedestal (Foot)	74-27012-0
Enclosure	70-20469-0
Chassis Support Kits	70-20761-01

\* If you are adding one of these drives to a previously diskless system, you need to use the RX50-M, RD51-M, and RD52-M options. These options contain the drive and the signal cables.

## 4: Removal & Replacement



VIEW A-A  
2 places



### NOTES:

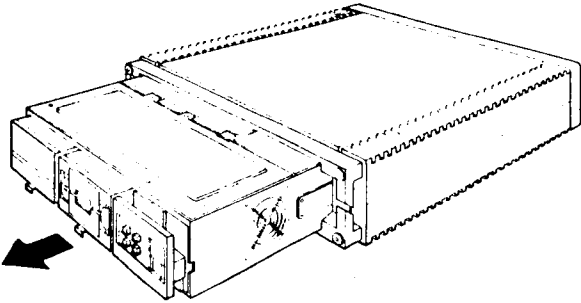
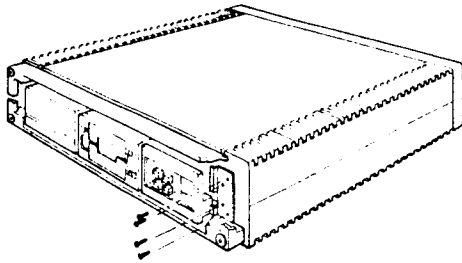
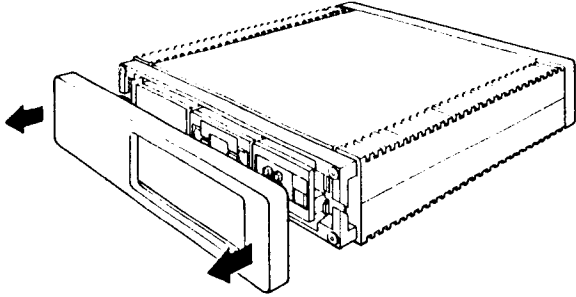
- 1 Connectors J1 & J2 are located on the back plane (H9278-A) assembly
- 2 If disk drive is not present, the power cable connector should be plugged into J3 on the distribution panel.
- 3 If disk drive is not present, the power cable connector should be plugged into J4 on the distribution panel
- 4 The rear fan cable is an integral part of the H7864 power supply.
- 5 The cable is an integral part of the 7020695-01 assembly.



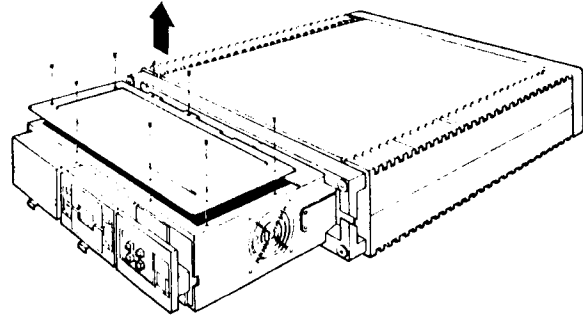
### Cabinet Disassembly

**Warning:** Never remove covers from the system unit, or attempt to remove or replace an FRU without first turning off the system power and unplugging the power cord from the wall receptacle. Failure to perform these actions will expose you to lethal voltages.

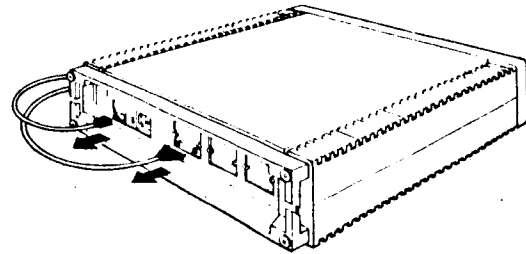
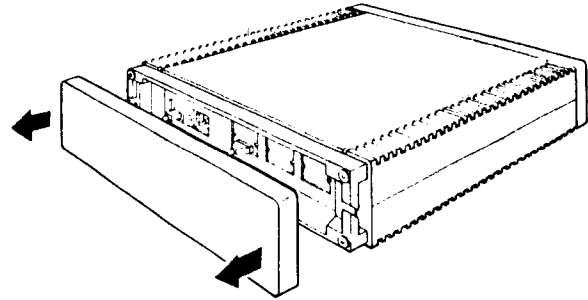
#### Gaining Access to the Front of the System Unit



Front Access

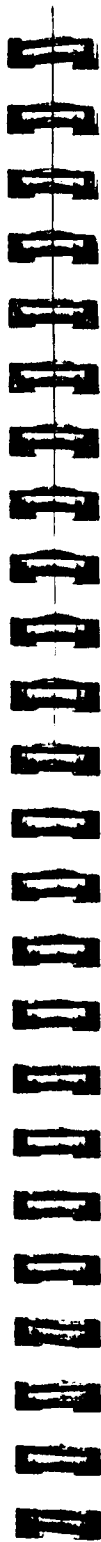


#### Gaining Access to the Rear of the System Unit



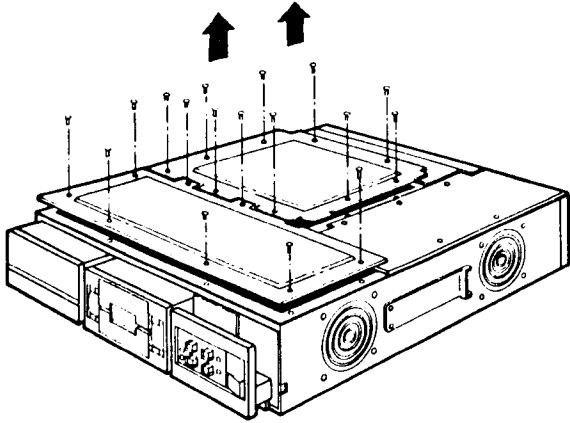
69

Rear Access

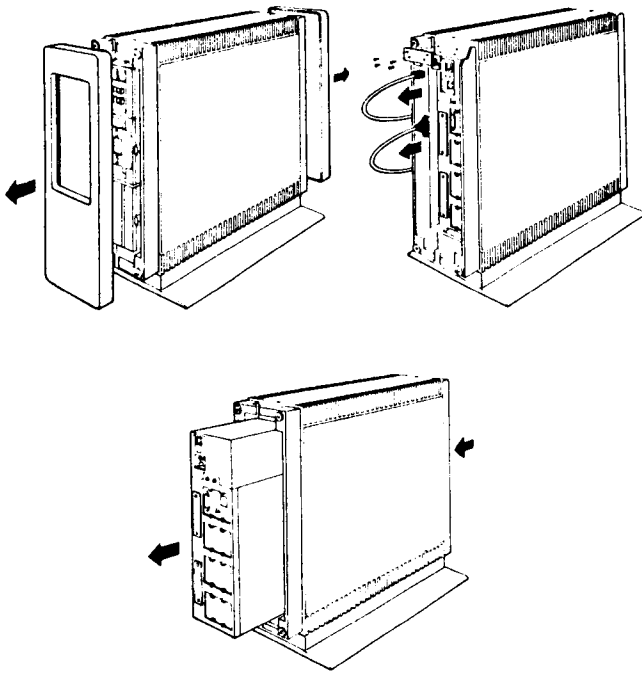


## 4: Removal & Replacement

### Gaining Access to the Top of the System Unit



### Floor Standing Systems

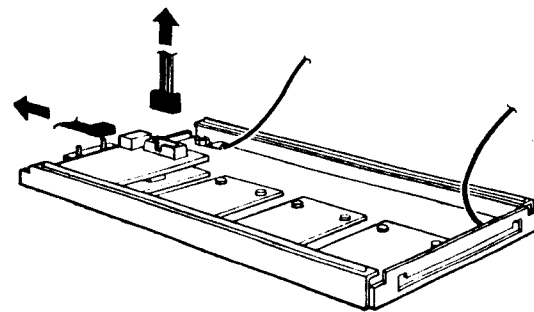
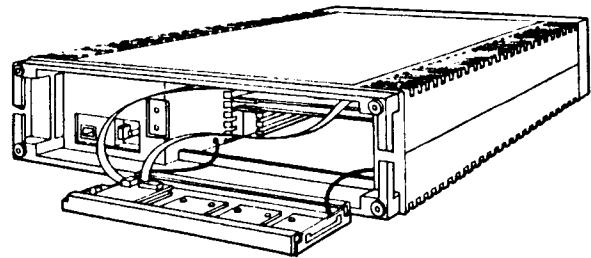
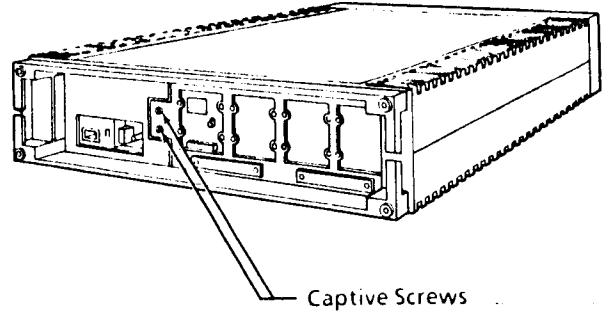


## 4: Removal & Replacement

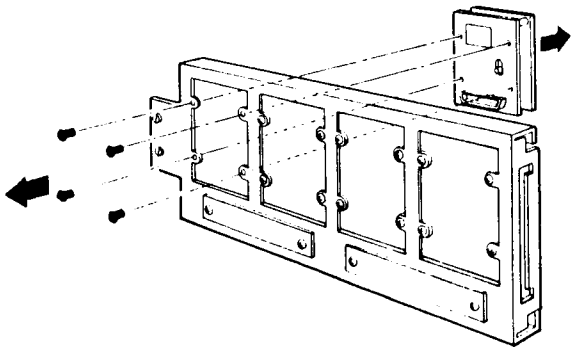
### Patch Panel

#### Removal (the CPU patch panel is shown here)

- 1 Gain access to the rear of the system unit
- 2 Loosen the two captive screws on the patch panel assembly.

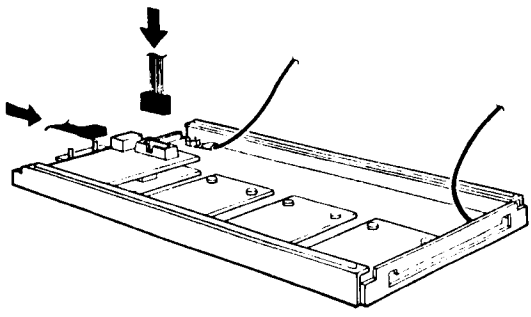


4: Removal & Replacement



Replacement (the CPU patch panel is shown here)

- 1. Ensure the orientation of the connectors is as shown

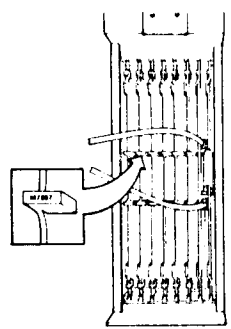


Q22 Bus Modules

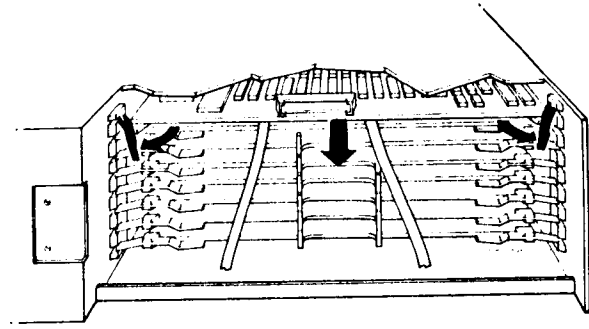
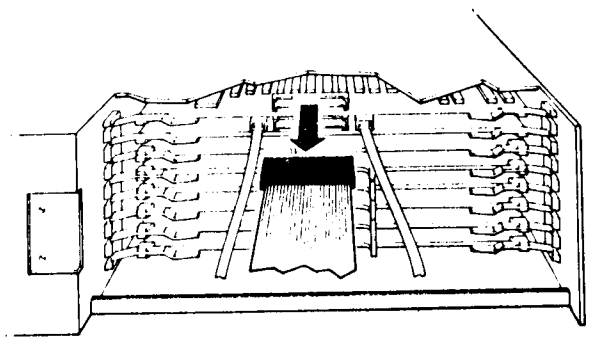
Removal

- 1. Gain access to the rear of the system unit.
- 2. Most modules have a part number stamped on the visible portion as you look into the rear of the unit. The MCT and DAP are installed in the first and second slots respectively. If fitted, the RQDX1-E and the DLVJ1 are located in the slots after the RQDX1.

Module	Part Number
MCT	M7136
DAP	M7135
MSV11-PL	M8067-LA
MSV11-PK	M8067-KA
DZV11	M7957
DEQNA	M7054
Grant Card	G7272
RQDX1	M8639
RQDX1-E	M7512
DLVJ1	M8043



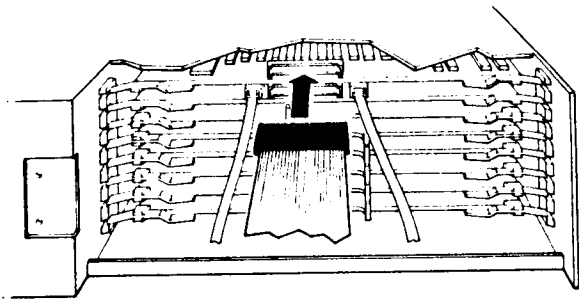
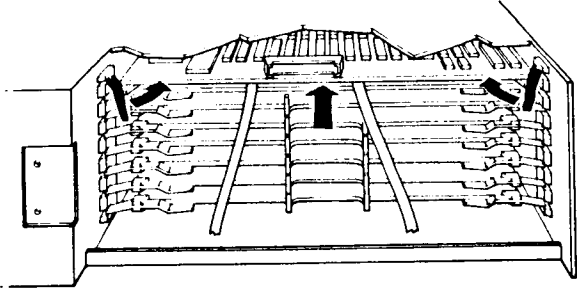
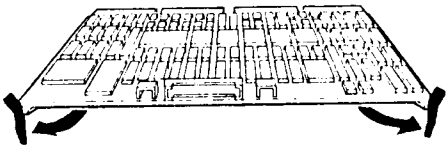
4: Removal & Replacement



Replacement

- 1. Ensure the configuration of jumpers on the replacement module is as described in section "5: System Configuration". If you are replacing the DAP, MCT, RQDX1, RQDX1-E or the first MSV11-P, DEQNA, DZV11 or DLVJ1 module, the jumpers are set correctly in the factory. All memory modules should be in sequential slots starting from the third slot.
- 2. If you are replacing the RQDX1 disk controller, it is normally installed in the last occupied slot of the backplane (unless you have a DLVJ1 or RQDX1-E installed). If empty slots are left between the other modules and the RQDX1 disk controller, install grant cards in the empty slots to accommodate the interrupt and direct memory access structure of the backplane.
- 3. If you have an RQDX1-E installed, it must be fitted in the AB columns of the last-used slot. The RQDX1 must be in the slot before the RQDX1-E.
- 4. If you have a DLVJ1 installed, it must be fitted in the last-used slot. Because the DLVJ1 is a dual board, it must be fitted in the CD columns with a grant card fitted in the AB columns. If you have both a DLVJ1 and an RQDX1-E, you may fit the RQDX1-E in the AB columns rather than the grant card.

## 4: Removal & Replacement



## RD51 and RD52 Disk Drives

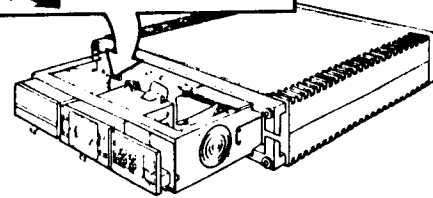
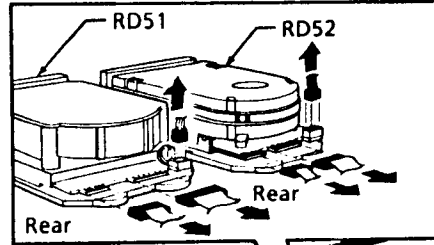
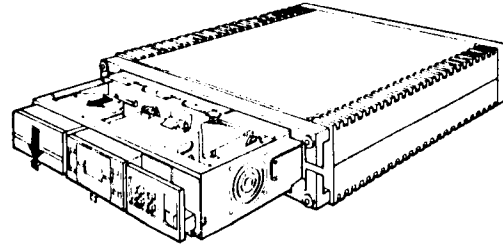
**Caution:** Use extreme care when handling the RD51/RD52 disk drive. Sudden physical shocks to the drive will damage it.

### Removal

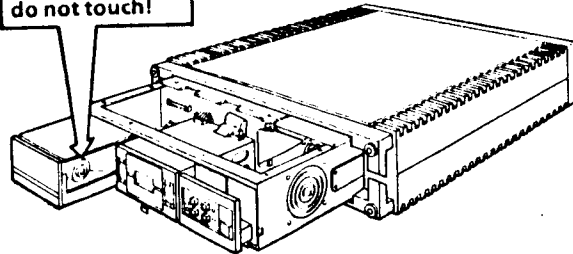
1. Gain access to the front of the system unit.
2. Obtain access to the cables connected to the rear of the drive by pressing down on the release tab and sliding the drive forward.

**Caution:** When sliding the drive forward, do not hold the sides of the drive as this could cause damage. Instead, push down the release tab, and slide the drive forward about two inches as shown on next page.

## 4: Removal & Replacement



**Head positioner  
do not touch!**

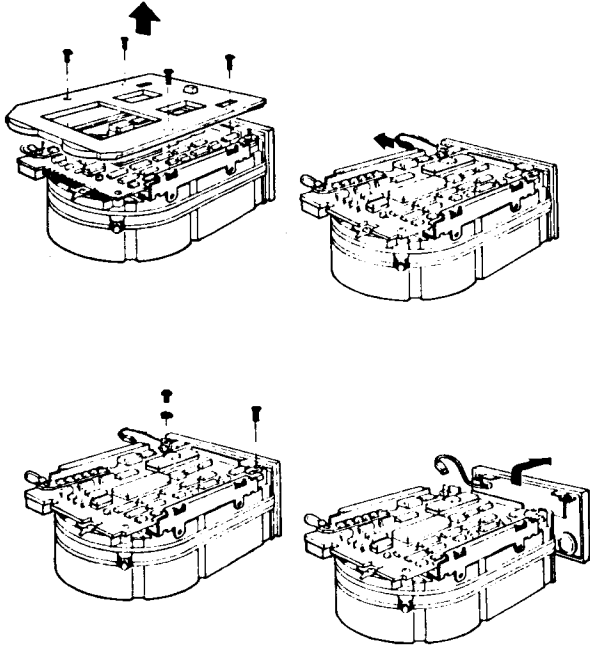
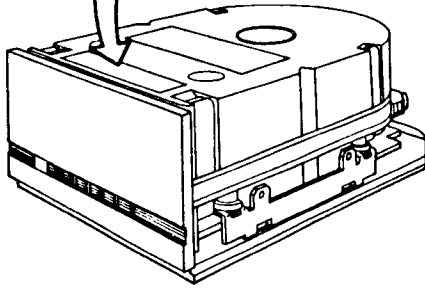


## 4: Removal & Replacement

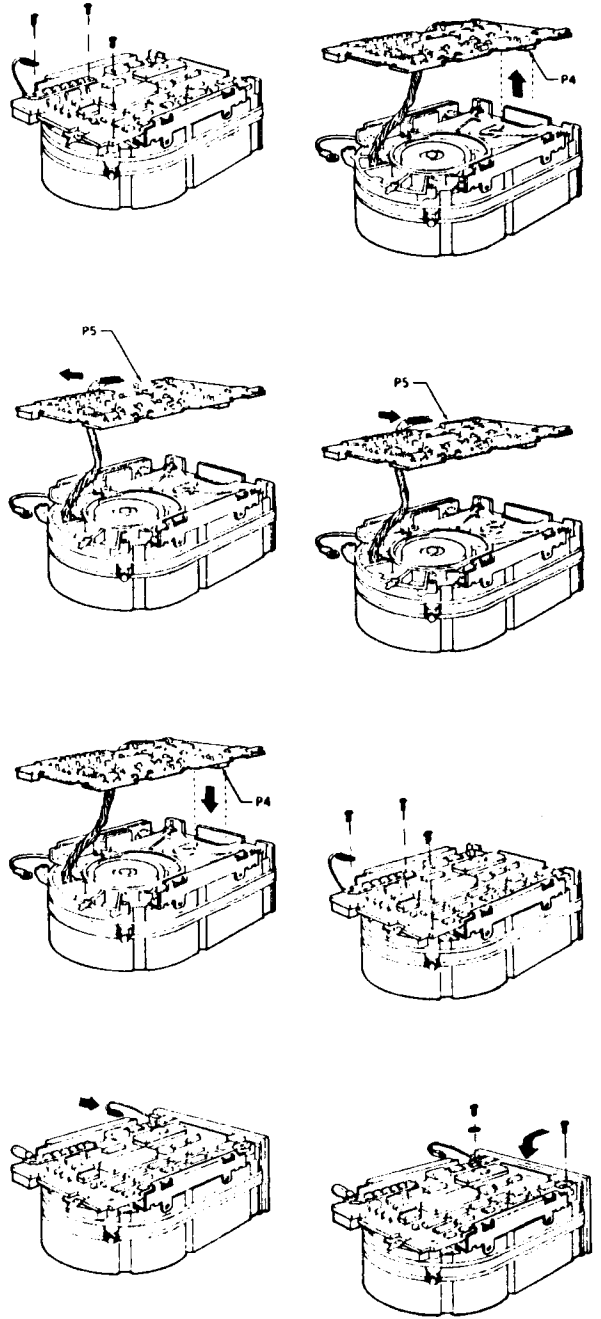
### Replacement

- (RD52-A with part number 30-21721-02 only).  
If you have removed an RD52-A drive with this part number, replace the main printed circuit board (MPCB) before replacing the whole drive

RD52-A 30-21721-02 REV-A1

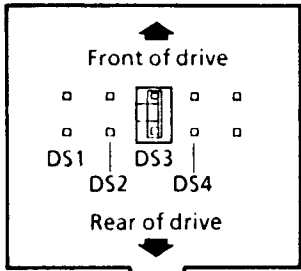


## 4: Removal & Replacement

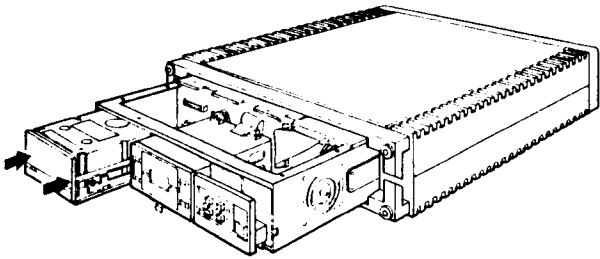
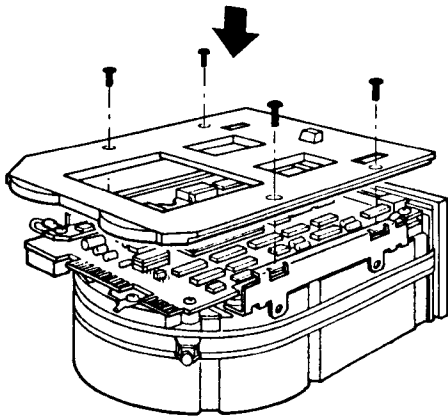
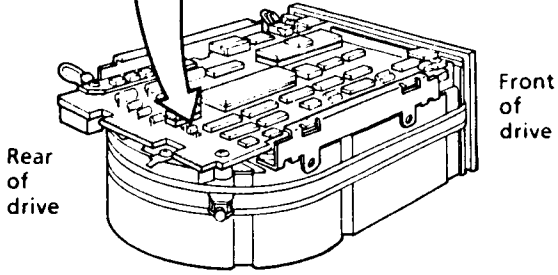




#### 4: Removal & Replacement



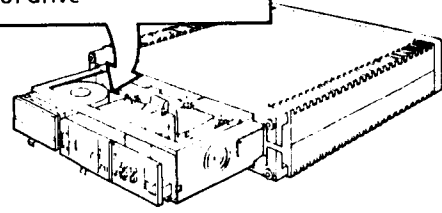
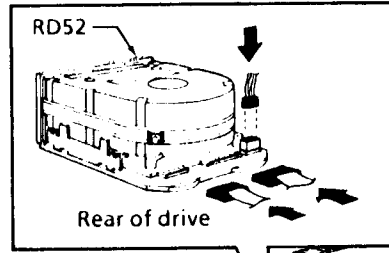
Note: DU1 is selected by installing the jumper on pin DS4.



RD52-A (#30-21721-02) 78



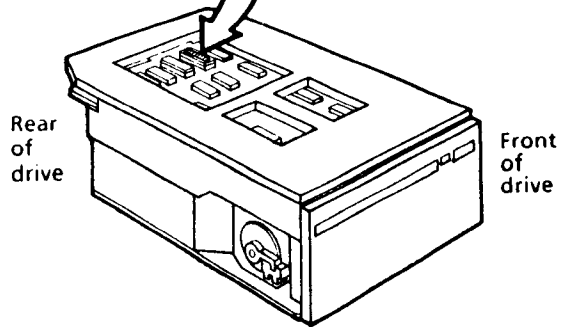
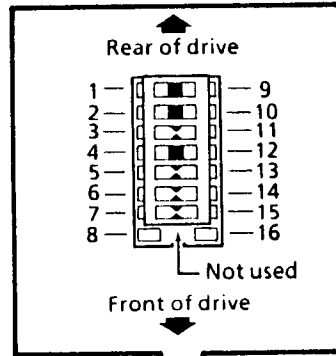
#### 4: Removal & Replacement



#### Replacement

##### 1. (RD51 only).

If the DIP shunt pack setting is not as shown, it will have to be replaced. Remove the DIP shunt pack. Fit a new DIP shunt pack (29-24115-00). Set the jumpers on the jumper pack as shown.



79

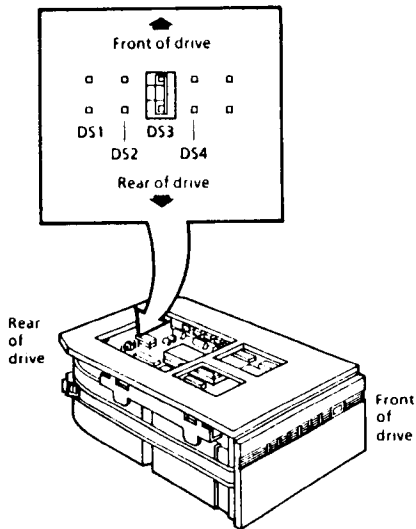
RD51

## 4: Removal & Replacement

### Replacement

#### 1 (RD52-A part number 30-21721-02 only).

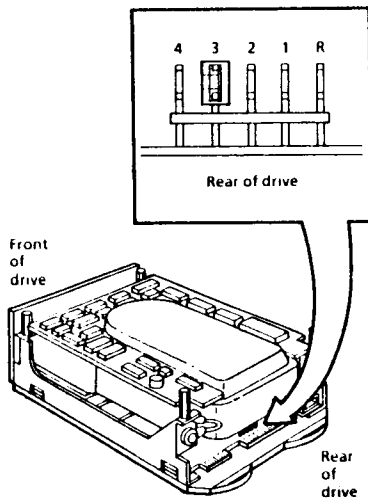
Set the drive select jumpers. The correct setting of the jumpers to select DU0 is shown below. To select DU1, jumper pin DS4



### Replacement

#### 1 (RD52-A part number 30-23227-02 only).

Set the drive select jumpers. The correct setting of the jumpers to select DU0 is shown below. To select DU1, jumper pin D4

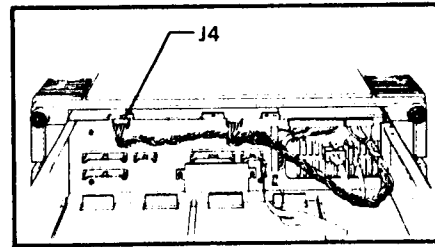
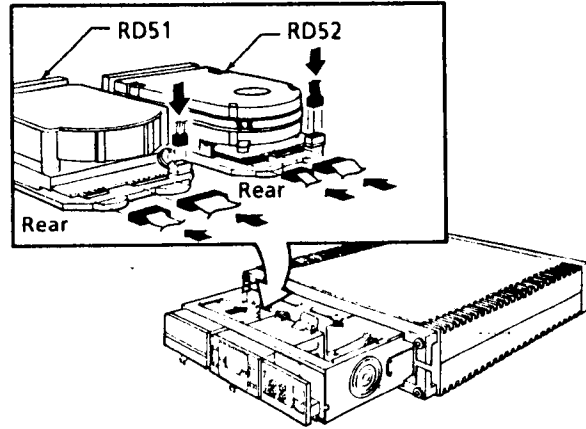


## 4: Removal & Replacement

2 Slide the drive most of the way into the chassis. Leave enough space to connect the cables

**Caution:** Do not hold the front right hand side of the drive. Push on the front corners.

**Note:** If you are installing the RD51/RD52 into a system that did not previously have one, the power cable is connected to J4 on the signal distribution board. Disconnect it from J4 and connect it to the RD51/RD52 power socket

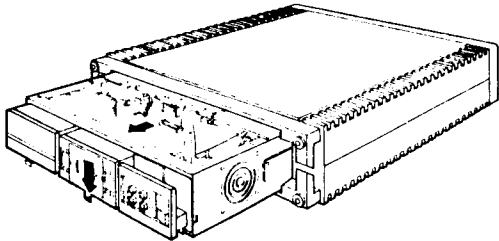
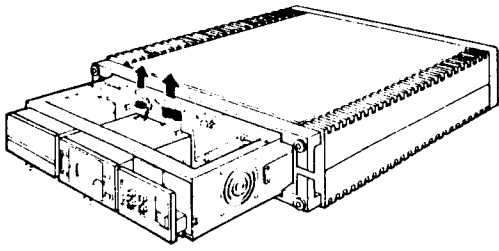


3 Pack the drive you removed in the special shipping case.

# RX50 Diskette Drive

## Removal

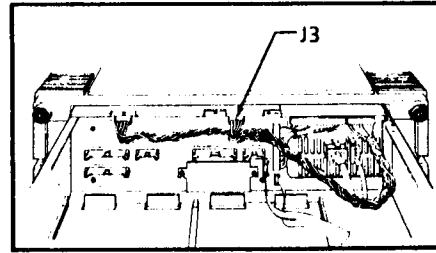
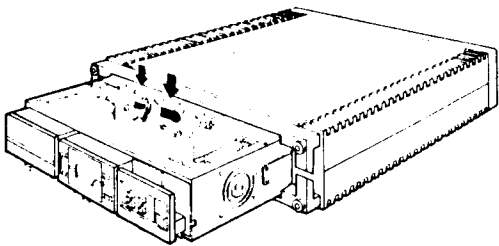
- 1 Gain access to the front of the system unit



## Replacement

- 1 To install the replacement drive, slide the drive into the chassis and connect the signal and dc power cables

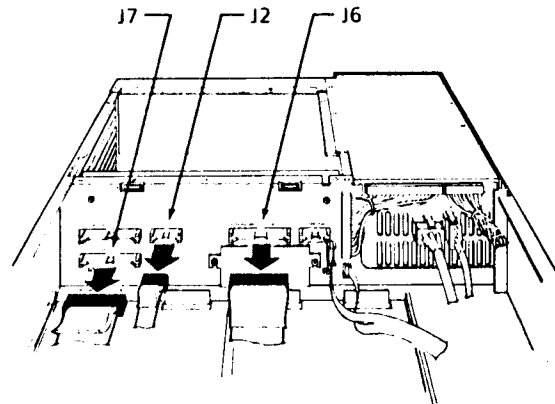
**Note:** If you are installing the RX50 into a system that did not previously have one, the power cable is connected to J3 on the signal distribution board. Disconnect it from J3 and connect it to the RX50 power socket



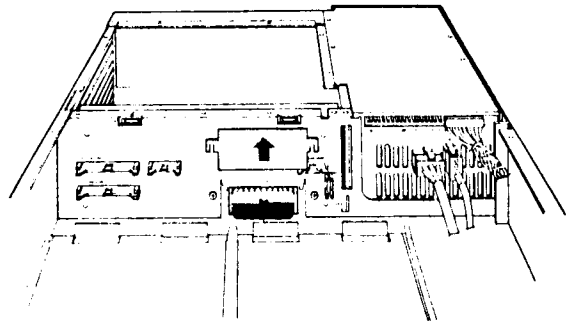
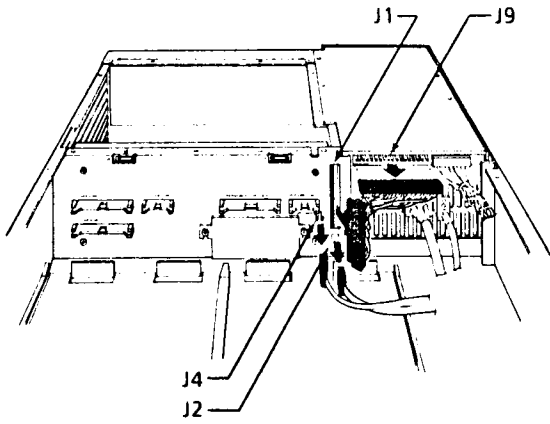
# Backplane Assembly and Signal Distribution Board

## Removal

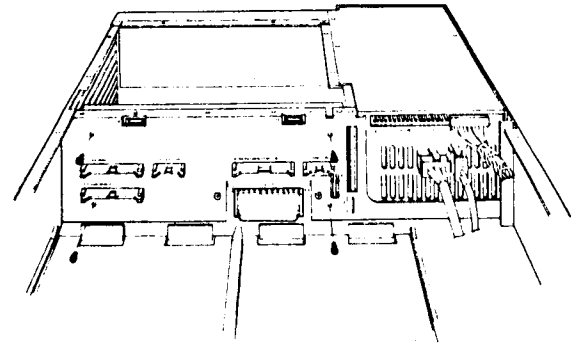
- 1 Gain access to the top of the system unit
- 2 Loosen the two captive screws and swing open the patch panel assembly
- 3 Remove the Q22 bus modules.
- 4 Remove the disk drives. Disconnect the signal cables from the signal distribution board, not the drives.



#### 4: Removal & Replacement

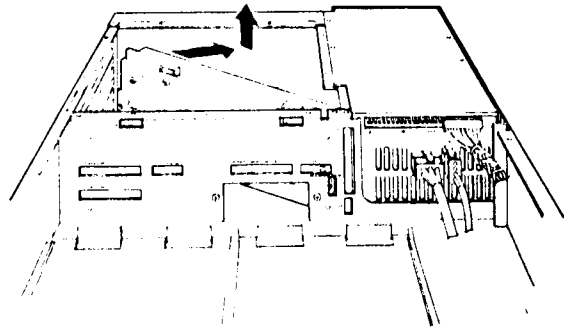


5 Remove the four screws that hold the backplane assembly to the chassis



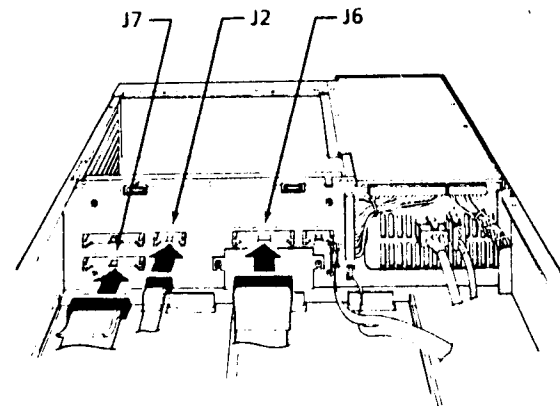
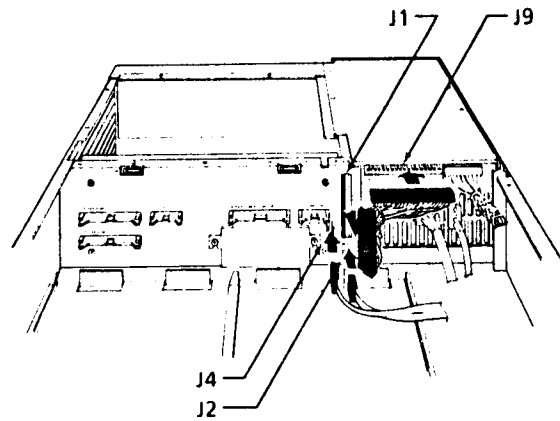
Backplane & Dist. Board 84

#### 4: Removal & Replacement



#### Replacement

- 1 Replace the back plane assembly Refit the four screws that hold the back plane assembly to the chassis
- 2 Reconnect all connectors and disk drives.



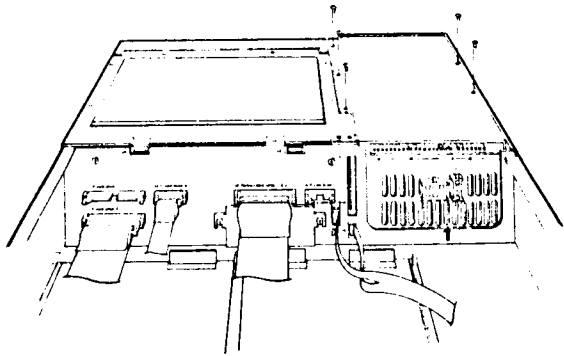
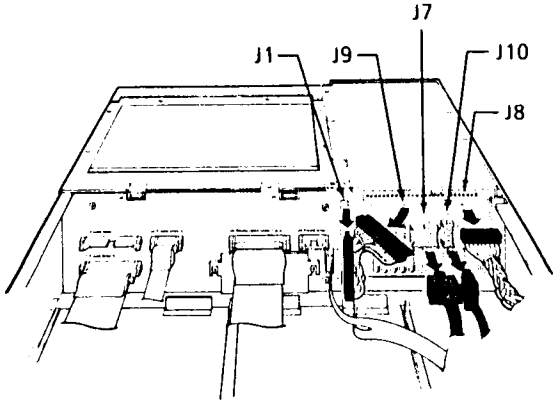
85 Backplane & Dist. Board



# Power Supply Unit

## Removal

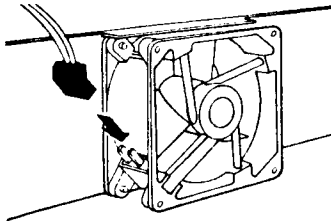
1. Gain access to the top of the system unit



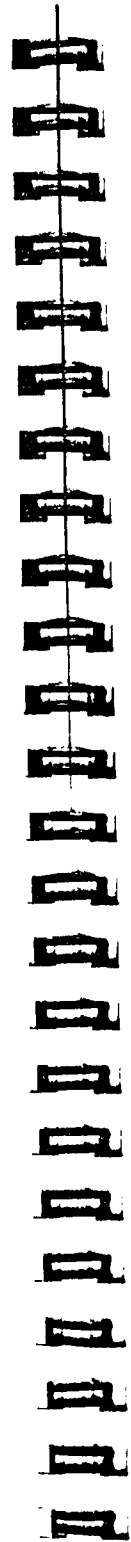
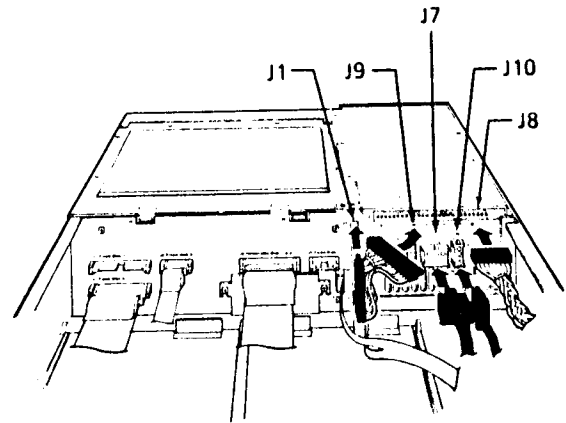
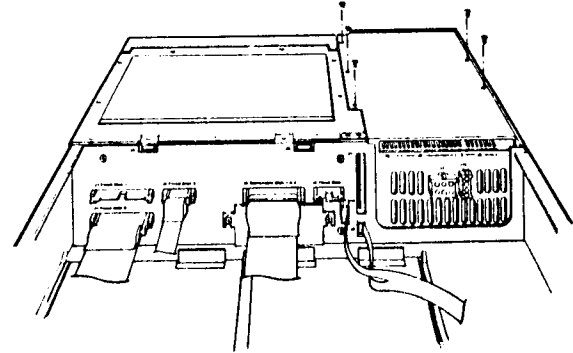
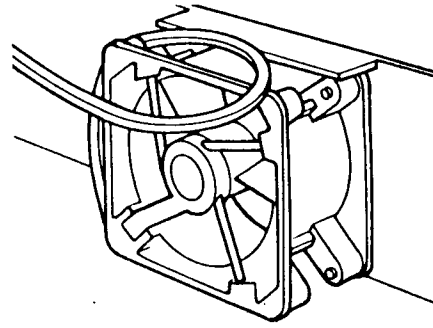
2. Lift the power supply out of the chassis and set it on top of the Q22 bus modules cover
3. Disconnect the power connector from the rear cooling fan

## Replacement

**Caution:** When reconnecting the rear fan power cable, observe the polarity of the connector because it is not keyed. The curve of the connector must match the curve of the fan housing as shown



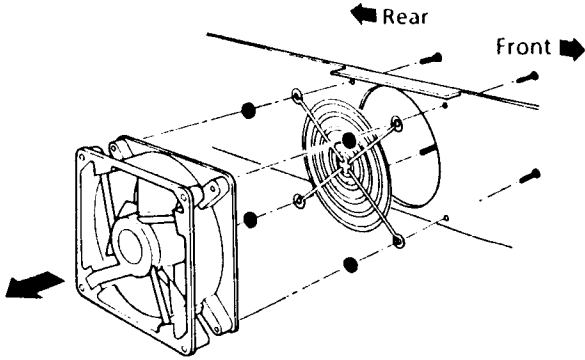
1. Place the power supply unit in position. Ensure the rear fan cable is routed over the top of the rear cooling fan as shown



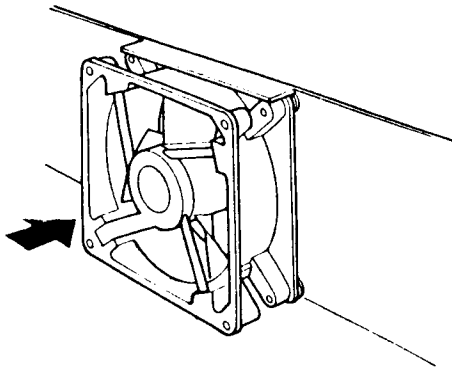
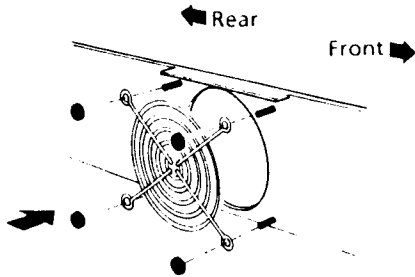
# Rear Cooling Fan

## Removal

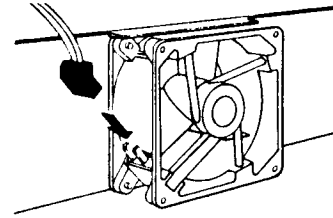
1. Gain access to the top of the system unit
2. Remove power supply



## Replacement



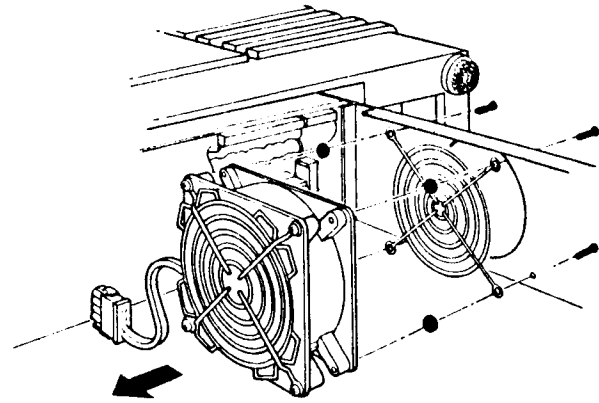
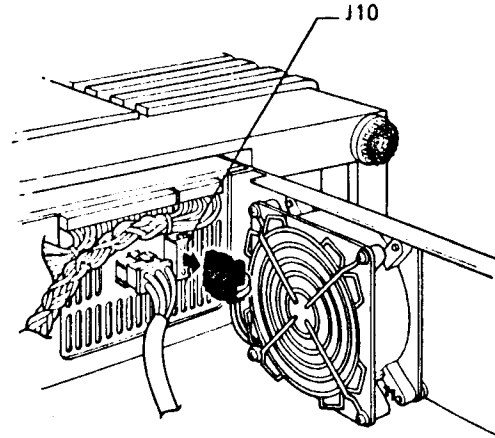
**Caution:** When reconnecting the rear fan power cable, observe the polarity of the connector because it is not keyed. The curve of the connector must match the curve of the fan housing as shown



# Front Cooling Fan

## Removal

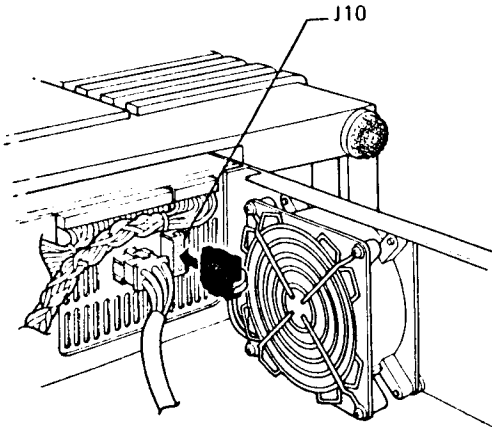
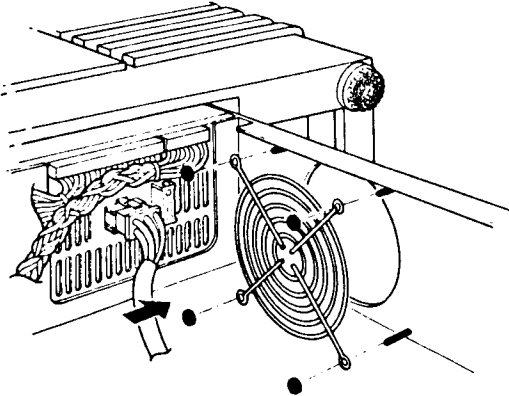
1. Gain access to the front of the system unit.
2. Remove RX50 diskette drive



Replacement

- 1. Remove the power cable and the fan guard from the intake side of the old fan and fit them to the replacement fan

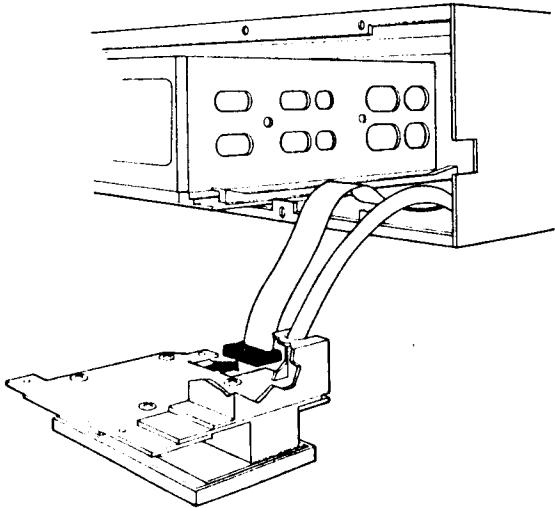
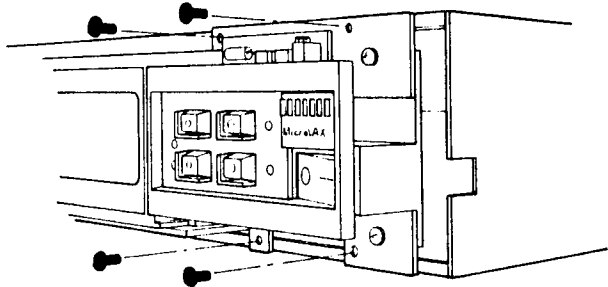
**Caution:** When reconnecting the fan power cable, observe the polarity of the connector because it is not keyed. The curve of the connector must match the curve of the fan. See drawing on previous page



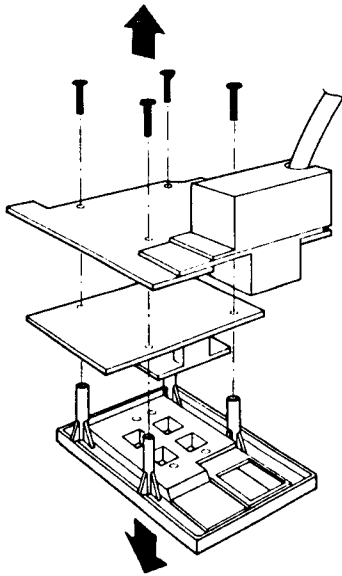
Front Cooling Fan

Front Control Panel

Removal

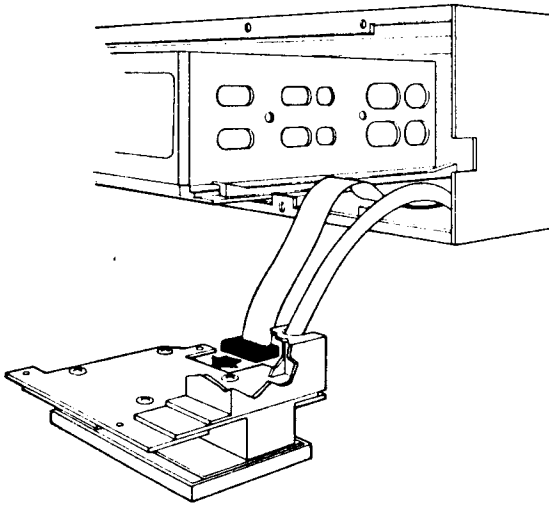


#### 4: Removal & Replacement



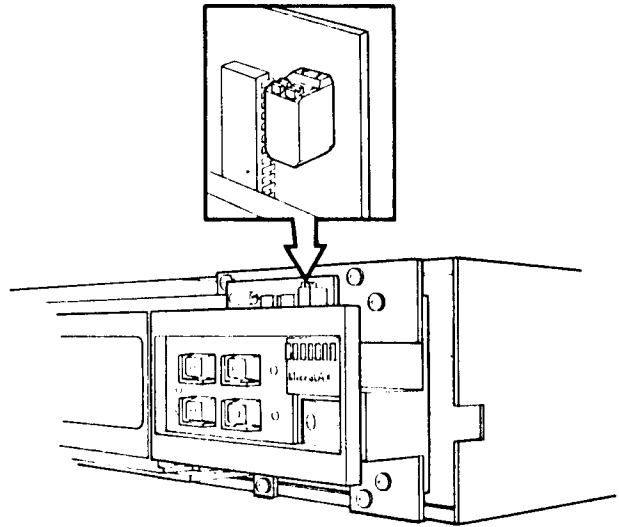
#### Replacement

1. Place the control panel on the assembly. Use the LEDs to orient the panel. Replace the four screws that hold the control panel to the assembly.

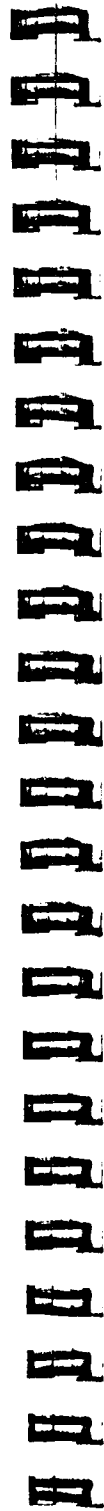


#### 4: Removal & Replacement

2. Ensure the two switches are in the out (forward) position as shown.







### MicroVAX I System Options & Power Consumption

Option	Size	+ 5 V	+ 12 V	AC Bus Load	Panel Insert
DEQNA	double	3.50	0.50	1.0	1" x 4"
DLVJ1	double	1.00	0.25	1.0	2" x 3"
DZV11	quad	1.15	0.40	4.0	2" x 3"
G7272 <sup>1</sup>	single	—	—	—	—
KD32-AA or AB <sup>2</sup>	two quads	12.00	0.50	4.0	2" x 3"
MSV11-PK <sup>3</sup>	quad	3.45	—	2.0	—
MSV11-PL <sup>4</sup>	quad	3.60	—	2.0	—
RQDX1 <sup>5</sup>	quad	6.40	0.1	2.5	—
RQDX1-E <sup>6</sup>	double	0.5	—	—	1" x 4"
RD51	—	1.00	1.60	—	—
RD52	—	1.50	2.50	—	—
RX50	—	0.85	1.80	—	—

<sup>1</sup> G7272 is the bus grant continuity card. If a double module is located between two quads, install the grant card in the A or C portion of the slot containing the double. The grant card's printed side must face away from the CPU.

<sup>2</sup> The KD32-AA consists of the memory controller module M7136 and the data path module M7135. The KD32-AB consists of the memory controller module M7136 and the data path module M7135-YA. The memory controller module must always be placed in slot 1 and the data path module in slot 2.

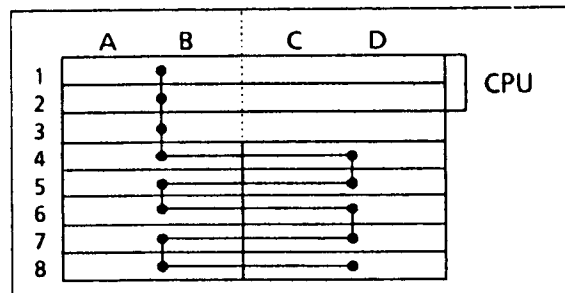
<sup>3</sup> Use 3.45 amps at +5 volts for the first installed MSV11-PK module. For each additional MSV11-PK module, use 3.0 amps at +5 volts.

<sup>4</sup> Use 3.6 amps at +5 volts for the first installed MSV11-PL module. For each additional MSV11-PL module, use 3.1 amps at +5 volts.

<sup>5</sup> The RQDX1 module must be installed if the system has any of the disk or diskette drives (RD51, RD51-D/-R, RD52, RD52-D/-R, RX50).

<sup>6</sup> The RQDX1-E module must be installed if the system has any of these drives: RD51-D or -R, or RD52-D or -R.

### MicroVAX I Q22 Bus Priority



Master System Configuration Worksheet

Slot Numbers

1 two quads = KD32-AA or KD32-AB

2

3 memory

4 1 quad or 2 doubles

5 1 quad or 2 doubles

6 1 quad or 2 doubles

7 1 quad or 2 doubles

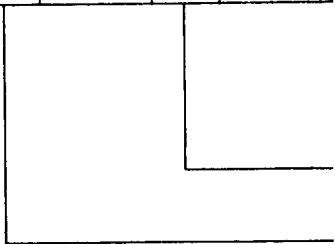
8 1 quad or 2 doubles

disk unit #1

disk unit #2

Option	Current (amps)			
	+ 5		+ 12	
	used	available	used	available
Maximum	—	36.0	—	7.0
CPU	12.0	22.0	0.5	6.5
MSV11-PL	3.6	18.4	0.0	6.5

AC Bus Loads		Panel Inserts			
		2 x 3		1 x 4	
used	available	used	available	used	available
—	29.0	—	4 or 2	—	2 or 5
4.0	25.0	1	3 or 1	—	2 or 5
2.0	23.0	—	3 or 1	—	2 or 5



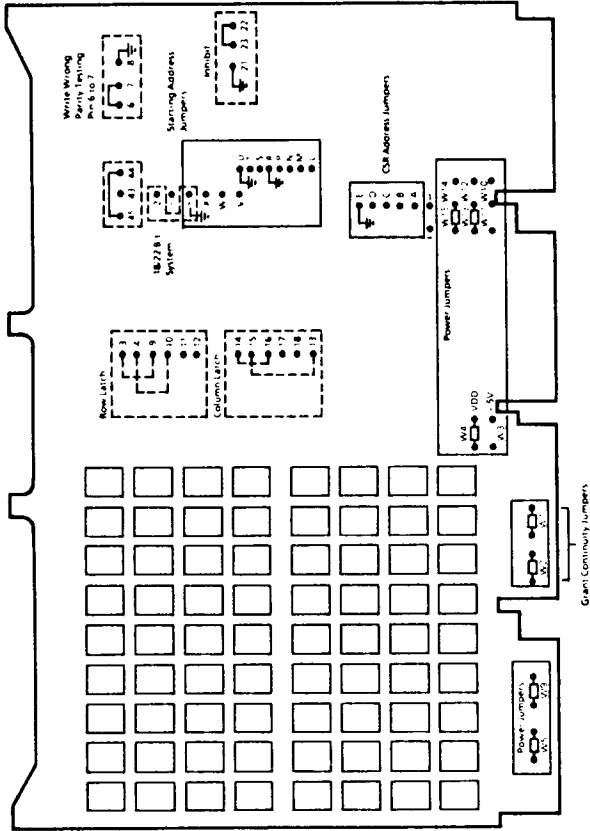
Total of this column x 12 =  watts at 12 V

Total of this column x 5 =  watts at 5 V

---

Total watts (must be 230 or less)

# MSV11-P Module



## MSV11-P Bus Grant Continuity Jumpers

Backplane Slot Configuration	W1	W2
QBUS/QBUS	in	in
Q22/Q22	in	in
QBUS/CD*	out	out
Q22/CD*	out	out

\*These jumper settings are valid unless this slot is the last CD slot

# Jumper List for MSV11-PL and MSV11-PK

Jumper Name or Pin to Pin	Jumper's Factory Setting	Wire Wrap or Solder	Function
6 to 7	in	WW	jumper in: write wrong parity
8 to 7	out	WW	jumper in: disables wrong parity
2 to Y	out	WW	jumper in: 18-bit machine jumper out: 22-bit machine
43 to 44	out	WW	jumper in: single voltage MOS RAM access time (150 ns device)
45 to 44	in	WW	jumper in: multiple voltage MOS RAM access time (200 ns device)
22 to 23	in	WW	not used
21 to 23	out	WW	not used
F to H	out	WW	jumper in: forces starting address to 16K jumper out: disables force function
3 to 9, 13 to 15	in in	WW WW	connected on 16K and 64K MOS chip
4 to 10, 14 to 16	in in	WW WW	connected only on 64K MOS chip
W3, W11	out	S	power for 16K chips
W13	in	S	power for 16K and 64K chips
W4, W5, W9,	in	S	power for 64K chips
W13, W15	in	S	
W1, W2	in	S	bus grant continuity
A, B, C, D, E	out	WW	CSR address; pin E is ground
X, W, V, Y	out	WW	module starting address;
P, N, M,	out	WW	pins Y and R are ground
L, T, R	out	WW	

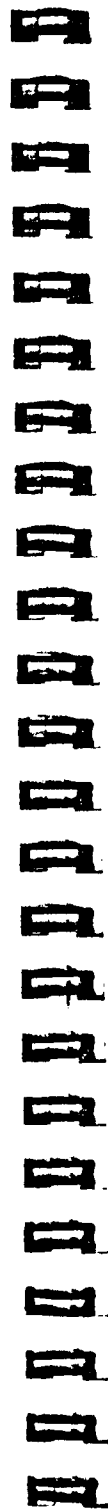
**MSV11-P CSR Address Selection**

Module Number	QBUS Address (octal)	Wire Wrap Pins
1	772100	no wire wraps
2	772102	wire wrap pin A to pin E
3	772104	wire wrap pin B to pin E
4	772106	wire wrap A to B, then B to E
5	772110	wire wrap pin C to pin E
6	772112	wire wrap A to C, then C to E
7	772114	wire wrap B to C, then C to E
8	772116	wire wrap A to B, B to C, then C to E
9	772120	wire wrap pin D to pin E
10	772122	wire wrap A to D, then D to E
11	772124	wire wrap B to D, then D to E
12	772126	wire wrap A to B, B to D, then D to E
13	772130	wire wrap C to D, then D to E
14	772132	wire wrap A to C, C to D, then D to E
15	772134	wire wrap B to C, C to D, then D to E
16	772136	wire wrap A to B, B to C, C to D, then D to E

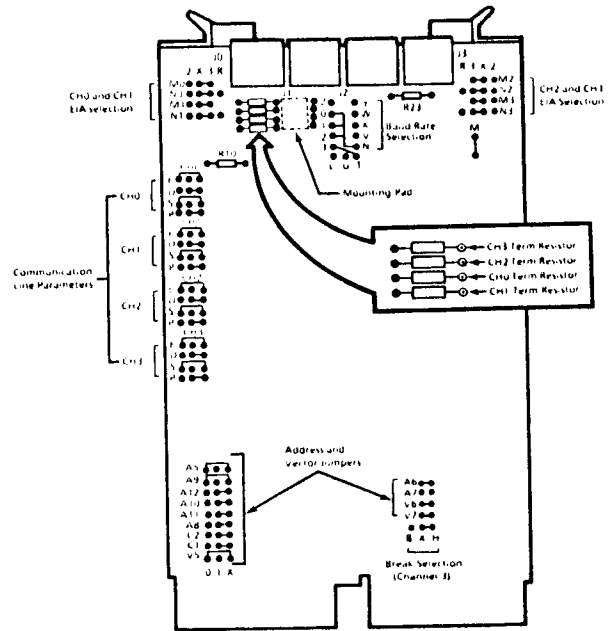
**Note:** Presently, six is the maximum number of memory modules that can be installed in a MicroVAX I system. This would provide a maximum of 3 Mb (3072 Kb) of memory, but the system would not have any disk or diskette drives as there would be no room in the backplane for the RQDX1 controller module. Four is the maximum number of memory modules for a system with disk and diskette drives; this provides up to 2 Mb (2048 Kb) of memory.

**Memory Module Jumpers**

Kb of Memory Currently Installed	Wire Wrap Pins
0	none
256	P to R
512	V to Y
768	V to Y, and P to R
1024	W to Y
1280	W to Y, and P to R
1536	V to W then W to Y
1792	V to W then W to Y, and P to R
2048	X to Y
2304	X to Y, and P to R
2560	V to X then X to Y



**DLVJ1 Module**



- Before installing a DLVJ1 in a MicroVAX I, you must:**
- 1 Remove the X to 1 wire wraps from jumpers C1 and C2. Install wire wraps from X to 0 on C1 and C2.
  - 2 Remove the BREAK jumper wire wrap from X to H.
  - 3 Remove the X to 0 wire wrap from jumper V5.

### Jumper List for DLVJ1 Communications Module

Jumper Label	Factory Setting	Function
C1, C2	X to 1	These jumpers enable channel 3 as the console device.
BREAK	X to H	This jumper enables the BREAK key on the console device connected to channel 3
A12, A11, A10, A8, A9, A5, A7	X to 1 X to 1 X to 0 jumper removed	This arrangement of jumpers A5 through A12 implements the octal base device address 7765XX (the high-order five bits are supplied as ones by the bank 7 select signal on the Q22 bus)
A6	jumper installed	
V7, V6, V5	jumper installed X to 0	This arrangement of jumpers V5 through V7 implements the octal base vector of 300, with channel 3 at 60 and 64
E, D, S, P	X to 0 X to 1 X to 0 X to 1	Jumpers E, D, S, and P determine the word format used by the four channels. There is one set of E, D, S and P jumpers for each channel. odd parity enabled eight data bits one stop bit no parity
0, 1, 2, 3	0 to N 1 to N 2 to N 3 to T	Jumpers 0, 1, 2, and 3 select the baud rate for each of the four channels. If more than one channel requires the same baud rate, daisy chain the wire wrap pins. 9600 baud 9600 baud 9600 baud 300 baud
M0-M3, N0-N3	X to 3 X to 3	These jumpers determine the EIA standard compatibility of the channels. All channels are set at the factory to be compatible with EIA RS-423 and RS-232C simultaneously.
R10	22K ohms	Channels 0 and 1 slew rate of 2 μs (used for EIA RS-423/232C).
R23	22K ohms	Channels 2 and 3 slew rate of 2 μs (used for EIA RS-423/232C)

### DLVJ1 Device Address Assignments

Address (octal)	Device Register
module base address (BA):	
BA = 776500	channel 0 RCSR
BA + 2 = 776502	channel 0 RBUF
BA + 4 = 776504	channel 0 XCSR
BA + 6 = 776506	channel 0 XBUF
BA + 10 = 776510	channel 1 RCSR
BA + 12 = 776512	channel 1 RBUF
BA + 14 = 776514	channel 1 XCSR
BA + 16 = 776516	channel 1 XBUF
BA + 20 = 776520	channel 2 RCSR
BA + 22 = 776522	channel 2 RBUF
BA + 24 = 776524	channel 2 XCSR
BA + 26 = 776526	channel 2 XBUF
BA + 30 = 776530	channel 3 RCSR
BA + 32 = 776532	channel 3 RBUF
BA + 34 = 776534	channel 3 XCSR
BA + 36 = 776536	channel 3 XBUF

### DLVJ1 Vector Assignments

Vectors (octal)	Interrupt Vector
module base vector (BV):	
BV = 300	channel 0 receiver
BV + 4 = 304	channel 0 transmitter
BV + 10 = 310	channel 1 receiver
BV + 14 = 314	channel 1 transmitter
BV + 20 = 320	channel 2 receiver
BV + 24 = 324	channel 2 transmitter
BV + 30 = 330	channel 3 receiver
BV + 34 = 334	channel 3 transmitter

### DLVJ1 Line Parameter Jumpers

Label	Parameter	Wirewrap Connection	
		X to 0	X to 1
D	number of data bits	7 bits	8 bits
S	number of stop bits	1 bit	2 bits
P	parity inhibit	parity generation and detection enabled	parity generation and detection disabled
E	even parity	odd parity enabled	even parity enabled

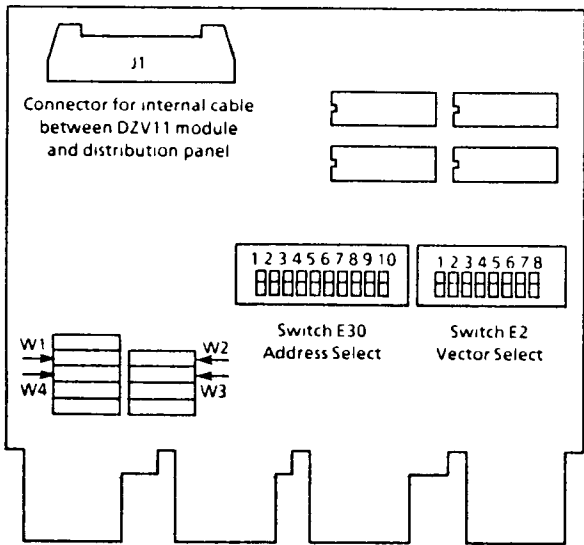
**DLVJ1 Baud Rate Pins**

Baud Rate Pin Label	Baud Rate
U	150
T	300
V	600
W	1200
Y	2400
L	4800
N	9600
K	19200
Z	38400

**DLVJ1 EIA Selection Jumpers**

Jumpers	EIA RS-422	EIA RS-232C/423
M0-M3	Wire wrap pin X to pin 2 for each M jumper	Wire wrap pin X to pin 3 for each M jumper
N0-N3	Wire wrap pin X to pin 2 for each N jumper	Wire wrap pin X to pin 3 for each N jumper

**DZV11 Module**



**DZV11 Address Switches**

Module	Address (octal)	Switch Numbers					
		1-6	7	8	9	10	
As shipped	760010	off	off	off	off	off	on
First installed	760100	off	on	off	off	off	off
Second installed	760110	off	on	off	off	off	on
Thrd installed	760120	off	on	off	on	on	on

**DZV11 Vector Switches**

Vector	E2 Switches					
	1	2	3	4	5	6
300*	off	on	on	off	off	off
310	off	on	on	off	off	on
320	off	on	on	off	on	off
330	off	on	on	off	on	on
340	off	on	on	on	off	off
350	off	on	on	on	off	on
360	off	on	on	on	on	off
370	off	on	on	on	on	on
400	on	off	off	off	off	off
410	on	on	on	off	off	on
420	on	on	on	off	on	off

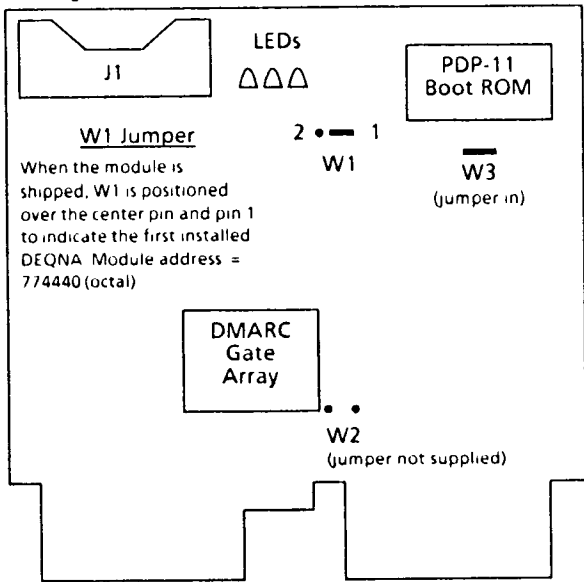
\*Vector switches set to 300 at factory

**DZV11 Vector Usage**

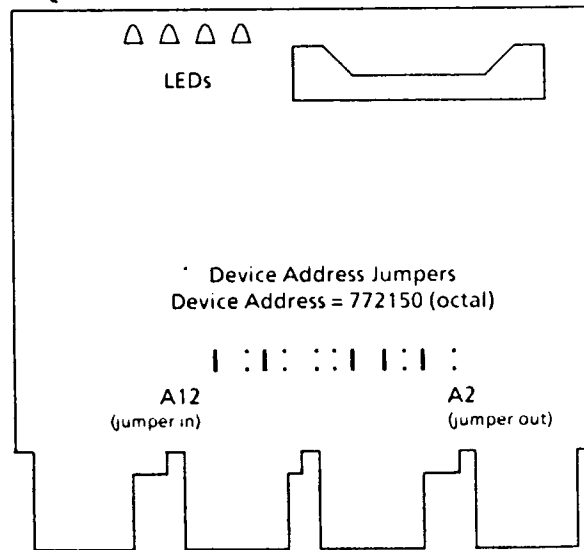
Quantity of DZV11(s)	Quantity of DLVJ1(s)	Use Vector
1	0	300*
2	0	310
3	0	320
1	1	340
2	1	350
3	1	360
1	2	400
2	2	410
3	2	420

\*Vector switches set to 300 at factory

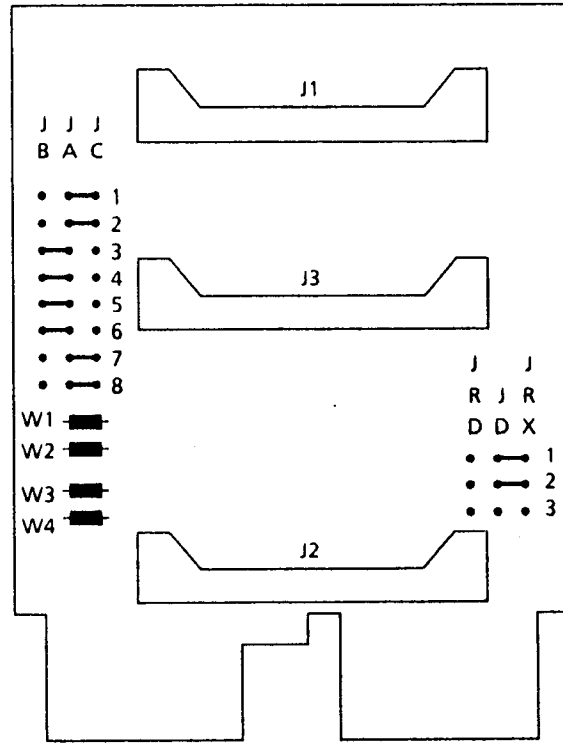
### DEQNA Module



### RQDX1 Module



### RQDX1-E



### RQDX1-E Bus Extender Module Jumpers

Jumpers	Functions	Factory Configuration
W1 - W4	Manufacturing use only	Must be installed
JRD/JD/JRX	Factory set, do not change.	JD1 to JRX1 JD2 to JRX2
JB/JA/JC	Determine which connector (J2 or J3) the RD read/write will connect to.	JA1 to JC1 JA2 to JC2 JA3 to JB3 JA4 to JB4 JA5 to JB5 JA6 to JB6 JA7 to JC7 JA8 to JC8

## MicroVAX Instruction Set

Mnemonic	Opcode	Description
ACBB	9D	Add compare and branch byte
<sup>1</sup> ACBD	6F	Add compare and branch D_floating
<sup>2</sup> ACBF	4F	Add compare and branch F_floating
<sup>3</sup> ACBG	4FFD	Add compare and branch G_floating
<sup>4</sup> ACBH	6FFD	Add compare and branch H_floating
ACBL	F1	Add compare and branch longword
ACBW	3D	Add compare and branch word
ADAWI	58	Add aligned word interlocked
ADDB2	80	Add byte 2-operand
ADDB3	81	Add byte 3-operand
<sup>1</sup> ADDD2	60	Add D_floating 2-operand
<sup>1</sup> ADDD3	61	Add D_floating 3-operand
<sup>2</sup> ADDF2	40	Add F_floating 2-operand
<sup>2</sup> ADDF3	41	Add F_floating 3-operand
<sup>3</sup> ADDG2	40FD	Add G_floating 2-operand
<sup>3</sup> ADDG3	41FD	Add G_floating 3-operand
<sup>4</sup> ADDH2	60FD	Add H_floating 2-operand
<sup>4</sup> ADDH3	61FD	Add H_floating 3-operand
ADDL2	C0	Add longword 2-operand
ADDL3	C1	Add longword 3-operand
<sup>5</sup> ADDP4	20	Add packed 4-operand
<sup>5</sup> ADDP6	21	Add packed 6-operand
ADDW2	A0	Add word 2-operand
ADDW3	A1	Add word 3-operand
ADWC	06	Add with carry

<sup>1</sup> This instruction generates a reserved instruction fault in the KD32-AA processor. The KD32-AB processor implements this instruction in hardware.

<sup>2</sup> The MicroVAX architecture specifies this as an emulated instruction, but both MicroVAX I processors implement it in hardware.

<sup>3</sup> This instruction generates a reserved instruction fault in the KD32-AB processor. The KD32-AA processor implements this instruction in hardware.

<sup>4</sup> This instruction generates a reserved instruction fault in both MicroVAX I processors.

<sup>5</sup> This instruction generates an instruction emulation exception in both MicroVAX I processors.



Mnemonic	Opcode	Description
AOBLEQ	F3	Add one and branch on less or equal
AOBLSS	F2	Add one and branch on less
ASHL	78	Arithmetic shift longword
5 ASHP	F8	Arithmetic shift and round packed
ASHQ	79	Arithmetic shift quad
BBC	E1	Branch on bit clear
BBCC	E5	Branch on bit clear and clear
BBCCI	E7	Branch on bit clear and clear interlocked
BBCS	E3	Branch on bit clear and set
BBS	E0	Branch on bit set
BBSC	E4	Branch on bit set and clear
BBSS	E2	Branch on bit set and set
BBSSI	E6	Branch on bit set and set interlocked
BCC	1E	Branch on carry clear
BCS	1F	Branch on carry set
BEQL	13	Branch on equal
BEQLU	13	Branch on equal unsigned
BGEQ	18	Branch on greater or equal
BGEQU	1E	Branch on greater or equal unsigned
BGTR	14	Branch on greater
BGTRU	1A	Branch on greater unsigned
BICB2	8A	Bit clear byte 2-operand
BICB3	8B	Bit clear byte 3-operand
BICL2	CA	Bit clear longword 2-operand
BICL3	CB	Bit clear longword 3-operand
BICPSW	B9	Bit clear processor status word
BICW2	AA	Bit clear word 2-operand
BICW3	AB	Bit clear word 3-operand
BISB2	88	Bit set byte 2-operand
BISB3	89	Bit set byte 3-operand
BISL2	C8	Bit set longword 2-operand
BISL3	C9	Bit set longword 3-operand
BISPSW	BB	Bit set processor status word
BISW2	A8	Bit set word 2-operand
BISW3	A9	Bit set word 3-operand
BITB	93	Bit test byte
BITL	D3	Bit test longword

Mnemonic	Opcode	Description
BITW	B3	Bit test word
BLBC	E9	Branch on low bit clear
BLBS	E8	Branch on low bit set
BLEQ	15	Branch on less or equal
BLEQU	1B	Branch on less or equal unsigned
BLSS	19	Branch on less
BLSSU	1F	Branch on less unsigned
BNEQ	12	Branch on not equal
BNEQU	12	Branch on not equal unsigned
BPT	03	Break point fault
BRB	11	Branch with byte displacement
BRW	31	Branch with word displacement
BSBB	10	Branch to subroutine with byte displacement
BSBW	30	Branch to subroutine with word displacement
BUGL	F0FF	VMS bugcheck
BUGW	F0FF	VMS bugcheck
BVC	1C	Branch on overflow clear
BVS	1D	Branch on overflow set
CALLG	FA	Call with general argument list
CALLS	FB	Call with argument list on stack
CASEB	8F	Case byte
CASEL	CF	Case longword
CASEW	AF	Case word
CHME	BD	Change mode to executive
CHMK	BC	Change mode to kernel
CHMS	BE	Change mode to supervisor

<sup>1</sup> This instruction generates a reserved instruction fault in the KD32-AA processor. The KD32-AB processor implements this instruction in hardware.

<sup>2</sup> The MicroVAX architecture specifies this as an emulated instruction, but both MicroVAX I processors implement it in hardware.

<sup>3</sup> This instruction generates a reserved instruction fault in the KD32-AB processor. The KD32-AA processor implements this instruction in hardware.

<sup>4</sup> This instruction generates a reserved instruction fault in both MicroVAX I processors.

<sup>5</sup> This instruction generates an instruction emulation exception in both MicroVAX I processors.

Mnemonic	Opcode	Description
CHMU	BF	Change mode to user
CLRB	94	Clear byte
<sup>1</sup> CLRD	7C	Clear D-floating
<sup>2</sup> CLRF	D4	Clear F-floating
<sup>3</sup> CLRG	7C	Clear G-floating
<sup>4</sup> CLRH	7CFD	Clear H-floating
CLRL	D4	Clear longword
<sup>5</sup> CLRO	7CFD	Clear octaword
CLRQ	7C	Clear quad
CLRW	B4	Clear word
CMPB	91	Compare byte
<sup>2</sup> CMPC3	29	Compare character 3-operand
<sup>5</sup> CMPCS	2D	Compare character 5-operand
<sup>1</sup> CPMD	71	Compare D-floating
<sup>2</sup> CMPF	51	Compare F-floating
<sup>3</sup> CMPG	51FD	Compare G-floating
<sup>4</sup> CMPH	71FD	Compare H-floating
CMPL	D1	Compare longword
<sup>5</sup> CMPP3	35	Compare packed 3-operand
<sup>5</sup> CMPP4	37	Compare packed 4-operand
CMPV	EC	Compare field
CMPW	B1	Compare word
CMPZV	ED	Compare zero-extended field
<sup>5</sup> CRC	0B	Calculate cyclic redundancy check
<sup>1</sup> CVTBD	6C	Convert byte to D-floating
<sup>2</sup> CVTBF	4C	Convert byte to F-floating
<sup>3</sup> CVTBG	4CFD	Convert byte to G-floating
<sup>4</sup> CVTBH	6CFD	Convert byte to H-floating
CVTBL	98	Convert byte to longword
CVTBW	99	Convert byte to word
<sup>1</sup> CVTDB	68	Convert D-floating to byte
<sup>1</sup> CVTDF	76	Convert D-floating to F-floating
<sup>4</sup> CVTDH	32FD	Convert D-floating to H-floating
<sup>1</sup> CVTDL	6A	Convert D-floating to longword
<sup>1</sup> CVTDW	69	Convert D-floating to word
<sup>2</sup> CVTFB	48	Convert F-floating to byte
<sup>1</sup> CVTFD	56	Convert F-floating to D-floating
<sup>3</sup> CVTFG	99FD	Convert F-floating to G-floating

Mnemonic	Opcode	Description
<sup>4</sup> CVTFH	98FD	Convert F-floating to H-floating
<sup>2</sup> CVTFL	4A	Convert F-floating to longword
<sup>2</sup> CVTFW	49	Convert F-floating to word
<sup>3</sup> CVTGB	48FD	Convert G-floating to byte
<sup>3</sup> CVTGF	33FD	Convert G-floating to F-floating
<sup>4</sup> CVTGH	56FD	Convert G-floating to H-floating
<sup>3</sup> CVTGL	4AFD	Convert G-floating to longword
<sup>3</sup> CVTGW	49FD	Convert G-floating to word
<sup>4</sup> CVTHB	68FD	Convert H-floating to byte
<sup>4</sup> CVTHD	F7FD	Convert H-floating to D-floating
<sup>4</sup> CVTHF	F6FD	Convert H-floating to F-floating
<sup>4</sup> CVTHG	76FD	Convert H-floating to G-floating
<sup>4</sup> CVTHL	6AFD	Convert H-floating to longword
<sup>4</sup> CVTHW	69FD	Convert H-floating to word
CVTLB	F6	Convert longword to byte
<sup>1</sup> CVTLD	6E	Convert longword to D-floating
<sup>2</sup> CVTLF	4E	Convert longword to F-floating
<sup>3</sup> CVTLG	4EFD	Convert longword to G-floating
<sup>4</sup> CVTLH	6EFD	Convert longword to H-floating
<sup>5</sup> CVTLP	F9	Convert longword to packed
CVTLW	F7	Convert longword to word
<sup>5</sup> CVTPL	36	Convert packed to longword
<sup>5</sup> CVTPS	0B	Convert packed to leading separate
<sup>5</sup> CVTPT	24	Convert packed to trailing
<sup>1</sup> CVTRDL	6B	Convert rounded D-floating to longword

<sup>1</sup> This instruction generates a reserved instruction fault in the KD32-AA processor. The KD32-AB processor implements this instruction in hardware.

<sup>2</sup> The MicroVAX architecture specifies this as an emulated instruction, but both MicroVAX I processors implement it in hardware.

<sup>3</sup> This instruction generates a reserved instruction fault in the KD32-AB processor. The KD32-AA processor implements this instruction in hardware.

<sup>4</sup> This instruction generates a reserved instruction fault in both MicroVAX I processors.

<sup>5</sup> This instruction generates an instruction emulation exception in both MicroVAX I processors.

Mnemonic	Opcode	Description
<sup>2</sup> CVTRFL	4B	Convert rounded F-floating to longword
<sup>3</sup> CVTRGL	4BFD	Convert rounded G-floating to longword
<sup>4</sup> CVTRHL	6BFD	Convert rounded H-floating to longword
<sup>5</sup> CVTSP	09	Convert leading separate to packed
<sup>5</sup> CVTTP	26	Convert trailing to packed
CVFWB	33	Convert word to byte
<sup>1</sup> CVTWD	6D	Convert word to D-floating
<sup>2</sup> CVTWF	4D	Convert word to F-floating
<sup>3</sup> CVTWG	4DFD	Convert word to G-floating
<sup>4</sup> CVTWH	6DFD	Convert word to H-floating
CVTWL	32	Convert word to longword
DECB	97	Decrement byte
DECL	D7	Decrement longword
DECW	B7	Decrement word
DIVB2	86	Divide byte 2-operand
DIVB3	87	Divide byte 3-operand
<sup>1</sup> DIVD2	66	Divide D-floating 2-operand
<sup>1</sup> DIVD3	67	Divide D-floating 3-operand
<sup>2</sup> DIVF2	46	Divide F-floating 2-operand
<sup>2</sup> DIVF3	47	Divide F-floating 3-operand
<sup>3</sup> DIVG2	46FD	Divide G-floating 2-operand
<sup>3</sup> DIVG3	47FD	Divide G-floating 3-operand
<sup>4</sup> DIVH2	66FD	Divide H-floating 2-operand
<sup>4</sup> DIVH3	67FD	Divide H-floating 3-operand
DIVL2	C6	Divide longword 2-operand
DIVL3	C7	Divide longword 3-operand
<sup>5</sup> DIVP	27	Divide packed
DIVW2	A6	Divide word 2-operand
DIVW3	A7	Divide word 3-operand
<sup>5</sup> EDITPC	38	Edit packed to character string
EDIV	7B	Extended divide
<sup>1</sup> EMODD	74	Extended modulus D-floating
<sup>2</sup> EMODF	54	Extended modulus F-floating
<sup>3</sup> EMODG	54FD	Extended modulus G-floating
<sup>4</sup> EMODH	74FD	Extended modulus H-floating
EMUL	7A	Extended multiply



Mnemonic	Opcode	Description
ESCD	FD	Escape D
ESCE	FE	Escape E
ESCF	FF	Escape F
EXTV	EE	Extract field
EXTZV	EF	Extract zero-extended field
FFC	EB	Find first clear bit
FFS	EA	Find first set bit
HALT	00	Halt (kernel mode only)
INCB	96	Increment byte
INCL	D6	Increment longword
INCW	B6	Increment word
INDEX	0A	Index calculation
INSQHI	5C	Insert at head of queue, interlocked
INSQTI	5D	Insert at tail of queue, interlocked
INSQUE	0E	Insert into queue
INSV	F0	Insert field
JMP	17	Jump
JSB	16	Jump to subroutine
LDPCTX	06	Load process context (only legal on interrupt stack)
<sup>2</sup> LOCC	3A	Locate character
<sup>5</sup> MATCHC	39	Match characters
MCOMB	92	Move complemented byte
MCOML	D2	Move complemented longword
MCOMW	B2	Move complemented word
MFPR	DB	Move from processor register (kernel mode only)
MNEGB	8E	Move negated byte

<sup>1</sup> This instruction generates a reserved instruction fault in the KD32-AA processor. The KD32-AB processor implements this instruction in hardware.

<sup>2</sup> The MicroVAX architecture specifies this as an emulated instruction, but both MicroVAX I processors implement it in hardware.

<sup>3</sup> This instruction generates a reserved instruction fault in the KD32-AB processor. The KD32-AA processor implements this instruction in hardware.

<sup>4</sup> This instruction generates a reserved instruction fault in both MicroVAX I processors.

<sup>5</sup> This instruction generates an instruction emulation exception in both MicroVAX I processors.

Mnemonic	Opcode	Description
1 MNEGD	72	Move negated D-floating
2 MNEGF	52	Move negated F-floating
3 MNEGG	52FD	Move negated G-floating
4 MNEGH	72FD	Move negated H-floating
MNEGL	CE	Move negated longword
MNEGW	AE	Move negated word
MOVAB	9E	Move address of byte
1 MOVAD	7E	Move address of D-floating
2 MOVAF	DE	Move address of F-floating
3 MOVAG	7E	Move address of G-floating
4 MOVAH	7EFD	Move address of H-floating
MOVAL	DE	Move address of longword
5 MOVAO	7EFD	Move address of octaword
MOVAQ	7E	Move address of quadword
MOVAV	3E	Move address of word
MOVB	90	Move byte
MOVCB	28	Move character 3-operand
MOVCS	2C	Move character 5-operand
1 MOVDB	70	Move D-floating
2 MOVFB	50	Move F-floating
3 MOVGB	50FD	Move G-floating
4 MOVHB	70FD	Move H-floating
MOVL	D0	Move longword
5 MOVOD	7DFD	Move octaword
5 MOVOP	34	Move packed
MOVPSL	DC	Move processor status longword
MOVQ	7D	Move quadword
5 MOVTC	2E	Move translated characters
5 MOVTC	2F	Move translated until character
MOVW	B0	Move word
MOVZBL	9A	Move zero-extended byte to longword
MOVZBW	9B	Move zero-extended byte to word
MOVZWL	3C	Move zero-extended word to longword
MTPR	DA	Move to processor register (kernel mode only)
MULB2	84	Multiply byte 2-operand
MULB3	85	Multiply byte 3-operand
1 MULD2	64	Multiply D-floating 2-operand

Mnemonic	Opcode	Description
1 MULD3	65	Multiply D-floating 3-operand
2 MULF2	44	Multiply F-floating 2-operand
2 MULF3	45	Multiply F-floating 3-operand
3 MULG2	44FD	Multiply G-floating 2-operand
3 MULG3	45FD	Multiply G-floating 3-operand
4 MULH2	64FD	Multiply H-floating 2-operand
4 MULH3	65FD	Multiply H-floating 3-operand
MULL2	C4	Multiply longword 2-operand
MULL3	C5	Multiply longword 3-operand
5 MULP	25	Multiply packed
MULW2	A4	Multiply word 2-operand
MULW3	A5	Multiply word 3-operand
NOP	01	No operation
1 POLYD	75	Evaluate polynomial D-floating
2 POLYF	55	Evaluate polynomial F-floating
3 POLYG	55FD	Evaluate polynomial G-floating
4 POLYH	75FD	Evaluate polynomial H-floating
POPR	BA	Pop registers
PROBER	0C	Probe read access
PROBEW	0D	Probe write access
PUSHAB	9F	Push address of byte
1 PUSHAD	7F	Push address of D-floating
2 PUSHAF	DF	Push address of F-floating
3 PUSHAG	7F	Push address of G-floating
4 PUSHAH	7FFD	Push address of H-floating
PUSHAL	DF	Push address of longword

1 This instruction generates a reserved instruction fault in the KD32-AA processor. The KD32-AB processor implements this instruction in hardware.

2 The MicroVAX architecture specifies this as an emulated instruction, but both MicroVAX 1 processors implement it in hardware.

3 This instruction generates a reserved instruction fault in the KD32-AB processor. The KD32-AA processor implements this instruction in hardware.

4 This instruction generates a reserved instruction fault in both MicroVAX 1 processors.

5 This instruction generates an instruction emulation exception in both MicroVAX 1 processors.

Mnemonic	Opcode	Description
<sup>5</sup> PUSHAO	7FFD	Push address of octaword
PUSHAQ	7F	Push address of quadword
PUSHAW	3F	Push address of word
PUSHL	DD	Push longword
PUSHR	BB	Push registers
REI	02	Return from exception or interrupt
REMQHI	5E	Remove from head of queue, interlocked
REMQTI	5F	Remove from tail of queue, interlocked
REMQE	0F	Remove from queue
RET	04	Return from procedure
ROTL	9C	Rotate longword
RSB	05	Return from subroutine
Reserved	57	Reserved
Reserved	5A	Reserved
Reserved	5B	Reserved
Reserved	77	Reserved
Reserved	FE	Reserved
Reserved	FF	Reserved
SBWC	D9	Subtract with carry
<sup>2</sup> SCANC	2A	Scan for character
<sup>2</sup> SKPC	3B	Skip character
SOBGEQ	F4	Subtract one and branch on greater or equal
SOBGTR	F5	Subtract one and branch on greater
<sup>2</sup> SPANC	2B	Span characters
SUBB2	82	Subtract byte 2-operand
SUBB3	83	Subtract byte 3-operand
<sup>1</sup> SUBD2	62	Subtract D-floating 2-operand
<sup>1</sup> SUBD3	63	Subtract D-floating 3-operand
<sup>2</sup> SUBF2	42	Subtract F-floating 2-operand
<sup>2</sup> SUBF3	43	Subtract F-floating 3-operand
<sup>3</sup> SUBG2	42FD	Subtract G-floating 2-operand
<sup>3</sup> SUBG3	43FD	Subtract G-floating 3-operand
<sup>4</sup> SUBH2	62FD	Subtract H-floating 2-operand
<sup>4</sup> SUBH3	63FD	Subtract H-floating 3-operand

Mnemonic	Opcode	Description
SUBL2	C2	Subtract longword 2-operand
SUBL3	C3	Subtract longword 3-operand
<sup>5</sup> SUBP4	22	Subtract packed 4-operand
<sup>5</sup> SUBP6	23	Subtract packed 6-operand
SUBW2	A2	Subtract word 2-operand
SUBW3	A3	Subtract word 3-operand
SVPCTX	07	Save process context (kernel mode only)
TSTB	95	Test byte
<sup>1</sup> TSTD	73	Test D-floating
<sup>2</sup> TSTF	53	Test F-floating
<sup>3</sup> TSTG	53FD	Test G-floating
<sup>4</sup> TSTH	73FD	Test H-floating
TSTL	D5	Test longword
TSTW	B5	Test word
XFC	FC	Extended function call
XORB2	8C	Exclusive OR byte 2-operand
XORB3	8D	Exclusive OR byte 3-operand
XORL2	CC	Exclusive OR longword 2-operand
XORL3	CD	Exclusive OR longword 3-operand
XORW2	AC	Exclusive OR word 2-operand
XORW3	AD	Exclusive OR word 3-operand

<sup>1</sup> This instruction generates a reserved instruction fault in the KD32-AA processor. The KD32-AB processor implements this instruction in hardware.

<sup>2</sup> The MicroVAX architecture specifies this as an emulated instruction, but both MicroVAX I processors implement it in hardware.

<sup>3</sup> This instruction generates a reserved instruction fault in the KD32-AB processor. The KD32-AA processor implements this instruction in hardware.

<sup>4</sup> This instruction generates a reserved instruction fault in both MicroVAX I processors.

<sup>5</sup> This instruction generates an instruction emulation exception in both MicroVAX I processors.

# Privileged Registers

Register Number	Register Name	Mnemonic	Type	Category
0	Kernel Stack Pointer	KSP	R/W	1
1	Executive Stack Pointer	ESP	R/W	1
2	Supervisor Stack Pointer	SSP	R/W	1
3	User Stack Pointer	USP	R/W	1
4	Interrupt Stack Pointer	ISP	R/W	1
5	Reserved			4
6	Reserved			4
7	Reserved			4
8	P0 Base Register	POBR	R/W	1
9	P0 Length Register	POLR	R/W	1
A	P1 Base Register	P1BR	R/W	1
B	P1 Length Register	P1LR	R/W	1
C	System Base Register	SBR	R/W	1
D	System Length Register	SLR	R/W	1
E	Reserved			4
F	Reserved			4
10	Process Control Block Base	PCBB	R/W	1
11	System Control Block Base	SCBB	R/W	1
12	Interrupt Priority Level	IPL	R/W	1
13	AST Level	ASTLVL	R/W	1
14	Software Interrupt Request	SIRR	W	1
15	Software Interrupt Summary	SISR	R/W	1
16	Reserved			4
17	CMI Error Register	CMERR		4
18	Interval Clock Control	ICCS	R/W	2
19	Next Interval Count	NICR	W	3
1A	Interval Count	ICR	R	3
1B	Time of Year	TODR	R/W	3
1C	Console Storage Receiver Status	CSRS	R/W	4
1D	Console Storage Receiver Data	CSRD	R	4
1E	Console Storage Transmit Status	CSTS	R/W	4
1F	Console Storage Transmit Data	CSTD	W	4

Category Key:

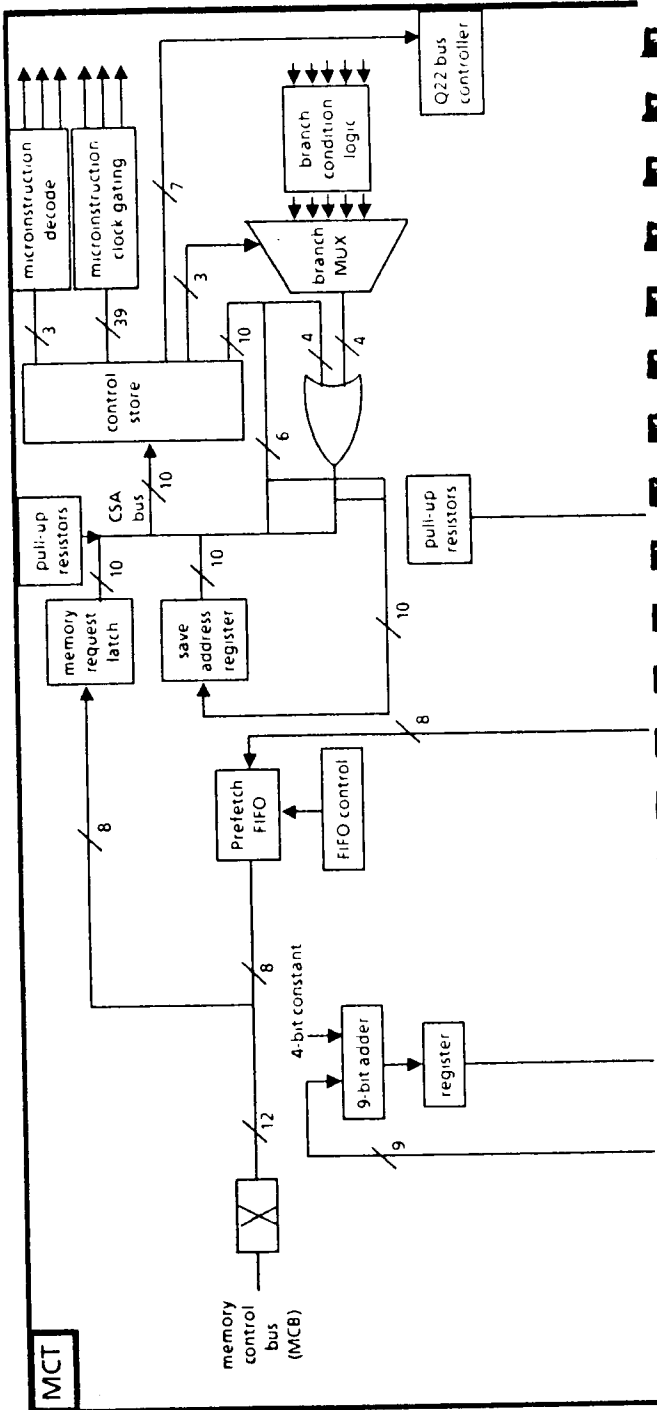
- 1 = implemented as defined by VAX architecture
- 2 = implemented by MicroVAX I uniquely
- 3 = read as zero, no operation on writes
- 4 = access not allowed; results in reserved operand fault

Register Number	Register Name	Mnemonic	Type	Category
20	Console Receive C/S	RXCS	R/W	1
21	Console Receive D/B	RXDB	R	1
22	Console Transmit C/S	TXCS	R/W	1
23	Console Transmit D/B	TXDB	W	1
24	Translation Buffer Disable	TBDR	R/W	3
25	Cache Disable	CADR	R/W	2
26	Machine Check Error Summary	MCESR	R/W	2
27	Cache Error	CAER	R/W	3
28	Accelerator Control/Status	ACCS		4
29	Accelerator Maintenance	ACCR		4
2A	Reserved			4
2B	Reserved			4
2C	Writable Control Store Address	WCSA		4
2D	Writable Control Store Data	WCSB		4
2E	Reserved			4
2F	Reserved			4
30	SBI Fault/Status	SBIFS	R/W	3
31	SBI Silo	SBIS	R	3
32	SBI Silo Comparator	SBISC	R/W	3
33	SBI Maintenance	SBIMT	R/W	3
34	SBI Error Register	SBIER	R/W	3
35	SBI Timeout Address	SBITA	R	3
36	SBI Quadword Clear	SBIQC	W	3
37	Initialize Bus	IORESET	W	2
38	Memory Management Enable	MAPEN	R/W	1
39	Translation Buffer Invalidate All	TBIA	W	1
3A	Translation Buffer Invalidate Single	TBIS	W	1
3B	Translation Buffer Data	TBDATA	R/W	3
3C	Microprogram Breakpoint	MBRK	R/W	3
3D	Performance Monitor Enable	PMR	R/W	3
3E	System Identification	SID	R	1
3F	Translation Buffer Check	TBCHK	W	1

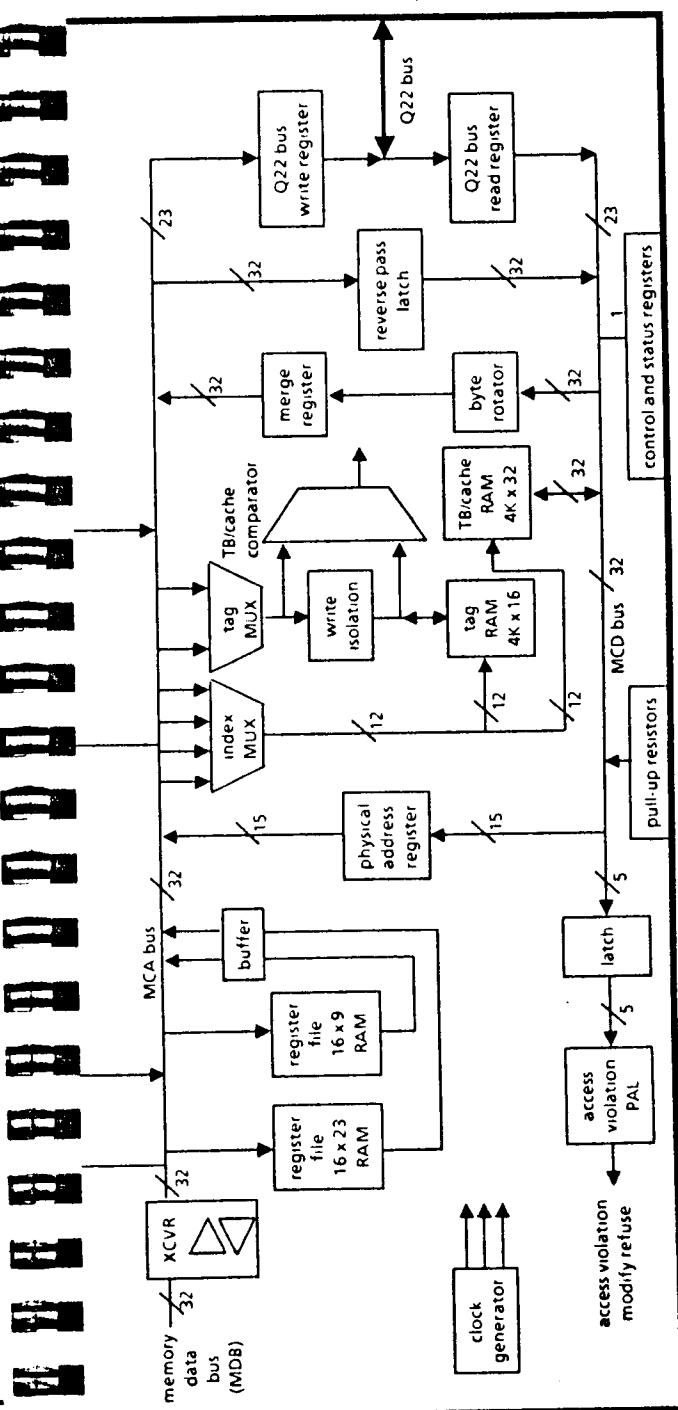
Category Key:

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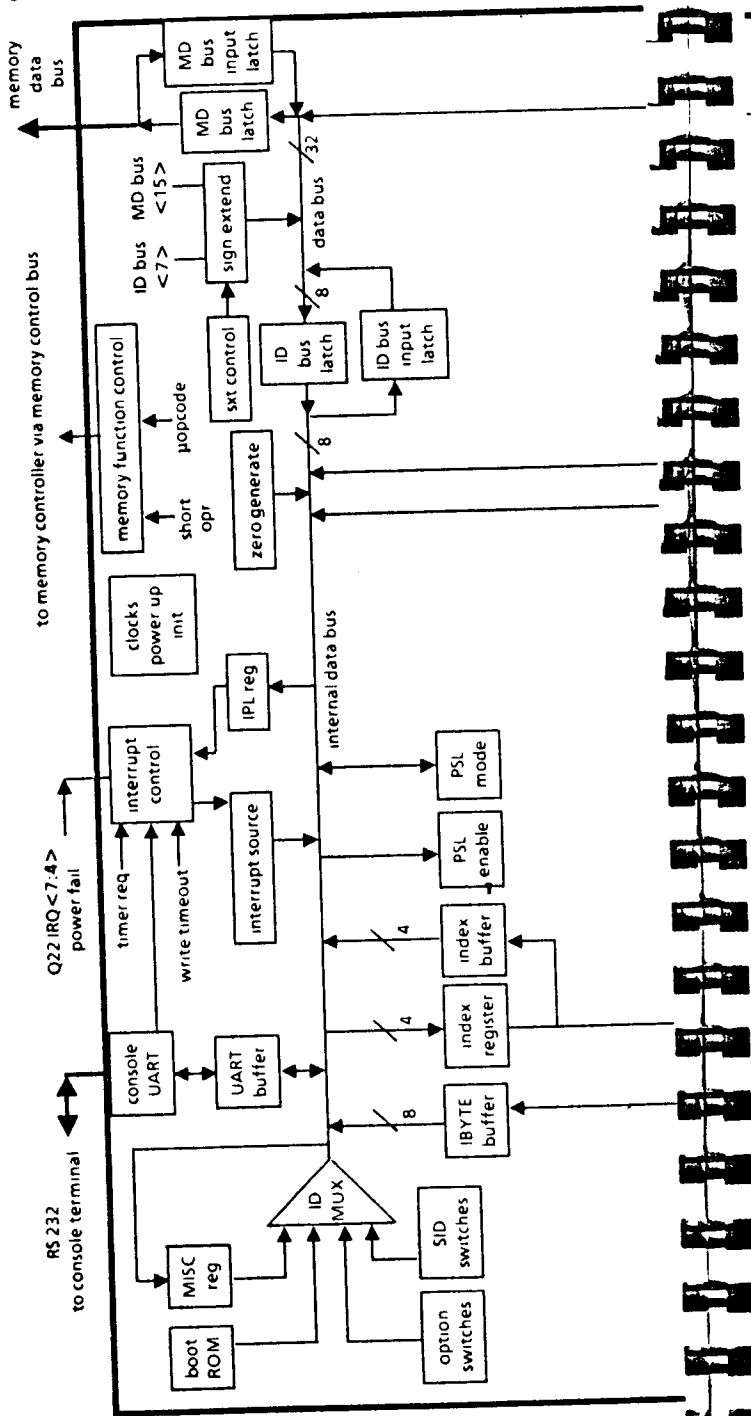
MCT Block Diagram 124



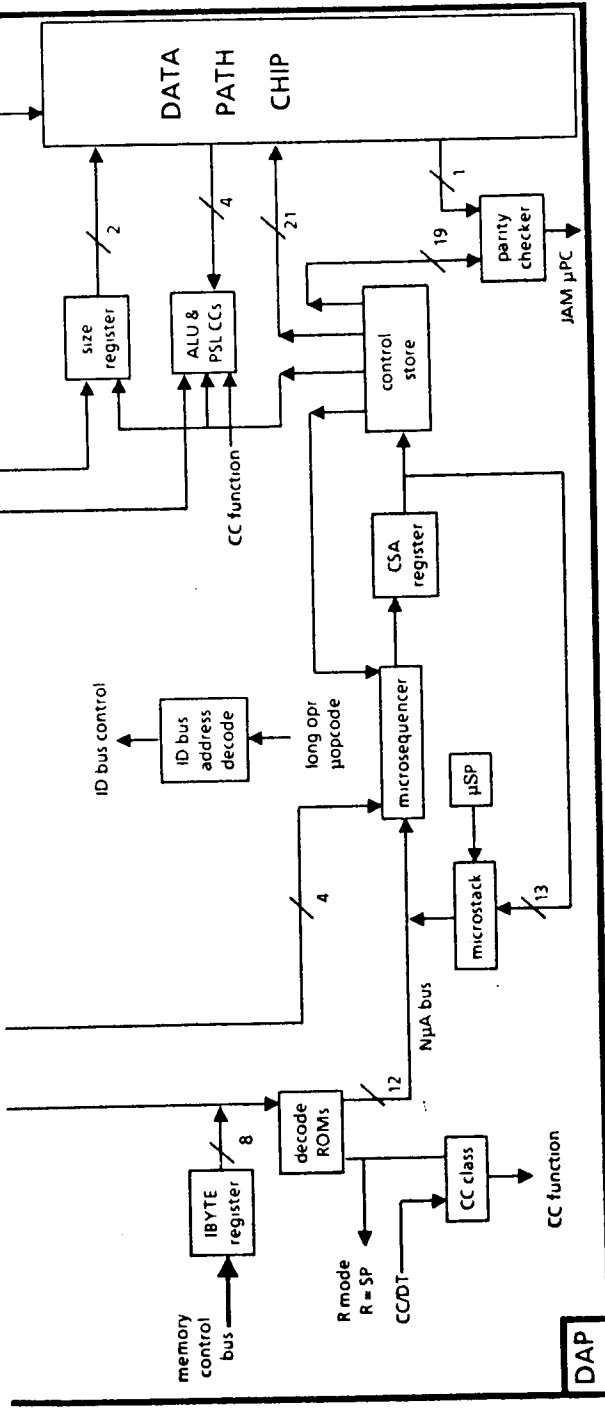
Memory Controller Block Diagram

125 MCT Block Diagram





DAP Block Diagram



DAP Block Diagram

Data Path Block Diagram

