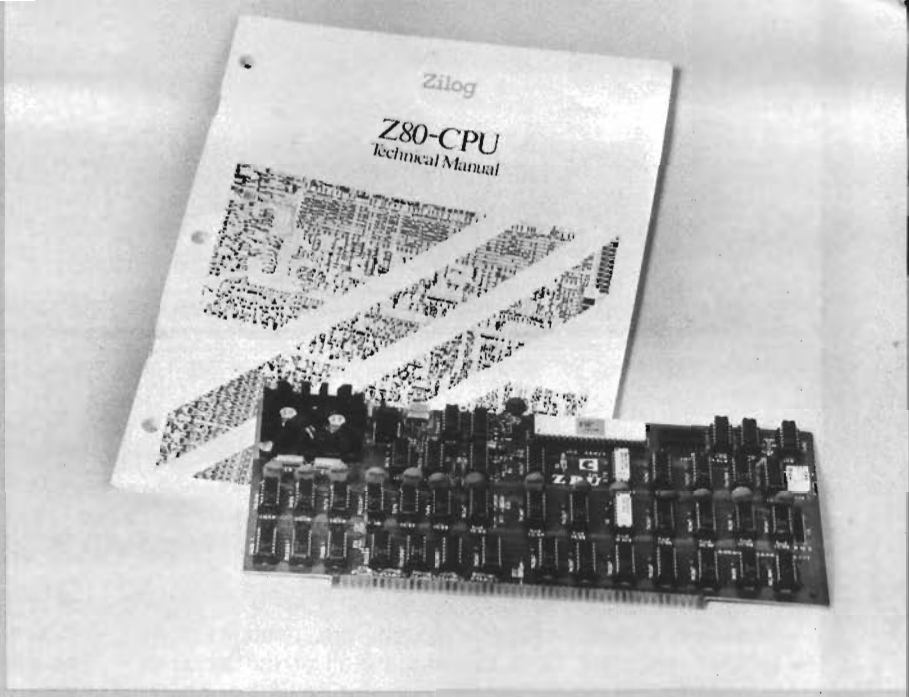
For most people the Z-80 chip signaled the start of another learning curve in microprocessor technology while others enjoyed the start of a whole new microcomputer revolution



CARD OF THE MONTH THE TDL ZPU™

By Roger Edelson, Hardware Editor

To be fair, this article should have run before my discussion of the other available S-100 bus compatible Z-80 CPU card. The reason is simple: TDL (Technical Design Labs) were out first with their Z-80 CPU board. So this month I will cover the Z-80 CPU card from TDL. I don't know which company, TDL or Sony owns the rights to the name ZPU, nor is my intention to compare the two boards, rather to confine myself to a discussion of the TDL entry. I must say, however, that either board would be a worthwhile addition to your computer.

Let us take a look at the TDL ZPU™ kit before we cover operation and design. The kit is particularly easy to build. My son who is fourteen years of age took about three hours - with time off for ice cream. The board worked the first time out. Assembly instructions are excellent, but please read the paragraph on the identification of the electrolytic capacitor lead polarity. One of the capacitors, C 20, is very strange. It has a single big black dot located in the middle of the two leads. When the dot faces you, the right lead is the positive one. Further on this subject, let me voice a minor gripe: the capacitor is not shown on the schematic diagram. In fact none of the regulator components is shown. This makes troubleshooting this area somewhat difficult. I hope TDL redraws their schematic to include these components.

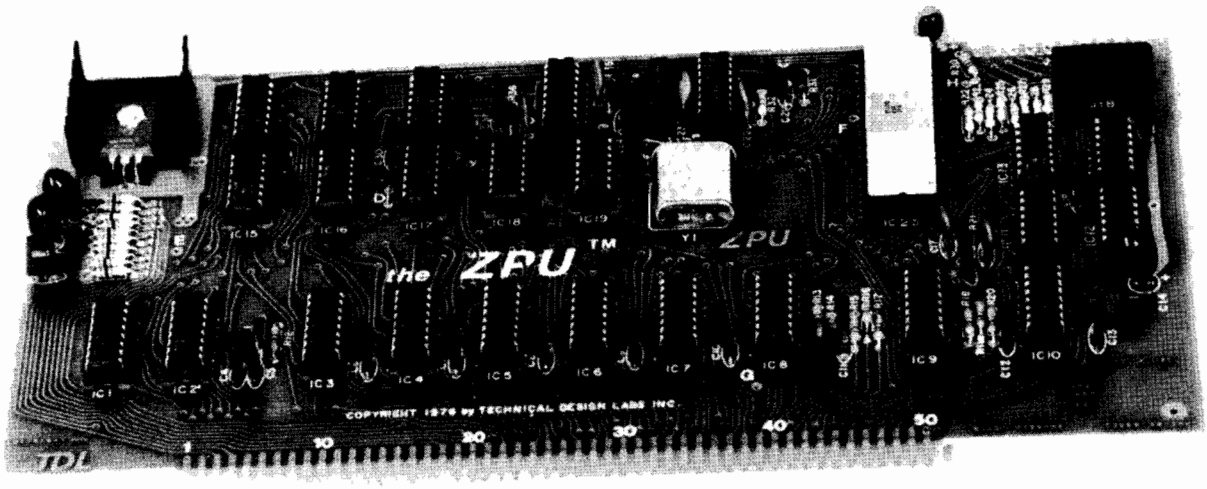
The printed circuit board is high quality with gold-plated edge-connector pins. Sockets are provided for all integrated circuits. A nice touch is the numbering of every tenth pin on the front of the board. The solder masking is generally adequate, but there were some outages on the board front. Where these occurred under a silk-screened component identification, the printing did not take. It is then difficult to read the component identification. With mine most of the resistor numbers on the left side of the board vanished and some identification on the top was also lost. That was a minor problem, but does not detract from the board's construction nor use.

The assembly of the board is straightforward and easy. The assembly instructions contain a particularly good section on the proper procedure for board cleaning. The card is designed to be compatible with the S-100 bus structure or the Altair/IMSAI front panel interconnection. Separate jacks are provided to accommodate the front panel connectors of either computer, and the ZPU user may elect to install either one or both during assembly.

Now let us take a look at the general board design and the specific features provided by TDL. As stated previously, the TDL ZPU ™ is S-100 bus compatible. In order to maintain this compatibility the ZPU must generate a number of bus signals not normally produced by the Z-80. The ZPU card produces these signals by logical interaction and gating of the Z-80's status signals and the clock lines.

The most important status generated by the Z-80 are:

1. Memory request
2. I/O Request
3. Read
4. Write
5. M1



The five signals, properly gated, are used in conjunction with the clock to generate all of the required control timing. To follow the description of the logical design of the ZPU, please refer to the schematic of the ZPU card shown on Figure 1.

The Z-80, unlike the 8080, outputs continuous status information whereas the 8080 information is strobed into an 8 bit latch (usually an 8212) during "Sync"time. Consequently, the Z-80 generates no sync pulse. In order to retain the Altair Bus structure, a "psuedo-sync pulse" was created.

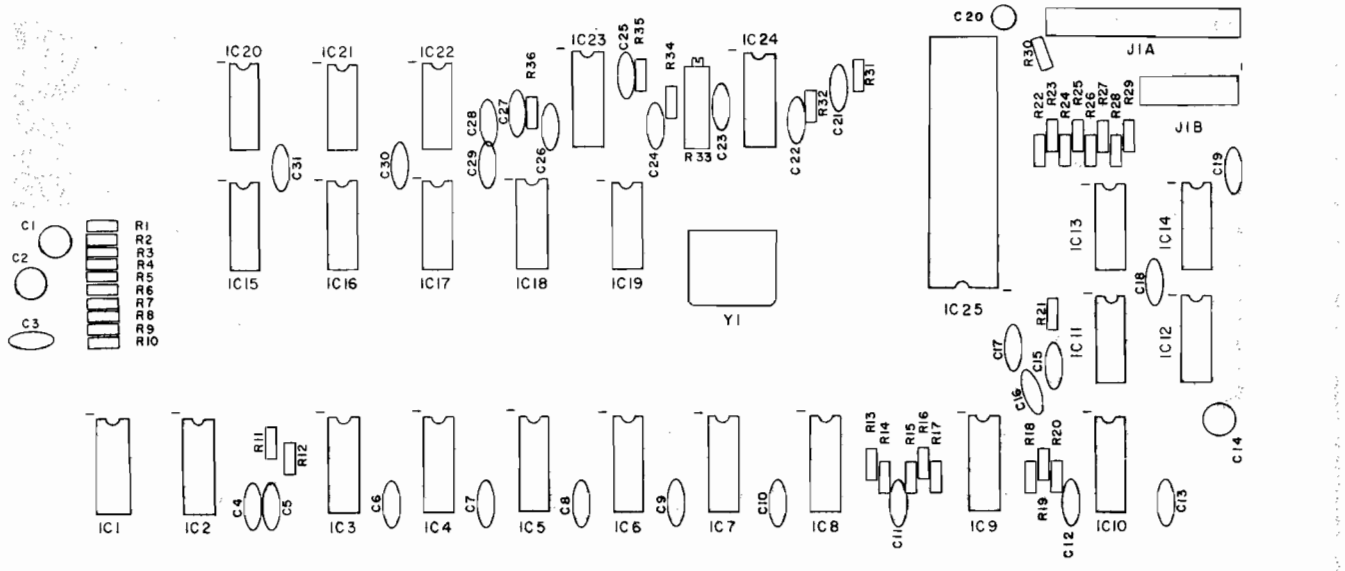
Specifically, PSYNC is generated by gating I/O request and memory request thru a NAND gate (IC21) whose output goes to the input of a 74LS74 (IC16) which is clocked by the Phase 2 signal. PSYNC is taken off of the $\overline{Q}$ of IC16.

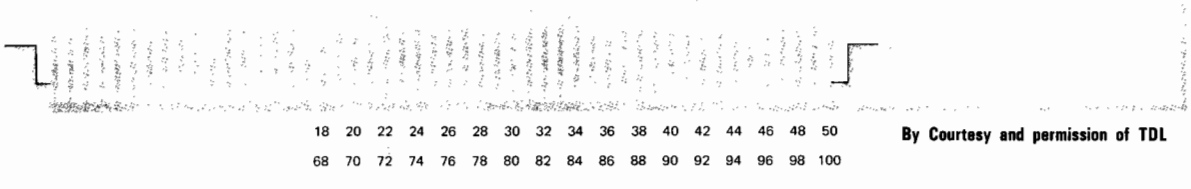
A wait is accomplished by gating the PRDY signal and forcing a low into the wait control line of the Z-80. In addition, an extra PRDY line has been made available which may be ***jumpered*** to any unused bus line for future applications. When not in use these lines should be ***jumpered*** together. (pins # 3 and #5 of IC17) The wait signal is initiated by the coincidence of the clock pulse with the pulling down of any of the 3 ready lines (PRDY, XRDY, LRDY).

The interrupts enabled flag is not provided on the Z-80. This has been simulated by the use of an 8 input NAND gate (IC14) and some decode gating (IC17) feeding a set-reset flip flop (IC18) to provide the user with a proper indication when the interrupts are enabled.

The interrupt pin of the Z-80 is handled in exactly the same fashion as that of the 8080, coming to the same bus pin. However, the non-maskable interrupt pin of the Z-80, which represents a significant feature of the Z-80 is brought out to a pull-up resistor, and may be ***jumpered*** to pin #4 on the bus, VIØ, the highest priority interrupt line. Thus configuring the Z-80 into the Altair Bus does not detract from this Z-80 feature.

The SSTACK status signal of the 8080 is not gener-





By Courtesy and permission of TDL

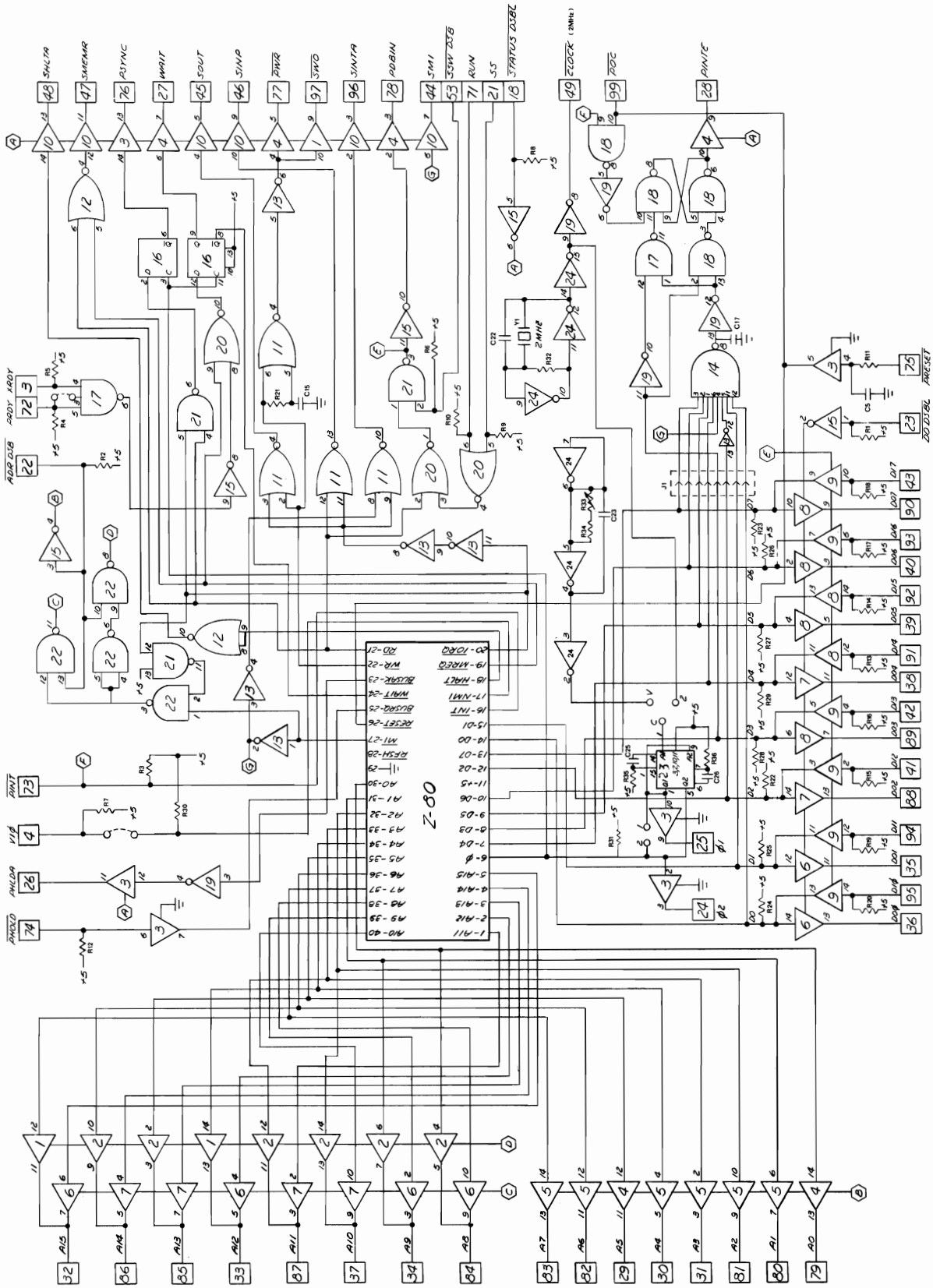


Figure 1. TDL ZPU™ Schematic Diagram

By Courtesy and permission of TDL

ated. Instead, the Z-80 REFRESH signal may be ***jumpered*** out to this line for use with future dynamic memory designs.

Processor write is generated by the Z-80, however in this application TDL has added some additional delay in order that the STATUS OUT or MWRITE may be properly decoded.

Handling of the remaining control timing is straightforward. HALT ACK is generated by the Z-80. The MREAD signal is a function of the Z-80 READ and MREQ signals. STATUS OUTPUT is a function of WRITE in conjunction with an I/O request. STATUS INPUT is a function of a READ in conjunction with an I/O request. PDBIN is a function of the READ signal. The interrupt acknowledge signal is a function of a simultaneous MI and I/O request.

All processor signals with the exceptions of phase one, phase two, and not clock are tri-statable thru the normal Altair bus signal.

The ZPU card features two clocks on-board. The first is fixed at 2MHz thru crystal control, and the second is variable between less than 1 and greater than 4 Mhz by means of a 20 turn trimpot.

The 2Mhz crystal controlled clock is selected by placing a jumper between the augat pins labeled "C" and "2M".

The variable speed clock is selected by "jumpering" between "C" and "V". (The pins "C", "2M" and "V" are located in area A on the ZPU card.)

The crystal oscillator is a parallel resonant circuit using a 2Mhz crystal in conjunction with several gates of IC24, a 4049 CMOS oscillator chip. This clock generates $\overline{\text{CLOCK}}$ and a driving signal for a pair of one-shots. The one-shots (IC23 — no IC number was given on the schematic originally) comprise both halves of a F4123 and are used to generate Ø1 and Ø2 clock signals. This is not a bad way to produce these non-overlapping clock signals.

The variable oscillator utilizes the remaining sections of IC24 in a free-running oscillator whose frequency is controlled by a precision RC network, and the frequency may be varied by adjusting R33, a 20K 20 turn trimpot. The variable oscillator presents phase one and two to the bus. $\overline{\text{CLOCK}}$ is always a function of the crystal oscillator and is always maintained at 2MHz by that clock so that peripheral cards may be made to operate correctly regardless of processor speed. See the section on High-speed operation for details on this.

Regardless of which clock is selected, if the variable clock is tuned to within 100KHz or so of the crystal, there is a tendency for the 2 clocks to "lock in" to each other, that is to get into a fixed resonance. The operational effect of this is that when the variable clock is selected in this condition, initial frequency change either up or down will tend to be resisted until the frequency "jumps" roughly 50KHz, at which point smooth frequency adjustment may be made.

Two augat pins (in area "B" and "C" respectively on the board) are provided for observation of the phase one and phase two signals. These points are test points only and not intended for adjustment of clock speed. Clock speed should always be measured at point C in area A. (On my board area C was hard to find because of the loss of silk-screened information.)

By removing the jumper choosing either of the two on-board clocks and connecting the common pin (C) to an external frequency source, the ZPU card may be synchronized with another system if the user chooses. This also makes it possible to run the processor at very low speeds (down to DC) which on occasion can be tremendously useful. (For example, individual T-states may be observed on the front panel.) This is one of the nice hardware features of the Z-80. It would facilitate matters if a coax connector could be placed at the top of the board to aid in bringing in this external clock.

A visual inspection of the ZPU card reveals more buffers (8T97s or 74367s, ICs 1 - 10) than are usually seen on a CPU card. This additional buffering was necessary to reduce bus loading and to assure normal front panel operation.

The front panels of both the Altair and the IMSAI look at the high order addresses for information about the I/O port number during I/O operations. This was optional with the original designers of the 8080 systems because the I/O port number is output to both the high and low order addresses by the 8080.

The Z-80 outputs I/O port information only to the low order addresses. (Contents of the accumulator are then present on the high order addresses.) Hence, in order for the sense switches to operate normally 8 additional buffers have been added which transfer the lower 8 bits to the high order address lines during I/O operations.

The normal configuration of the ZPU card is that which enables it to operate in an Altair or IMSAI with other peripheral boards.

The kit as supplied and the instructions as given result in a CPU card which may act as a direct replacement for your current 8080 processor. There are however some options which may be exercised by the user which take advantage of several of the Z-80 options. These are:

1. Connecting the REFRESH signal to pin 98 on the bus.
2. Connecting the non-maskable interrupt to vectored interrupt lines.
3. Altering the processor speed.
4. Use of the duplicate PRDY line.

Pin #28 of the Z-80 outputs a $\overline{\text{RFSH}}$ signal, which may be used to provide refresh timing for dynamic memories. This signal may be placed on pin #98 of the bus. Pin #98 is normally occupied by SSTACK on the S-100 bus 8080 system, however this status indicator is not terribly useful and was omitted on the Z-80 altogether.

The $\overline{\text{RFSH}}$ signal may be picked up at area F, immediately to the left of the Z-80, and "jumpered" to the pad in area G, straight down and slightly to the left from the Z-80. This places the signal on the bus.

When the signal is on the bus, the status light on the front panel, labeled STACK will now stay lit when the processor is running, indicating that the REFRESH signal is on the bus.

For the exact timing information about the $\overline{\text{RFSH}}$ signal, see the Z-80 manual. This signal is useful to systems utilizing dynamic RAM storage.

On the Z-80, pin 17 is $\overline{\text{NMI}}$, the non-maskable interrupt. To quote the Z-80 manual:

"The non maskable interrupt request line has a higher priority than $\overline{\text{INT}}$ and is always recognized at the

end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{NMI}$ automatically forces the Z-80 CPU to restart to location 0066_H."

This powerful interrupt capability is made available to the ZPU user.

Pin #17 of the Z-80 and pin #4 of the bus (VIØ) are normally both held high by pullups. Solder pads at location H and location E may be jumpered together, thus making the NMI available at VI0, the highest priority vectored interrupt line.

The Z-80 has the capability of operating from DC on up to some maximum limit greater than 2.5MHz because of its static nature. To take full advantage of this capability the ZPU card has been designed with a variable speed clock on-board.

P #1, an augat pin soldered to a wire represents the phase one and two inputs to the processor. If the pin is placed in J2, the augat pin labeled "V" in area A, then by adjusting the trimpot located above the crystal, the frequency may be varied over a range of approximately 3 MHz.

Normally, when one is reducing the speeds, simply turning the speed down is sufficient, and no problems will be encountered. For individuals whose systems may currently be marginal at 2MHz, reducing the processor speed may well greatly increase reliability of the system. Some marginal memories may operate with no wait states if the clock is set at about 1.5 MHz.

When speed is increased it is sometimes necessary to readjust the timing of the 74123 for stable operation. This RC network (R36 and C26) effects the phase one and phase two relationships, which become more critical as processor speed is increased.

The duplicate PRDY line was included in order to facilitate operation with the Altair 8800B, or for any other use the user might dream up.

The extra PRDY line comes off of IC17, area D, immediately to the left of the IC has 2 pads which are normally ***jumpered*** together. If one wishes to use the extra PRDY line, remove the jumper, and take the PRDY signal off of pin #3, the top of the two pads.

The 8800B requires 2 additional RDY lines. XRDY2 is on bus line #12. If operation with the 8800B is desired, ***jumper*** the additional RDY line on the ZPU to this bus pin. The other RDY line is FRDY, which is pin #58 on the bus. The user may use this line as he wishes.

The Z-80 unlike the 8080 does not necessarily stop on an M1 state. In order to operate the front panel, the processor must, however, be in the M1 state. TDL has decided to omit additional circuitry which would force the Z-80 to halt at M1. Therefore when operating in single-step mode it is necessary to make sure that you step the processor to an M1 state and then operate the front panel.

The Z-80 chip itself is guaranteed to operate up to 2.5 MHz. Most Z-80's appear to operate in the neighborhood of 3MHz and some will operate at 4MHz. TDL has designed the ZPU board to operate reliably at clock speeds up to 4MHz. The ZPU manual contains an excellent section on high speed operation of the ZPU, including a simple procedure for adjusting the speed of the processor using the TDL SPU to its maximum.

It is important to note that although the system $\overline{CLOCK}$ line is maintained at 2 MHz regardless of processor speed, some boards use 01 or 02 for their

timing. These boards will not operate correctly when the processor timing is altered. In order to fix this problem, simply cut the clock trace on the non-operating board (from 02 or 02 and ***jumper*** it to the $\overline{\text{CLOCK}}$ line.) I have done this routinely on all my I/O boards so that I may substitute either the ZPU or the CPU card at will.

The TDL ZPU manual contains a section on compatibility. Bear in mind the fact that there are two types of compatibility, hardware and software. In general, with the exception of the SSTACK signal and the previously mentioned single-step problem, hardware compatibility between the TDL ZPU and the S-100 CPU has been achieved. The front panel of your system will operate in its normal fashion with all switches serving their normal function.

The Z-80 is 100% machine code compatible with the 8080's seventy-eight instructions. Hence standard 8080 software will run without modification on the Z-80. However, if you are using software controlled timing by means of the number of machine cycles necessary to complete a loop, 100% compatibility will not exist. The problem is inherent in the Z-80. The architecture of the Z-80 is more efficient than that of the 8080. In its design many instructions of the 8080 — while having the same machine code, have fewer "T-states": thus the instruction is executed faster in real time.

Obviously where the real time length of a timing loop is controlled by software, the program will have to be rewritten to adjust for the higher realtime execution speed of the Z-80. This is true even if both the 8080 and the Z-80 are running at exactly 2MHz. In the benchmark programs the Z-80 running only the 8080 instruction set has been found to be about 10% faster even while being maintained at 2MHz clock speed.

TDL notes that almost all 8080 languages run without a hitch on the TDL ZPU. The sole exception is Altair Basic. This Basic has as part of its routines several occasions where the parity flag is checked as part of the function. In the Z-80 the parity flag indicates OVERFLOW and not parity during math routines. As a result Altair Basic will not run on the Z-80. However, the structure of the Basic language does not require this use of the parity flag; it was used to reduce program space by several bytes. It therefore can be patched by those who wish to do so. An attractive alternative would be to procure TDL's 8K Basic which is Altair compatible and which contains a large number of exclusive and desirable features. Another solution would be to buy one of the Z-80 Basics now available which provide operational features. They are not, however, 8080 compatible.

The ease of assembly, low cost, and special features of the TDL ZPU make it a good alternative to the standard CPU card. In addition TDL's ZPU manual is very comprehensive and the Zilog Z-80 is also included. TDL also provides a listing and paper tape of their ZAP monitor.

The ZAP Monitor is a IK version of TDL's 2K ZAPPLE Monitor. It is relocatable (can be placed anywhere in memory), expandable ("modules" of additional commands can be tacked on at the end, like cars on a freight train.), and quite powerful as a system executive.

The expandable feature should be of great interest to the user. Since it is designed in a modular fashion, and since the ZAPPLE is its direct parent, this monitor features tremendous expandability - either of routines generated by the user, or by routines provided by Technical Design Labs. Several "modules" which will be of great interest include powerful "breakpoint", "search" and "register display" commands.

For only $269.00 the TDL ZPU represents a very nice low cost means to enhance your S-100 bus system.

(16)

ZPU PARTS LIST

IC 1 to 10	8T97 or 74367
IC 11, 12, 20	74LS02
IC 13, 15, 19	74LS04
IC 14	74LS30
IC 16	74LS74
IC 17	74LS10
IC 18, 21, 22	74LS00
IC 23	74123
IC 24	4049
IC 25	Z-80
IC 26	7805
R 1 to 10	1K, 5%, Brown, Black, Red, Gold
R 12 to 20	1K, 5%, Brown, Black, Red, Gold
R 30	1K, 5%, Brown, Black, Red, Gold
R 11, 31	100 ohm, 5%, Brown, Black, Brown, Gold
R 21	47 ohm, 5%, Yellow, Violet, Black, Gold
R 22 to 29	4.7K, 5%, Yellow, Violet, Red, Gold
R 32	4.7K, 5% Yellow, Violet, Red, Gold
R 34	3.3K, 5%, Orange, Orange, Red, Gold
R 35	10K, 5%, Brown, Black, Orange, Gold
R 36	12K, 5%, Brown, Red, Orange, Gold
R 33	20K, 20 turn trimpot
C 1, 2, 14	47Mf, 25V, dipped tantalum electrolytic
C 3 to 13	.1Mf Disc Ceramic
C 16, 18, 19	.1Mf Disc Ceramic
C 15, 17	.001Mf Disc Ceramic
C20	33Mf, 25V dipped tantalum electrolytic
C 21, 24	.1Mf Disc Ceramic
C 27 to 31	.1Mf Disc Ceramic
C 22	10Pf Disc Ceramic
C 23	6 Pf Disc Ceramic
C 25	27 Pf Disc Ceramic
C 26	47 Pf Disc Ceramic
Y1	2Mhz Crystal
J1A	10 pin molex connector
J1B	16 pin high profile DIP socket
J3, 4, 5, 6	Augat pins
P1	Augat Pin
1 Heatsink	
1 ea. 6/32 x 5/16"	machine screw, lockwasher, nut
1 ZPU PC board	
12	14 pin low profile IC sockets
12	16 pin low profile IC sockets
1	40 pin high profile IC socket

Miscellaneous

6"	jumper wire
5'	solder
1	Zilog ***Z80 CPU Technical Manual***
1	ZPU Documentation Manual
1	Paper tape of the ZAP monitor