CHAPTER 7

HARDWARE DESCRIPTION

Chapter 7 provides a functional description of the MC68000 Educational Computer Board and detailed information on using the wire-wrap facilities.

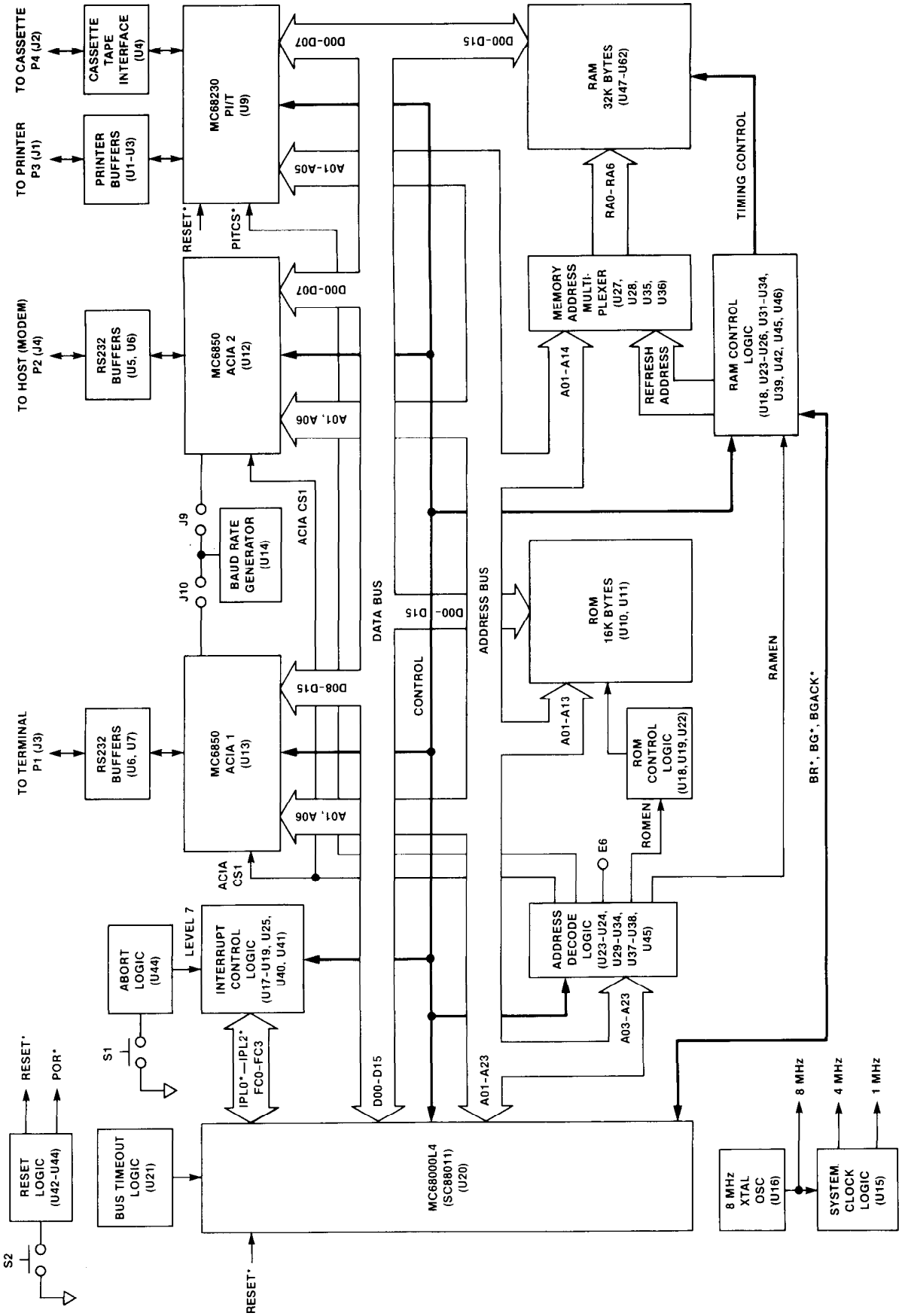

FIGURE 7-1. Block Diagram - Educational Computer Board

CHAPTER 7

HARDWARE DESCRIPTION

7.1 INTRODUCTION

Chapter 7 provides a functional description of the MC68000 Educational Computer Board hardware, including a block diagram. With the description contained here and the schematic drawings of Chapter 8, the user can gain a good understanding of the board's design. Also discussed in this chapter is use of the wire-wrap area of the board. Throughout Chapters 7 and 8, the asterisk (*) is used to denote active low signals.

7.2 FUNCTIONAL DESCRIPTION

The MC68000 Educational Computer Board is a complete microcomputer system built around a 4 MHz processor (MC68000L4). All memory and I/O devices communicate with the processor via a common unbuffered bus structure. The block diagram of the board is shown in Figure 7-1, which illustrates data paths, the addressing scheme, and control logic flow. The functional areas are described in the following paragraphs.

7.2.1 MC68000L4 Microprocessor

The L4 version of the MC68000 is a 4 MHz clock device. The 4 MHz clock is the time base from which all processor timing is derived (see MC68000 data sheet for details). The 4 MHz rate does not relate to bus transaction times directly because these can be either asynchronous in nature or generated by an E clock which is supplied by the MC68000L4 (4 MHz divided by 10 = 400 kHz E clock).

7.2.2 Address Decode

The memory map for the educational computer is shown in Table 7-1. The Address Decode Logic (U23-U24, U29-U34, U37-U38, U45) shown in Figure 7-1 generates enable signals RAMEN, ROMEN, ACIA CS1, and PITCS* in accordance with this memory map. Address lines A03-A23 are decoded and used with the proper control signals to generate these signals.

The RAM is addressed at the bottom of the map ($000007-$007FFF) excluding the first eight locations which contain the initial stack pointer and program counter contents and are stored in ROM. The RAM is divided into two areas; that is, $000008-$0008FF the system area reserved for use by the system firmware, and $000900-$007FFF the user area.

Within the system area, addresses $000000-$0003FF are used for the MC68000 exception vector table. The remaining 1280 bytes (addresses $000400-$0008FF) are used as scratchpad memory for the TUTOR firmware including data buffers, pointers, temporary storage, etc.

The firmware ROM (EPROM) is located just above the RAM in the map at $008000-$00BFFF.

All I/O devices are mapped into the same 64K byte page at $010000-$01FFFF. Redundant mapping occurs within the page (that is, the same device appears at several addresses) because the address is not fully decoded. Chapter 6 contains Tables 6-1 and 6-2 which give the I/O address maps in detail.

Also, a special signal (E6) is provided as a 64K-byte page decode located at $030000-$03FFFF. This signal is intended to allow an M6800 type bus interface via the wire-wrap capability.

TABLE 7-1. Memory Map

FUNCTION			ADDRESS
System Memory	Exception Vector Table	ROM/EPROM RAM	$000000-$000007 (1) $000008-$0003FF
	Tutor Scratchpad	RAM	$000400-$0008FF
User Memory		RAM	$000900-$007FFF
Tutor Firmware		ROM/EPROM	$008000-$00BFFF (1)
Not Used			$00C000-$00FFFF
I/O Devices	PI/T (Lower byte only)		$010000-$01003F
	ACIA2 (Lower byte) & ACIA1 (Upper byte)		$010040-$010043
	Redundant Mapping		↓ $01FFFF
Not Used			$020000-$02FFFF
M6800 Page (E6)			$030000-$03FFFF
Not Used			$040000-$FFFFFF

NOTE: (1) Denotes read only

7.2.3 32K Byte RAM

Sixteen three-supply MCM4116B (16K x 1) devices (U47-U62) make up the dynamic RAM array. These can be accessed either on a byte or word basis, and data transfers to and from the MC68000 use asynchronous bus transfers. The memory access time is approximately 450 nanoseconds and the RAM DTACK* is generated about 500-625 nanoseconds after the start of a read or write cycle.

Operation of the memories is determined by the RAM CONTROL LOGIC (U18, U23-U26, U31-U34, U39, U42, U45, U46). The control logic generates timing control for the RAM devices as well as control signals for the MEMORY ADDRESS MULTIPLEXER (U27, U28, U35, U36). The multiplexer generates row and column addresses from lines A01-A14 during read and write cycles. Refresh addresses are also routed to the memories by the multiplexer during memory refresh.

The DRAM's are completely refreshed once every 1.5 milliseconds on the average (1.9 milliseconds worst case) using a technique called RAS only refresh. When the refresh timer indicates the MCM4116B's need to be refreshed, the RAM CONTROL LOGIC requests control of the MC68000 bus via a Bus Request (BR*) signal. This is a convenient way to prevent the processor from accessing RAM during refresh.

The MC68000 releases the bus and asserts Bus Grant (BG*) in response to the BR*. The RAM CONTROL LOGIC then asserts Bus Grant Acknowledge (BGACK*), releases the BR*, and proceeds with the memory refresh. After the BR* is released, the MC68000 releases BG* and waits for BGACK* to release.

During a refresh cycle, eight rows are refreshed at the rate of one row per microsecond. Sixteen such cycles are required to completely refresh the memory every 1.5-1.9 milliseconds. At the end of each cycle the BGACK* is released, the MC68000 regains control of the bus, and processing proceeds.

7.2.4 16K Byte ROM

The system firmware (TUTOR) is stored in two 64K bit ROM's (U10, U11). MCM68764 EPROM's or MCM68A364 ROM's can be used. Access time for the ROM's can vary from 350 nanoseconds to 450 nanoseconds, depending on the device used.

The system ROM can be read on a byte or word basis. Attempting a write to ROM will result in a bus timeout error. The ROM also uses an asynchronous bus interface with the ROM DTACK* returned 500-625 nanoseconds after ROMEN is received.

7.2.5 Serial Communications Ports

Paragraph 6.2 discusses operation of the serial communications ports in detail. Two MC6850 ACIA's provide the bus interface for the serial ports. ACIA1 (U13) is used for the terminal Port 1 and is connected to bits D08-D15 of the data bus. ACIA2 (U12) is used for the host Port 2 and is connected to bits D00-D07.

The baud rate generator (U14) provides transmit and receive clocks for both ACIA's. Headers J9 and J10 are used to jumper select baud rates varying from 110 to 9600 baud.

Both serial ports are RS-232C compatible. Buffers U5, U6, and U7 translate the ACIA voltage levels to RS-232C interface levels.

The ACIA's are the only devices on the Educational Computer Board that take advantage of the MC68000's M6800 compatible synchronous interface. The ACIA's can only be accessed using a synchronous type of bus transfer. These devices are clocked by a signal called the E clock which is supplied by the MC68000 (E = 4 MHz divided by 10 = 400 kHz). Whenever the address decode signals that either ACIA is to be accessed (VPA* is asserted), the MC68000 synchronizes itself with the E clock and uses a synchronous bus cycle. More detail concerning this mode of operation is given in Section 6 of the MC68000 User's Manual, MC68000UM.

7.2.6 MC68230 PI/T (Printer Interface, Cassette Tape Interface, and Timer)

The MC68230 provides several features on the educational board. The PI/T contains an on-board programmable 24-bit timer. Parallel Ports A and B of the PI/T are buffered to drive a Centronics-compatible printer. Also, Port C of the PI/T is buffered as a cassette tape interface. These are discussed in Chapter 6 of this manual.

The MC68230 is tied to data bus lines D00-D07 and uses the MC68000 asynchronous interface.

7.2.7 Interrupt Control Logic

Devices U17-U19, U25, U40, and U41 compose the INTERRUPT CONTROL LOGIC. The interrupt priority levels and vectoring techniques are discussed in paragraph 6.6. The logic priority encodes the interrupt request and inputs the highest request level to the MC68000 (IPL0*-IPL2*). The logic also monitors the function codes (FC0-FC2) and generates interrupt acknowledge signals for the proper device. ACIA1, ACIA2, ABORT, and the special MC6800 IRQ all require an autovectored interrupt, and the VPA* signal is asserted. Also, when the timer interrupt is acknowledged, TIACK* is asserted to the PI/T. Finally, when the PI/T parallel port interrupt is acknowledged, PIACK* is asserted.

7.2.8 System Clocks

An 8-MHz crystal oscillator (U16) is the time base from which all clock frequencies are derived. Counter U15 is used to generate 4-MHz and 1-MHz clocks. The MC68000 runs from the 4-MHz clock. Control logic and other devices in the system use all three frequencies as time bases.

7.2.9 Bus Timeout Logic

With an asynchronous bus interface, bus timeout logic (U21) must be provided. The timeout logic ends the bus cycle if a device fails to respond within the allotted time, and a bus error is signaled. A device may fail to respond due to circuit failure, addressing a non-used location, or attempting a write cycle to ROM. The bus timeout on the Educational Computer Board is about 10 microseconds long.

7.2.10 System Initialization

The RESET LOGIC (U42-U44) provides system initialization under two modes. Under system power-up, a timer activates both the RESET* and Power On Reset (POR*) signals. RESET* initializes the MC68000 and MC68230. All other timing devices are initialized by POR*.

The second mode is when the reset switch S2 is activated. In this case, only RESET* is activated and thus only the MPU and PI/T are initialized.

It should be noted that the HALT* line to the processor is also activated during power-up. An LED indicator is driven from the HALT* line and lights whenever the processor is in a halt condition.

The initialization sequence for the MC68000 includes loading the supervisory stack pointer and program counter values stored in ROM ($000000-$000007), setting the status register to interrupt level 7, and beginning processing at the PC address. This process starts up the TUTOR firmware package and initializes all system registers and devices.

7.2.11 ABORT Function

Switch S1 activates the ABORT LOGIC (U44). Under this condition, a level 7 non-maskable interrupt is generated, which returns control of the system to TUTOR. The ABORT routine does not reinitialize the system. The ABORT function is useful to regain control of processing without destroying system conditions such as existing register and memory contents.

The interrupt vector to the ABORT firmware is located in RAM. If this vector is altered, the ABORT firmware may not be executed; the results are indeterminate. A user-provided vector can be used. In this case, the user software will be executed when the ABORT button is pressed. RESET will reprogram the vector to point to the TUTOR firmware.

7.3 INTERFACE USING THE WIRE-WRAP AREA

The MC68000 Educational Computer Board provides a small wire-wrap area for those users desiring to do custom interface. The location of the wire-wrap area and the signal connection points are shown in Figure 7-2. The following paragraphs provide a detailed discussion of various aspects of doing custom interface to the ECB.

7.3.1 Wire-wrap Device Mounting Area

An area of approximately 3.5 square inches is provided to mount devices (see detail Figure 7-3). Six rows of holes (24 holes/row) are available to mount sockets or devices. The holes are on one-tenth inch centers and the rows are three-tenths inch apart. The component side of the board has seven metal areas which are tied to the board's ground plane. On the opposite side of the board, metal strips are provided which are tied to +5.0 Vdc power.

With the hole pattern provided, most standard dual-in-line devices can be mounted, up to and including a 48-pin package. This is large enough to accommodate another MC68230 PI/T as an example.

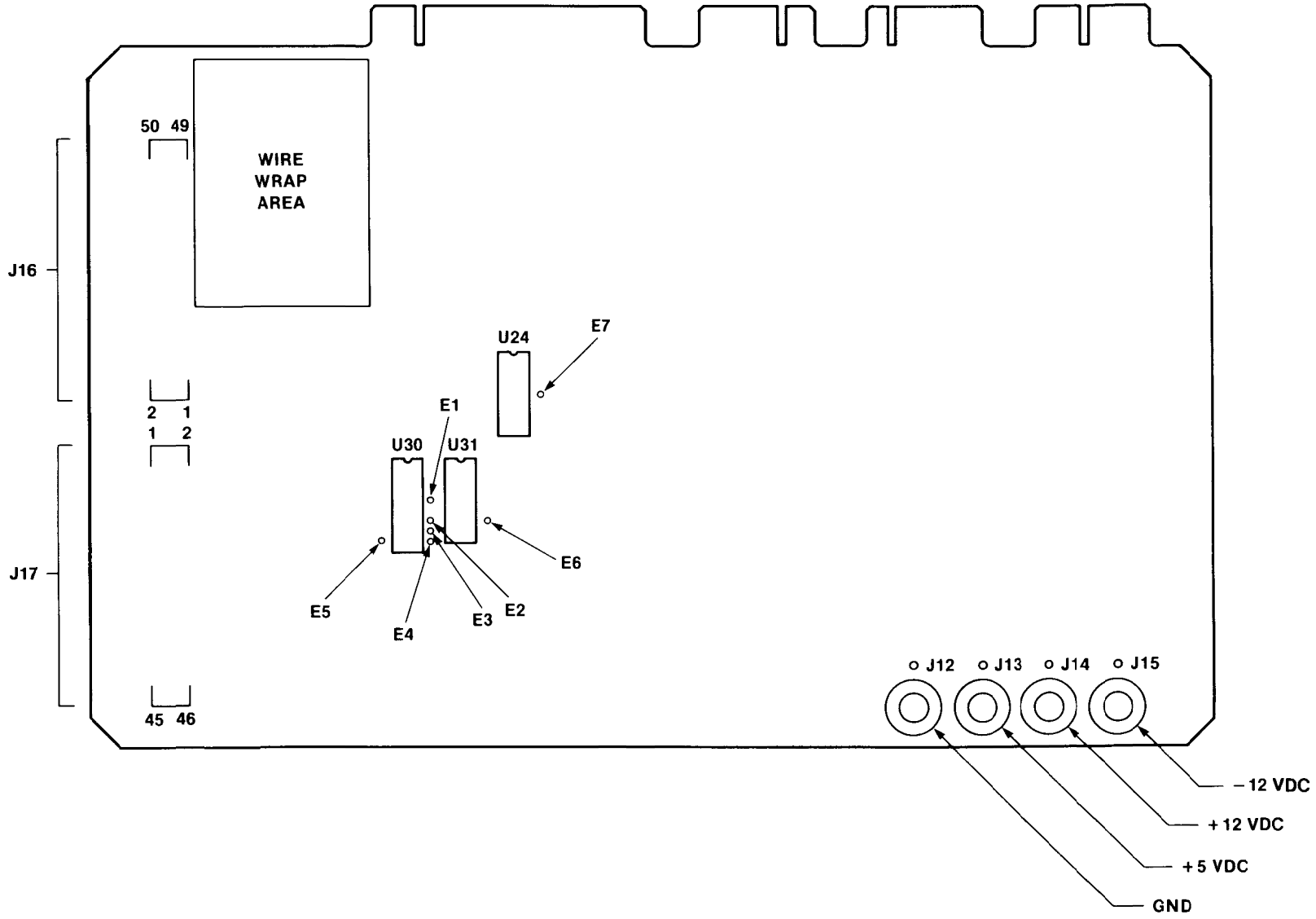

FIGURE 7-2. MEX68KECB Signal Connection Points For Wire-Wrap

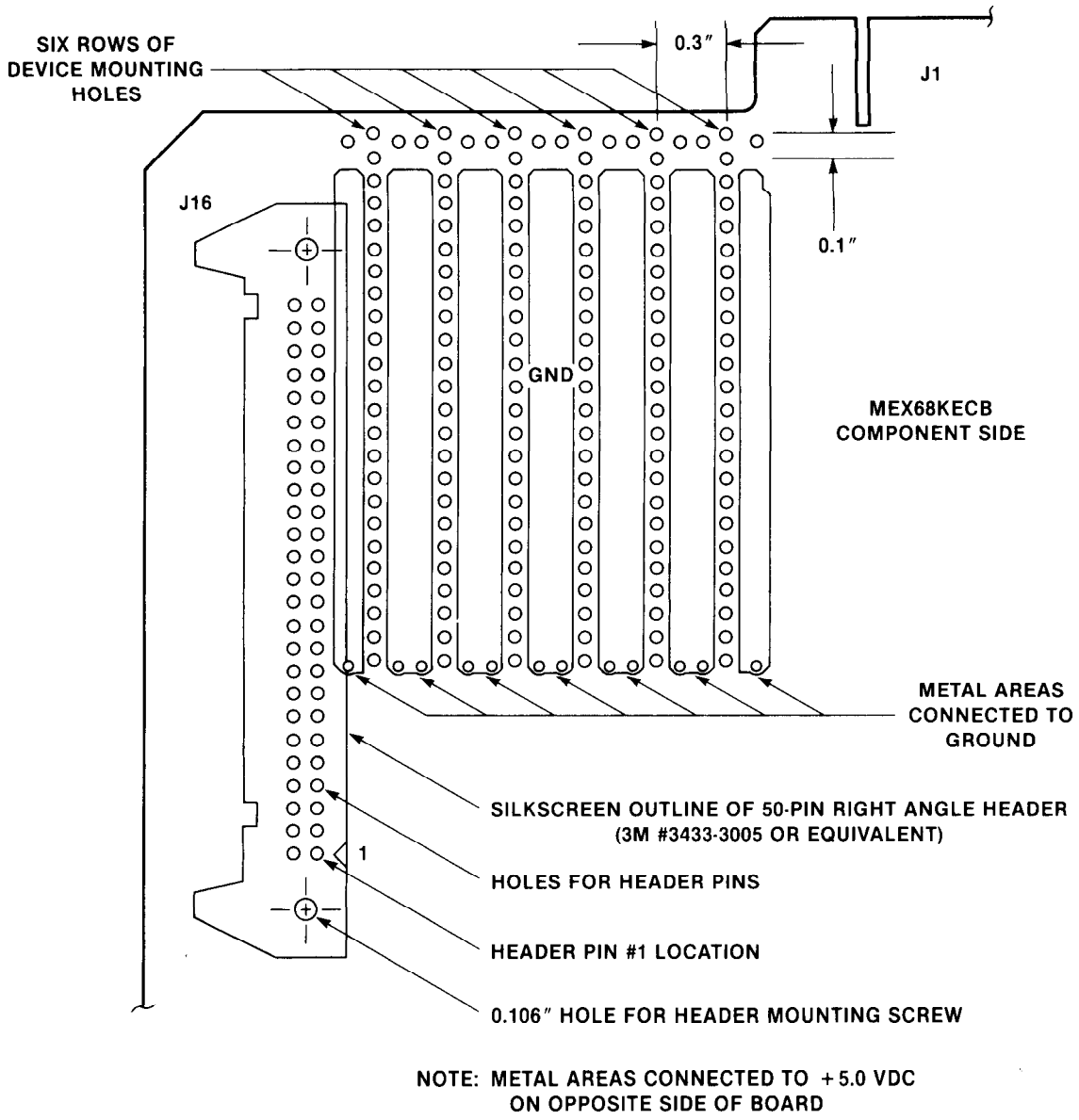

FIGURE 7-3. Detail of Wire-wrap Area

7.3.2 Auxiliary I/O Header J16

In addition to the wire-wrap area, the ECB has provision for an auxiliary I/O header (designated J16). The Figure 7-3 detail shows the location of the header, and Figure 7-4 illustrates the header mounting detail. The hole pattern is designed to accept a 50-pin wrap tail right angle header (standard profile) which is 3M #3433-3005 or equivalent.

When mounting the header as shown in Figure 7-4, two #2 x 3/8 inch screws and two #2 hex nuts are used. The board silkscreen shows an outline of the header. A 50-pin ribbon cable can be connected to this header, and signals are wire-wrapped to the header wrap tails.

7.3.3 MC68000 Bus Signal Connections

A connection area designated J17 gives access to the MC68000 bus signals and system timing. Figure 7-2 shows the location of J17 and gives pin locations. Table 7-2 lists J17 pin number vs. signal designation and also shows attributes of these signal lines.

To use the signal lines, individual wire-wrap pins should be mounted in the holes. These can be soldered in or press fit. Connections are then wrapped to these pins.

7.3.4 Extending System Address Decode

The memory map for the educational computer is given in Table 7-1. When using the wire-wrap area, the designer must not put devices at any of the occupied address locations. To facilitate user address decode, connection points E1 through E6 have been provided on the board, which give enable signals for unused areas of the MC68000 memory map. These connection points include two types:

a. Connection points E1 through E5 (see Figure 7-2 for location) give decode signals for various segments of the MC68000 upper memory map. Figure 7-5 shows the address decode logic and Table 7-3 lists the decoded segments.

   Each signal is low when enabled, and the user can utilize one of these enables as upper address decode. The signal is valid whenever the selected address segment is decoded and AS* is asserted.

b. Connection point E6 is used to select a memory segment for M6800 synchronous interface located at addresses $030000-$03FFFF. Paragraph 7.3.6.1 discusses this in detail.

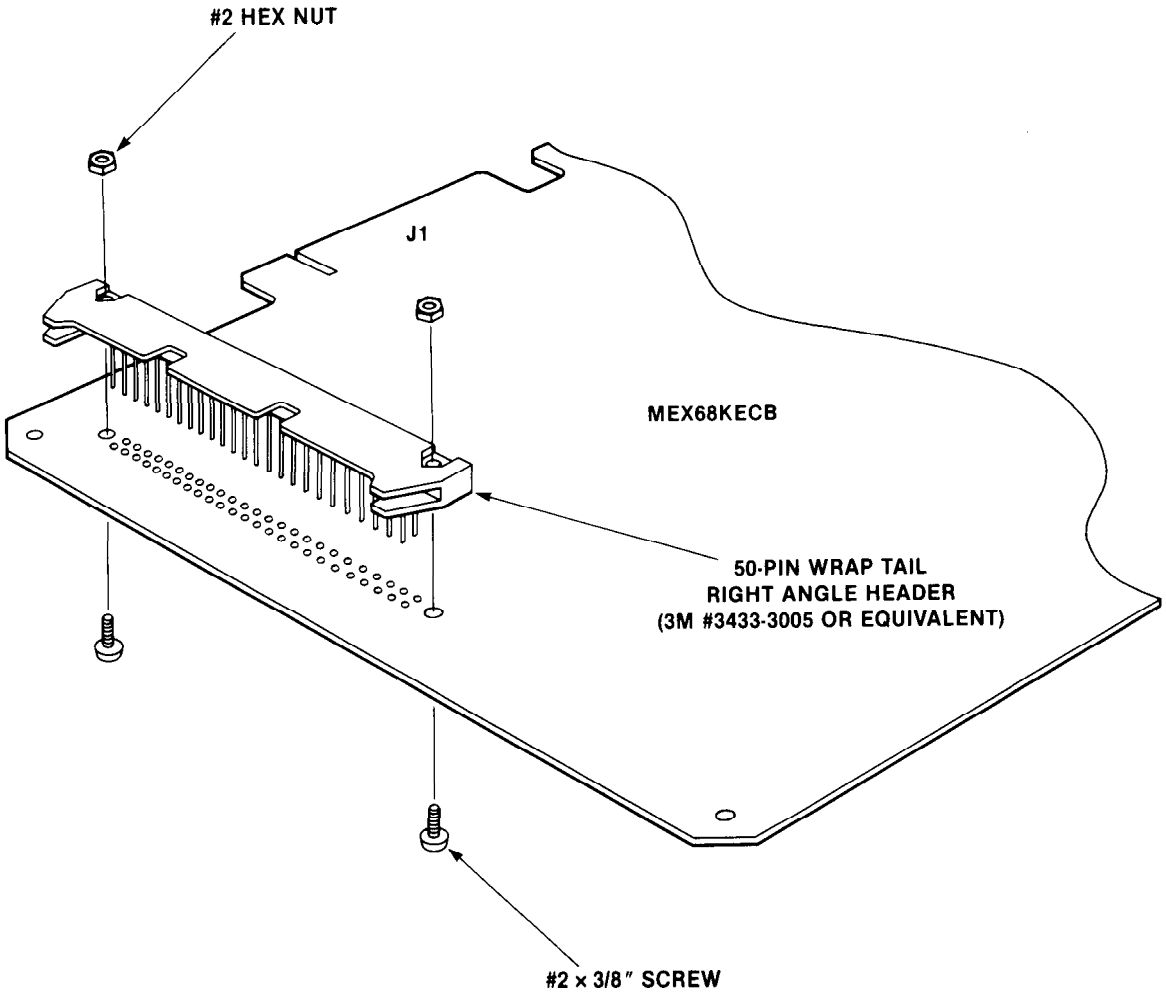

FIGURE 7-4. Auxiliary I/O Header Mounting Detail

TABLE 7-2. J17 Signal Designations

PIN NO.	SIGNAL NAME	DESCRIPTION	4700 ohm PULLUP	THREE-STATE
1	D04	Data Bus Bit 4	Yes	Yes
2	D03	Data Bus Bit 3	Yes	Yes
3	D05	Data Bus Bit 5	Yes	Yes
4	D02	Data Bus Bit 2	Yes	Yes
5	D06	Data Bus Bit 6	Yes	Yes
6	4 MHz CLK	4 MHz System Clock	No	No
7	D07	Data Bus Bit 7	Yes	Yes
8	D14	Data Bus Bit 14	Yes	Yes
9	D08	Data Bus Bit 8	Yes	Yes
10	D15	Data Bus Bit 15	Yes	Yes
11	D09	Data Bus Bit 9	Yes	Yes
12	RESET*	System Reset	Yes	No (O.C.)
13	D10	Data Bus Bit 10	Yes	Yes
14	D01	Data Bus Bit 1	Yes	Yes
15	D11	Data Bus Bit 11	Yes	Yes
16	E	E Clock (400 kHz)	No	No
17	D12	Data Bus Bit 12	Yes	Yes
18	AS*	Address Strobe	Yes	Yes
19	D13	Data Bus Bit 13	Yes	Yes
20	UDS*	Upper Data Strobe	Yes	Yes
21	D00	Data Bus Bit 0	Yes	Yes
22	LDS*	Lower Data Strobe	Yes	Yes
23	A15	Address Bus Bit 15	Yes	Yes
24	R/W*	Read/Write	Yes	Yes
25	A14	Address Bus Bit 14	Yes	Yes
26	A13	Address Bus Bit 13	Yes	Yes
27	A12	Address Bus Bit 12	Yes	Yes
28	FC2	Function Code Bit 2	No	Yes
29	A11	Address Bus Bit 11	Yes	Yes
30	FC1	Function Code Bit 1	No	Yes
31	A10	Address Bus Bit 10	Yes	Yes
32	FC0	Function Code Bit 0	No	Yes
33	A09	Address Bus Bit 9	Yes	Yes
34	A01	Address Bus Bit 1	Yes	Yes
35	A08	Address Bus Bit 8	Yes	Yes
36	A02	Address Bus Bit 2	Yes	Yes
37	A06	Address Bus Bit 6	Yes	Yes
38	A03	Address Bus Bit 3	Yes	Yes
39	A07	Address Bus Bit 7	Yes	Yes
40	A04	Address Bus Bit 4	Yes	Yes
41	A05	Address Bus Bit 5	Yes	Yes
42	DTACK*	Data Transfer Ack. (1)	No	No
43	8 MHz CLK	8 MHz System Clock	No	No
44	6800 IRQ*	M6800 Interrupt Request (2)	Yes	
45	1 MHz CLK	1 MHz System Clock	No	No
46	VMA*	Valid Memory Address	No	Yes

NOTES:

(1) DTACK* cannot have device outputs connected to it. See Paragraph 7.3.5.

(2) 6800 IRQ* is an input only line.

TABLE 7-3. Address Segment Enable Signals for Wire-wrap Users

ENABLE SIGNAL	ADDRESS SEGMENT
E1	$020000-$02FFFF
E2	$040000-$04FFFF
E3	$050000-$05FFFF
E4	$060000-$06FFFF
E5	$070000-$07FFFF
NOTE: Signals are a low TTL level when enabled.	

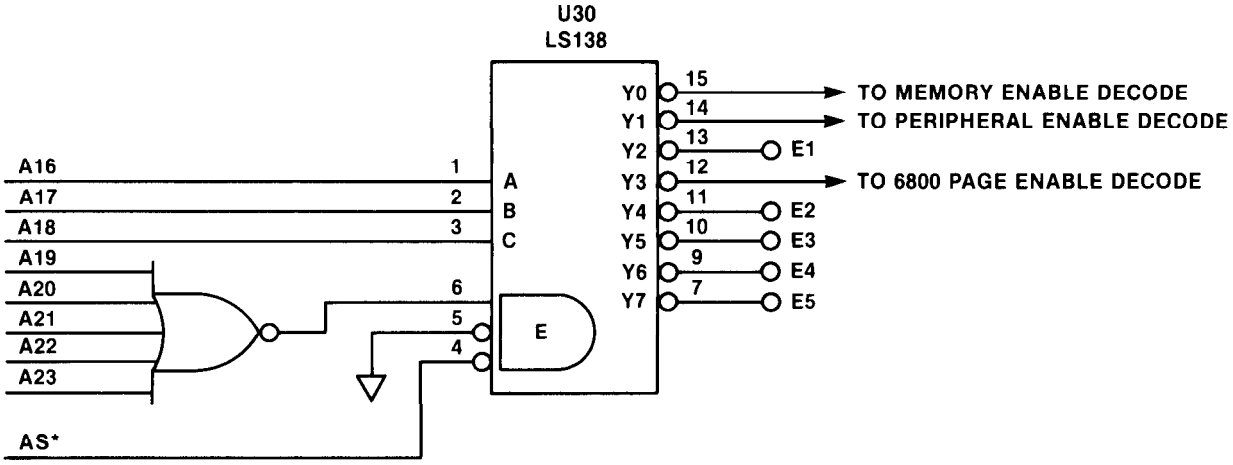

FIGURE 7-5. Address Decode Logic For Memory Map Primary Segments

7.3.5 Asynchronous Bus Interface

Although the MC68000 is capable of doing synchronous bus operations, it is primarily an asynchronous bus machine. The user can interface additional devices to the on-board asynchronous bus via the wire-wrap area; however, care must be taken. The following guidelines apply:

a. The on-board MC68000 bus is unbuffered. The user must not exceed loading requirements of the MC68000.

b. The user must meet timing requirements specified on the MC68000 Data Sheet.

c. Access to the MC68000 signal lines is provided via J17. Special care must be taken with DTACK* (Data Transfer Acknowledge). The processor DTACK* is generated by ANDing DTACK PIT*, DTACK RAM*, and DTACK ROM*, as shown in Figure 7-6. The processor DTACK* goes low whenever any of these go low. The user cannot add another signal to the processor DTACK* because this signal is not an open-collector output.

   A USER DTACK* is connected to the system via connection point E7 as shown in Figure 7-6. The PIT DTACK* is turned off when not required, and the USER DTACK* can be bussed to this point. A 4700 ohm resistor holds PIT DTACK* high when the driver is turned off. The USER DTACK* must be an open-collector or three-state driver. (E7's location is between packages U24 and U25 as shown in Figure 7-2.)

d. If an interrupt capability is required, the user is restricted to an M6800 type autovectored priority level 4 interrupt. See paragraph 7.3.6.2 for usage.

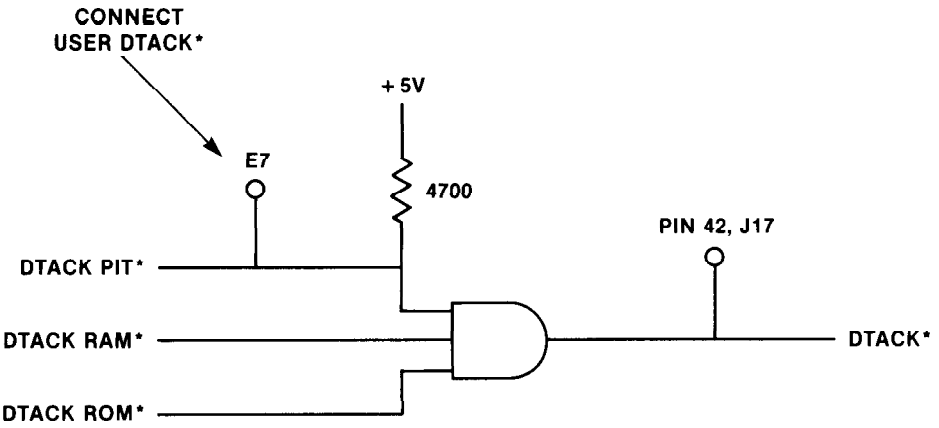

FIGURE 7-6. DTACK* Signal Generation

7.3.6 M6800 Type Synchronous 8-Bit Bus Interface

The MC68000 supports M6800 type synchronous bus transfers through the use of signal lines VMA*, VPA*, and E. Section 6 of the MC68000 User's Manual (MC68000UM) discusses these signal line functions in detail. The user can utilize the synchronous interface on the educational computer. The existing MC6850's also use this interface.

The same guidelines apply concerning bus loading, processor timing, and J17, as mentioned in paragraph 7.3.5. The educational computer also has special provision for user interface into the synchronous bus.

7.3.6.1 M6800 Page Address Decode. A 64K-byte segment of the system memory map is reserved for an M6800 type interface. Connection point E6 is enabled high whenever this page ($030000-$03FFFF) is selected. Connection point E6 can be located on Figure 7-2, and Figure 7-7 shows the logic generating signal E6.

The M6800 page enable E6 is activated when memory page $030000-$03FFFF is selected and both VMA* and LDS* are asserted. The memory page enable is first activated, which, in turn, activates VPA*. After the MC68000 receives VPA*, the processor synchronizes itself to the E clock and continues the bus cycle by asserting VMA*. Signal E6 recognizes that the M6800 page has been selected, VMA* has been asserted for a synchronous cycle, and the LDS* is asserted indicating a bus transfer on the lower eight data bus bits. Thus, the user must interface into the lower eight bits of the data bus when using signal E6.

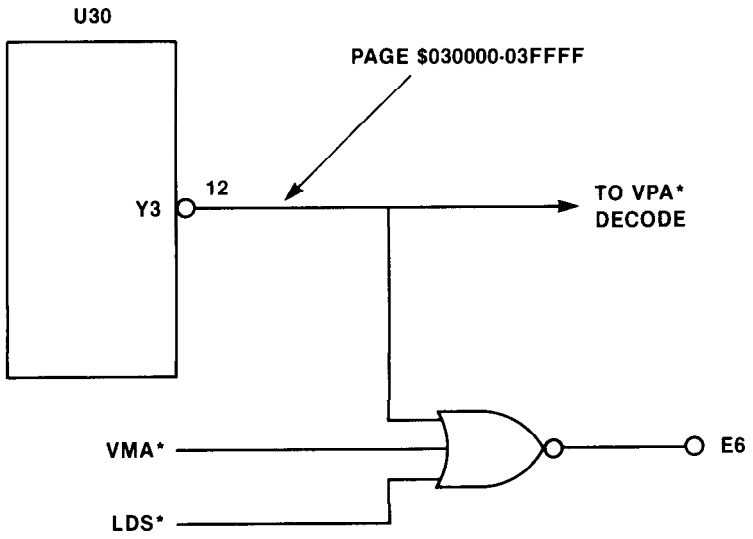

FIGURE 7-7. M6800 Page Address Signal Generation

7.3.6.2 Autovectored Interrupt Level 4. To facilitate an M6800 type interface, the educational computer also provides an autovectored interrupt request via Pin 44 of J17. When the interrupt request line is asserted (taken low), the MC68000 receives a level 4 priority interrupt. A level 4 interrupt acknowledge cycle from the MC68000 causes an autovectored response with the vector number equal to 28 (decimal) or $1C (hex).

The interrupt request must be held asserted until the interrupt service routine clears the interrupt request. The user must supply the interrupt service routine in his software, and he must also initiate the exception vector table at address $000070.

The M6800 interrupt request can also be used for devices on the asynchronous bus interface. The user must only follow the same rules for use and be aware the response is an autovectored interrupt.