National Semiconductor

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INS8073 NSC Tiny BASIC Microinterpreter

General Description

The INS8073, National's Tiny BASIC Microinterpreter, operates to provide a high level, easy to use language for performing control and computation functions in the user's system. The device is a self-contained CPU and Tiny BASIC interpreter on a single chip.

Designed for use in control applications, the Microinterpreter enables the user to write and debug programs on-line. The Microinterpreter executes source code directly, thus avoiding the need to translate the source code into machine language. The advantage of this approach is easier source code manipulation (because the source is always available), and instant revision of the program when errors are detected.

The NSC Tiny BASIC interpreter (resident in the INS8073) executes the user's source programs from read/write memory or ROM/PROM automatically. The program statements are interpreted and executed line-by-line.

The INS8073 is a programmed version of the INS8072, a 2.5K x 8 mask-programmable ROM and CPU. It provides complete TTL compatibility and uses a single 5V power supply. Faster and more sophisticated computing power is available through multiprocessing.

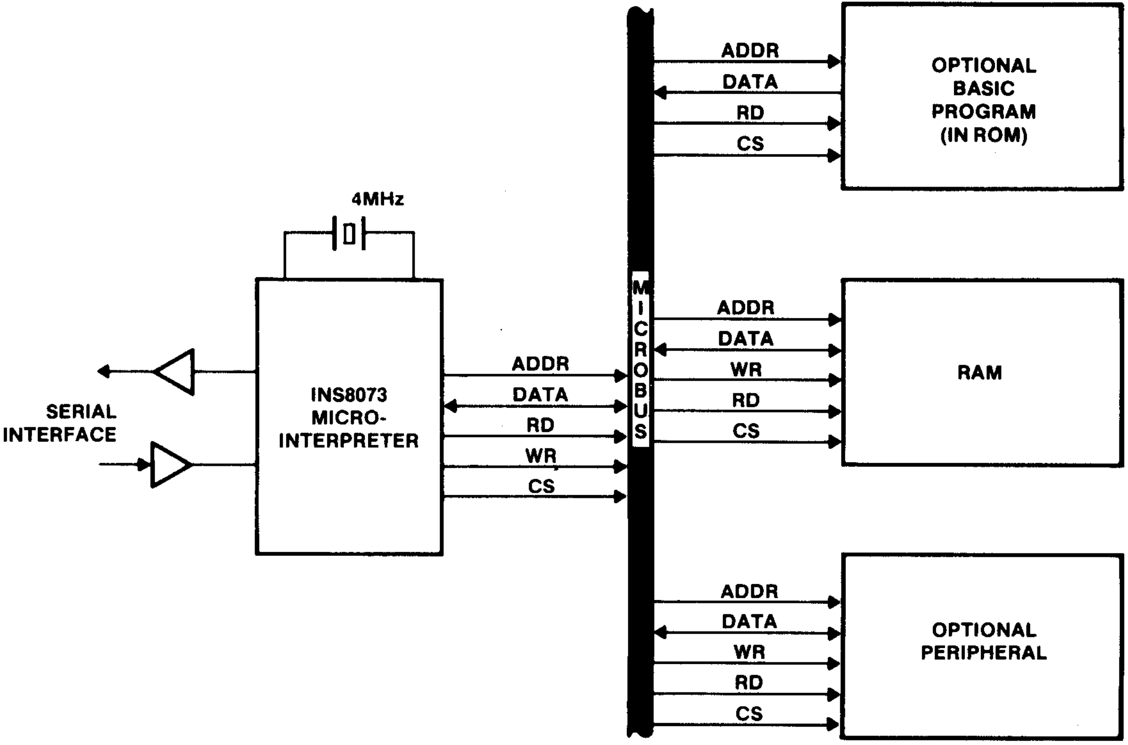
Features

- Reduces Software Effort in Microcomputer Applications
- Provides Easy Source Code Manipulation and Instant Program Revision
- Allows Immediate Mode Execution of Program Statements to Assist Program Checkout
- Provides Quick Sketches of Control Algorithms
- Facilitates User Hardware Checkout (Faster Than Assembly Language)

A REMINDER: NSC IS NOW SHIPPING THE XMOS INS 8073N. THE XMOS PROCESS IS THE SAME AS THE NMOS AS FAR AS PARAMETERS AND SPECIFICATIONS.

BUT, BECAUSE OF THE CHANGE IN PROCESS, THERE ARE TWO EXTERNAL COMPONENT CHANGES IN THE CLOCK CIRCUIT (1) THE 1K OHM RESISTOR SHOUDD BE 220 OHM (2) THE 27 PF CAPACITOR SHOULD BE AT 130 PF. THESE CHANGES DO NOT NECESSITATE BOARD LAYOUT CHANGES.

Simple System Diagram



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INTRODUCTION

National Semiconductor's INS8073 is a member of the INS8070 Family with an on-chip NSC Tiny BASIC interpreter. This interpreter resides in the chip's internal ROM, and offers the user the ability to program in a high level language in an absolute minimum system. The only other parts needed to program in NSC Tiny BASIC from a terminal are some RAM and RS-232 or TTY level translators. NSC Tiny BASIC is the revised version of NIBL/National's Industrial Basic Language.

For pinout details of the INS8073, refer to the INS8070 Data Sheet, or the 70-Series User's Manual. For a further description of the NSC Tiny BASIC language, refer to the NSC Tiny BASIC User's Manual.

COMMAND SUMMARY

NEW expr: Establishes a new start-of-program address equal to the value of 'expr'. NSC Tiny BASIC then executes its initialization sequence. If the value of 'expr' points to a ROM address, the NSC Tiny BASIC program which begins at this address will be automatically executed. Program memory is not altered by this command.

NEW: Sets the end-of-program pointer equal to the start-of-program pointer so that a new program may be entered. If a program already exists at the start-of-program address, it will be lost.

RUN: Runs the current program.

CONT: Continues execution of the current program from the point where execution was suspended (via a STOP, console interrupt, or reset).

LIST [expr]: Lists the current program (optionally starting at the line number specified by [expr]).

STATEMENT SUMMARY

REM anything: Remark (no operation).

CLEAR: Initializes all variables to 0, disables interrupts, and resets all stacks (GOSUB, FOR-NEXT, DO-UNTIL).

[LET] var = expr: Assigns expression value to variable.

[LET] STAT = expr: Sets the STATUS word equal to the least significant byte of 'expr'. When the STATUS word is used to enable interrupts at the hardware level, interrupt processing will be deferred for one statment.

[LET] @factor = expr: Sets the memory location pointed to by 'factor' equal to the least significant byte of 'expr'.

[LET] $factor = "string": Assigns a string in RAM starting at the address 'factor'. Strings are terminated by a carriage return.

[LET] $factor = $factor: Memory to memory assignment (copy).

PRINT expr: Prints the value of 'expr'.

PRINT "string": Prints the string.

PRINT $factor: Prints the string starting at the memory address 'factor'.

IF expr [THEN] statements: Remainder of the program line is executed if 'expr' is true (non-zero).

FOR var = expr TO expr [STEP expr]: FOR loop initialization. Loops may be nested to four levels.

NEXT var: FOR loop termination.

DO: DO loop initiation. DO loops may be nested to eight levels.

UNTIL expr: DO loop termination.

GO TO expr: Transfer control to statement number 'expr'.

GO SUB expr: Call subroutine at statement number 'expr'. Subroutines may be nested to eight levels.

RETURN: Return from subroutine.

INPUT var: Read value from console into variable.

INPUT $factor: Read string from console into memory beginning at address 'factor'.

LINK expr: Links to an assembly language subroutine which begins at address 'expr'. A "RET" instruction in this routine will cause continuation of the NSC Tiny BASIC program.

ON 1 or 2 expr: Interrupt processing definition. When interrupt number 1 or 2 occurs, NSC Tiny BASIC will execute a GOSUB beginning at line number 'expr'. If 'expr' is zero, the corresponding interrupt is disabled at the software level.

DELAY expr: Delay for 'expr' time units (nominally milliseconds, 1-1040). DELAY 0 gives the maximum delay of 1040 milliseconds.

STOP: Terminate program execution. A message is printed and the Microinterpreter returns to COMMAND mode.

OPERATOR SUMMARY

Arithmetic operators:	addition	+
	subtraction	-
	multiplication	*
	division	/
Relational operators:	less than	<
	greater than	>
	equal to	=>
	not equal to	<
	less than or equal to	<=
	greater than or equal to	>=
Logical operators:	logical AND	AND
	logical OR	OR
	logical NOT	NOT

FUNCTION SUMMARY

@factor: The memory/peripheral address for memory-I/O read/write operations.

STAT: STATUS register

TOP: Top-Of-Program address (first available memory address after end-of-program byte).

INC (x), DEC (x): Increment or Decrement a memory location (non-interruptable for multiprocessing).

MOD (x,y): Modulus function (remainder of x/y).

RND (x,y): Random number generator (in interval x,y).

MEMORY REQUIREMENTS

The NSC Tiny BASIC interpreter resides within the INS8073 on-chip ROM at memory locations X'0000-X'09FF. NSC Tiny BASIC uses all 64 bytes of on-chip RAM (X'FFC0-X'FFFF) and requires at least 256 bytes of external RAM.

RAM SEARCH FOLLOWING POWER-ON OR RESET

At power-on, or when the INS8073 is reset via the NRST pin, NSC Tiny BASIC automatically performs a nondestructive memory search. The search is conducted to determine the address range of the external RAM which is present. External RAM may be located anywhere in memory above the first 4K bytes (X'1000 or higher). The first 256 bytes of external RAM are used to store the Microinterpreter's variables, stacks and buffers. The remainder of the RAM may be used to store programs entered by the user. (Memory in which an NSC Tiny BASIC program is stored must be contiguous. The nondestructive memory search will identify only the first contiguous RAM block located at or above address X'1000.)

I/O devices may be memory mapped as long as they are not contiguous with RAM. Neither external RAM nor I/O devices may overlap or be contiguous with internal RAM at addresses X'FFC0-X'FFFF.

AUTOMATIC EXECUTION OF ROM PROGRAMS FOLLOWING POWER-ON OR RESET

After NSC Tiny BASIC has located external RAM, following power-on or reset, it tests address X'8000 to determine whether or not this location is RAM. If RAM is present at X'8000, the Microinterpreter will enter COMMAND mode. If address X'8000 is not RAM, the Microinterpreter will assume that it must be ROM, and will attempt to execute the program stored at this address. If there is no ROM at X'8000, this condition will be detected (the first valid character will not be the start of a line number), and NSC Tiny BASIC will enter COMMAND mode.

Since NSC Tiny BASIC will automatically execute a ROM based program at power-on, the INS8073 may be used as a stand-alone real-time controller.

BAUD RATE SELECTION

The Microinterpreter has built-in I/O routines to serially interface with a serial RS-232 terminal or TTY.

When the INS8073 is initialized, the desired baud rate is automatically selected by reading the contents of memory location X'FD00. To program the baud rate, this location must be decoded by external logic, and the appropriate logic levels supplied on data lines 1, 2, and 7. The baud rate is selected as follows:

D2	D1	Baud Rate
1	1	110
1	0	300
0	1	1200
0	0	4800

If the user-supplied subroutines are to be used for I/O, bit 7 of location FD00 should be zero (the other bits don't matter); and, locations FD01-FD02 contain the address of the character output routine. (Locations FD03-FD04 contain the address of the character input routine.) These address' should first be decremented by one, then stored in these locations low byte first.

Note from the above table that if only the 110 baud rate is required, pullup resistors on data lines D1, D2 and D7 represent the only external hardware required to select this baud rate.

The INS8073 F1 flag should be inverted and buffered to provide an RS-232 compatible voltage or a 20mA current output. The F2 flag can be used, if similarly buffered, to enable/disable the TTY reader relay.

The INS8073 will accept serial ASCII input data on its SA/INTA input; this configuration disallows one interrupt input. This data should be buffered to TTL levels without inversion.

PROGRAM MEMORY FORMAT

NSC Tiny BASIC programs are stored in ASCII characters. This feature simplifies the task of checking memory resident programs. Any nulls, line feeds, or blanks between program lines are ignored by the Microinterpreter. Source programs are terminated by any byte which is not one of the ASCII characters recognized by the Microinterpreter. (The byte X'7F is usually used as the end-of-program indicator.)

ENTRY OF NEW PROGRAMS INTO RAM FROM THE CONSOLE

Before a new program may be entered from the console, the Microinterpreter must be initialized by entering two commands. The first command is 'NEW' <address> which establishes the program starting address. The second command is 'NEW CR' (CR = carriage return) which establishes the initial value of the program ending address.

EXECUTION OF RAM RESIDENT AND ROM RESIDENT PROGRAMS

After a new program has been entered into RAM, it may be executed by entering the 'RUN' command. If a number of programs already exist in RAM, any one of them may be non-destructively executed by entering the 'NEW' <address> command followed by the 'RUN' command. The parameter

'<address>' must equal the starting address of the program to be executed.

It is unnecessary to enter the 'RUN' command in order to execute a ROM resident program. ROM programs will be executed immediately after the 'NEW'<address> command is entered.

ERROR CODE SUMMARY

If NSC Tiny BASIC encounters an error condition in RUN or COMMAND mode, it will alert the user by printing out 'ERROR', followed by an error number. Error numbers are defined as follows:

1. Out of memory
2. Statement used improperly
3. Unexpected character (after legal statement)
4. Syntax error
5. Value (format) error
6. Ending quote missing from string
7. GO target line does not exist
8. RETURN without previous GOSUB
9. Expression or FOR-NEXT, DO-UNTIL or GOSUB-RETURN nested too deeply
10. NEXT without previous matching FOR
11. UNTIL without previous DO
12. Division by zero

NOTES:

1. *In the instruction syntax, items in brackets* **[...]** *are optional.* '***Expr***' stands for any expression; '***var***' stands for any variable; '***factor***' stands for any of the following: a single number, a single variable, a single function, or any expression enclosed in parenthesis. The following are '***factors***':

A decimal number	(-32767 to +32767)
A hexadecimal number	(#hexvalue)
A variable	(A to Z)
Parenthesized expressions	(expr)

2. *Variables are single-letters, A to Z.*
3. *All arithmetic is 16-bit signed integer* **(-32767** *to* **+32767)**.
4. *All statements except INPUT may be used in COMMAND mode.*
5. *Multiple statements may be used on the same program line, with statements separated by a colon* **(:)**. **The colon** *is especially useful as it allows FOR-NEXT and DO-UNTIL to be used in the COMMAND mode.*
6. *The PRINT and INPUT statements usually specify a list of one or more items* **(***variables, etc.***)** *which are separated by commas. If the PRINT list ends with a semicolon* **(;)**, *the carriage return/line feed at the end of the line will be surpressed.*
7. *The required console response to an executing INPUT statement is a list of one or more expressions* (with a single number as the simplist case). *Expressions in an INPUT list may be separated by blanks or commas. There must be at least as many expressions in the input list as variables in the INPUT statement. If a console input error is detected, a message will be printed and the INPUT statement re-executed. The correct response to an 'INPUT $factor' statement is a string which is terminated by a carriage return.*

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INS807X Functional Pin Description

The following describes the function of all INS807X input/output pins. For brevity, the INS807X designator is used to refer to all members of the family.

INPUT SIGNALS

Reset (NRST)

Active low RESET input. This pin initializes the INS807X by resetting the program counter (PC) and the stack pointer (SP) to zero (low). All bits in the Status Register (except SA and SB) are also reset to zero. This input is buffered by a T^2L compatible Schmitt Trigger, allowing slow rise and fall times.

Hold (NHOLD)

Active low external memory cycle extend input for slow memories and slow peripherals. Also used for single memory cycle execution. NHOLD affects READ/WRITE cycles to external memory only.

Sense A/Interrupt A (SA/INTA)

Provides a T^2L compatible Schmitt Trigger buffered sense input which sets/resets the Sense A bit (SA) in the status register. When interrupts are enabled (IE = 1 in the STATUS register) this pin also acts as a trailing edge triggered interrupt input.

Sense B/Interrupt B (SB/INTB)

Similar operation as SA/INTA. Since SA/INTA has priority over SA/INTB, if both arrive simultaneously, Interrupt A will be serviced first.

Enable Input (NENIN)

Active low bus enable input to the on-chip bus allocation logic. For DMA and multiprocessing applications this logic allows bus access to be granted or denied to the INS807X. Devices which can share the bus include other INS807X processors, INS8060 processors, DP8350 CRT Controller and DMA logic. NENIN affects INS807X operation as follows:

1) If NENIN is high, INS807X sets NENOUT high and is denied access to the bus.

2) If NENIN is low and the INS807X is holding NBREQ low, INS807X sets NENOUT high and is granted access to the bus.

3) If NENIN and NBREQ are both low and the INS807X is not holding NBREQ low, INS807X sets NENOUT low, and is denied access to the bus.

Power

V_{CC} = +5V, Pin 40

V_{SS} = GND, Pin 20

OUTPUT SIGNALS

Address Bus (A_{15} - A_0)

TRI-STATE™ address outputs for all external memory READ and WRITE operations. These outputs are normally in high-impedance state except during external memory READ and WRITE operations (Refer to Timing Waveforms.)

Write Data Strobe (NWDS)

TRI-STATE active low WRITE strobe output. NWDS goes low during an external memory WRITE operation. NWDS is in the high-impedance state when an external memory WRITE operation is not in progress. (Refer to Write Cycle Timing.)

Read Data Strobe (NRDS)

TRI-STATE active low READ strobe output. NRDS goes low during an external memory READ operation. NRDS is in the high-impedance state when an external memory READ operation is not in progress. (Refer to Read Cycle Timing.)

Enable Output (NENOUT)

Active low bus enable output from the on-chip bus allocation logic. INS807X controls NENOUT as follows:

1) If NBREQ is low but INS807X is not holding it low, NENOUT = NENIN.

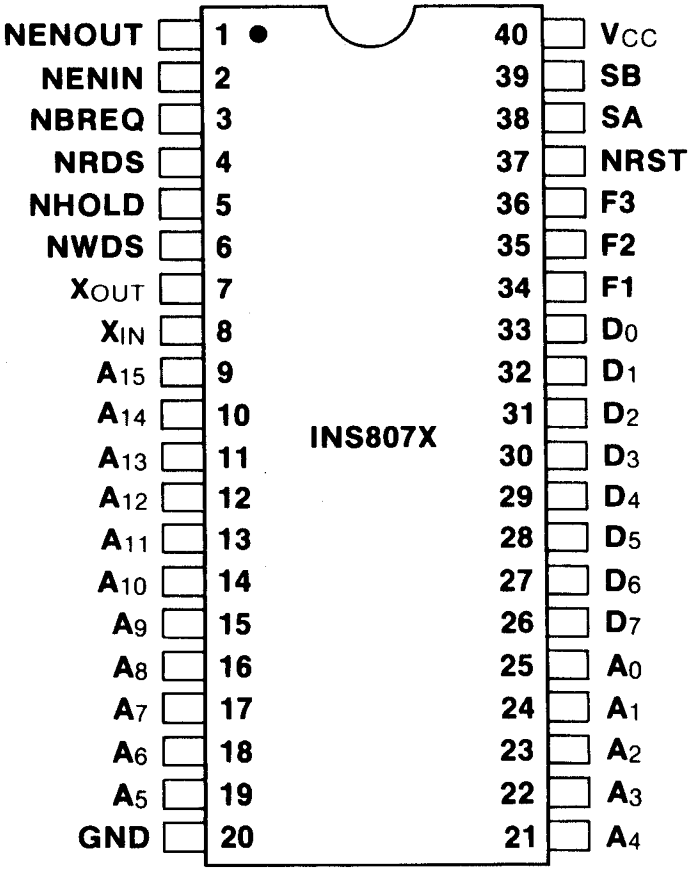
INS807X Functional Pin Description - Cont'd.

2) If NEBREQ is low and INS807X is holding it low, NENOUT = high.

3) If NBREQ = high, NENOUT = high.

Flags 1, 2, 3	(F1, F2, F3)	Flag outputs which can be set high/low by writing into the corresponding flag bits of the status register.
	BIDIRECTIONAL SIGNALS	
Bus Request	(NBREQ)	Bidirectional Bus Request input/output. NBREQ serves as an input/output to/from the on-chip bus allocation logic. When NBREQ is high (NBREQ acts as an input) and the processor requires use of the bus, the processor issues a bus request by pulling NBREQ low (NBREQ acts as an output.)
Data Bus	(D_0 - D_7)	Bidirectional TRI-STATE data bus input/output. These lines are normally in the high-impedance state except during external memory READ and WRITE operations. They provide input data during external memory READ; they provide output data during external memory WRITE.
Clock Inputs	(X_{IN}, X_{OUT})	On-chip clock generator input/outputs (see figure 1). The on-chip clock generator will operate with external crystal or RC inputs connected between X_{IN} and X_{OUT}. The on-chip clock generator may be disabled by supplying a T^{2}L level clock input on X_{IN}. In all modes a buffered T^{2}L level clock output is always available at X_{OUT}.

PIN CONFIGURATION


NENOUT 1
NENIN 2
NBREQ 3
NRDS 4
NHOLD 5
NWDS 6
X_{OUT} 7
X_{IN} 8
A_{15} 9
A_{14} 10
A_{13} 11
A_{12} 12
A_{11} 13
A_{10} 14
A_9 15
A_8 16
A_7 17
A_6 18
A_5 19
GND 20
40 V_{CC}
39 SB
38 SA
37 NRST
36 F3
35 F2
34 F1
33 D_0
32 D_1
31 D_2
30 D_3
29 D_4
28 D_5
27 D_6
26 D_7
25 A_0
24 A_1
23 A_2
22 A_3
21 A_4
INS807X