VERSION 2

1. MODEL 6500 CPU BOARD

OVERVIEW

The Model 6500 CPU Board is a self-contained computer system in a small, easily-packaged form. All the components necessary for a basic computer system are combined on this single board, along with the capability of expanding the CPU board's function by adding other 6500-Family boards to the system.

The 6500 CPU Board uses the Rockwell 6500 family of integrated circuits, including the 6502 microprocessor. The 6502 microprocessor is a high-performance, general-purpose 8-bit microprocessor that has found wide acceptance in industrial control and OEM applications.

In addition to the microprocessor CPU (central processing unit), the board contains the following components:

- Sockets for up to 20K of ROM/EPROM (read-only memory)
- 1K or 4K of RAM (read-write memory)
- 72 lines of programmable parallel I/O
- 5 programmable interval timers
- 2 programmable shift registers

The extensive input/output capabilities of the CPU board are provided using the Rockwell 6500 chip set. The interval timers, shift registers, and 72 lines of programmable I/O are provided by two 6522 versatile interface adapters (VIAs), one 6520 peripheral interface adapter (PIA), and one 6532 RAM-I/O-Timer (RIOT).

The Cubit 6500 CPU Board is software-compatible with the Rockwell AIM-65 and Microflex computers. Application programs developed on the AIM-65 may be transferred directly to the Cubit 6500 computer without modification. The Cubit 6500 CPU is also compatible with the keyboard, display, and printer driver routines in the AIM-

65 monitor, when the 6500 CPU is used with the Cubit keyboard, display and printer peripherals (See Chapters 5, 6, and 7 for further descriptions of these peripherals).

The ability to add expansion modules allows the 6500 CPU Board to be used in a wide variety of industrial or consumer applications. Succeeding chapters of this manual discuss the expansion modules and peripherals which are available, including a 20-character alpha-numeric display, a 20-character-wide printer-plotter, expansion RAM and ROM boards, and additional input/output capabilities.

THEORY OF OPERATION

The Model 6500 CPU Board uses a simple and easily-understandable system bus architecture. Each component of the CPU Board communicates with the other components on the board using this bus. The CPU Board consists of these five functional components:

- CPU (6502 microprocessor)
- RAM (read-write memory)
- ROM (read-only memory)
- I/O (programmable input/output)
- Programmable interval timers

The organization of these components around the system bus is depicted in Figure 1-1. This system bus is actually composed of three busses; an 8-bit data bus, a 16-bit address bus, and a 12-bit control bus. The entire bus is made available for off-board system expansion at the expansion connector, J3. This bus organization and the expansion connector are discussed further in the section "Using the Expansion Bus", later in this chapter.

The 6502 Microprocessor

The 6500 CPU Board uses a 6502 microprocessor, operating at a 1 MHz clock frequency (standard) or 2 MHz (optional). This general-purpose microprocessor features a 64-kilobyte memory addressability and a powerful 56-command, 13-address-mode instruction set.

Readers should consult the Rockwell R6500 Programming Manual for a complete explanation of this microprocessor's features, instruction set, and other programming considerations.

Read-Only and Read-Write Memory

The Model 6500 CPU Board has sockets for up to 20 kilobytes of non-volatile ROM (read-only) memory for program storage. The five on-board

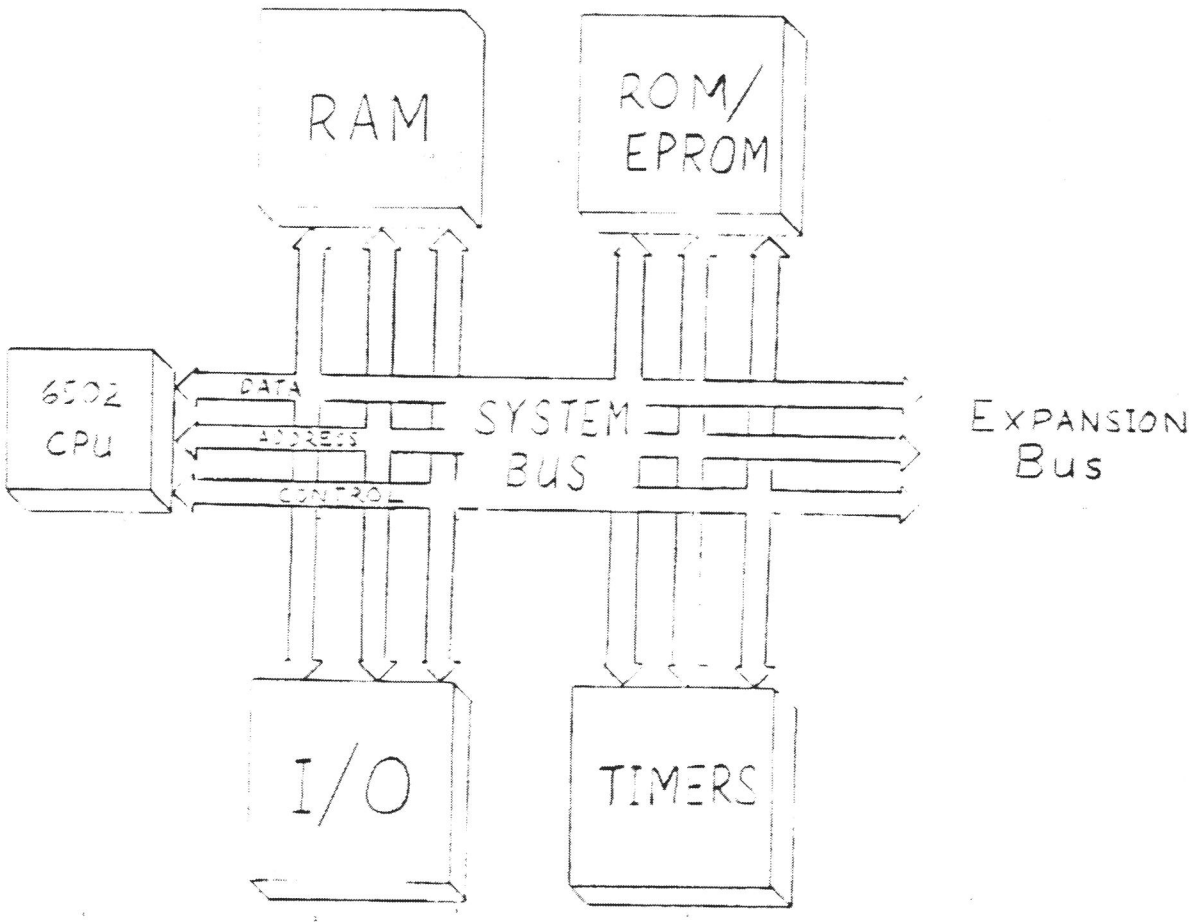


Figure 1-1. Model 6500 CPU Board Block Diagram

sockets can accept either 2332-type ROMs or 2532 or 2716-type EPROMs.

Because the system's interrupt request and power-on reset vectors are located in the highest addressable ROM locations, a 4K ROM or EPROM (either a 2332 ROM or 2532 EPROM) must be installed in socket Z22.

The 6500 CPU Board also provides sockets for up to 4 kilobytes of RAM (read-write) memory. The 6500 board is shipped with a minimum of 1 kilobyte of 2114-type static RAM installed. The board is also available with the full 4 kilobytes of RAM installed as an option.

Users who wish to install additional ROM or RAM memory after receiving the 6500 Board should refer to the sections "ROM Memory Installation" and "RAM Memory Installation", later in this chapter.

Programmable Input/Output (I/O)

Eight fully-programmable 8-bit parallel I/O ports are provided on the CPU Board. Four of these ports are equipped with two additional handshake/control lines, for a total of seventy-two lines of I/O. Each of the sixty-four data I/O lines is individually programmable as either an input or an output line. This feature allows maximum flexibility when configuring the board's input/output functions.

In addition to these eight parallel ports, the CPU Board contains two programmable shift registers. These shift registers allow automatic parallel-to-serial and serial-to-parallel data conversion without tying up the processor. The timing of the shift registers may be controlled by signals either generated internal to the 6500 board or generated externally. Each shift register operates independently and uses one of the data I/O lines to connect to external devices.

This collection of I/O ports is implemented on four R6500-family integrated circuit chips: two 6522 versatile interface adapters (VIA), one 6520 peripheral interface adapter (PIA), and one 6532 RAM-I/O-Timer (RIOT). Each of these Rock-

well chips is discussed individually in the Rockwell R6500 Hardware Manual. The 6520, 6522, and 6532 chips are detailed in sections 5, 6, and 8 of this reference manual, respectively. The manual discusses the different electrical characteristics of some of the port I/O lines, as well as the configuration and programming for each port.

The eight I/O ports and their associated control registers are accessed via software as a sequence of memory addresses. Further information regarding the programming and use of these ports is given in the discussion "Using the Input/-Output Capabilities" later in this chapter.

Programmable Interval Timers

Five programmable interval timers are included as part of the two 6522 VIAs and the 6532 RAM-I/O-Timer. The four available 16-bit timers are cascadable in pairs to provide two independent timers. These programmable timers may be used to interrupt the processor for system timing functions. Alternatively, certain of these timers may be used in conjunction with particular I/O lines to generate external timing signals, to control the operation of the shift registers, or to count external events. The fifth timer is a combined divide-down counter and a programmable 8-bit counter, which may be used for generating processor interrupts at intervals of up to one-quarter of a second.

Specific information on the configuration of these counters is given in the section "Using the Input/Output Capabilities" later in this chapter. Further information regarding these timing capabilities and their programming is available in the Rockwell R6500 Hardware Manual, under the sections covering the 6522 and 6532 circuits.

INSTALLATION

CPU Board Preparation

The 6500 CPU Board is shipped from the factory fully assembled and ready for use. No jumpering or reconfiguration of any kind is necessary. Typically, all that is required to prepare the CPU Board for use is to install the particular ROMs or EPROMs which contain the stored programs for the computer.

ROM Memory Installation

Five ROM sockets on the CPU Board accept up to 20 kilobytes of user ROM. If the AIM-65 Monitor ROMs were ordered with the 6500 CPU Board, these ROMs are shipped already installed in sockets Z22 and Z23 on the board. All other ROMs must be installed by the user.

Figure 1-2 shows the software addresses which correspond to the five ROM sockets. Whenever ROMs are installed, you should make sure that each ROM is inserted in its proper socket location.

To install a ROM or EPROM in the CPU Board, first make sure that no power is connected to the board. Inspect the pins on the ROM chip to ensure that all are clean and straight. Then, while supporting the back of the CPU Board, carefully insert the chip into its proper socket. Be careful to use the correct chip orientation: pin #1 points away from the expansion connector side of the board. All chips must be installed with pin #1 oriented in the same direction as pin #1 of all the other chips on the board.

Before connecting power to the system, make a final inspection to ensure that none of the ROM pins have been bent and that all of the ROMs are inserted completely into their sockets.

ROM Socket	Address Space (Hexadecimal)
Z22	F000 - FFFF
Z23	E000 - EFFF
Z24	D000 - DFFF
Z25	C000 - CFFF
Z26	B000 - BFFF

Figure 1-2. Read-Only Memory (ROM) Socket Address Spaces

RAM Socket	Address Space (Hexadecimal)
Z2, Z3	0000 - 03FF
Z6, Z7	0400 - 07FF
Z11, Z12	0800 - 0BFF
Z17, Z18	0C00 - 0FFF

Figure 1-3. Read-Write Memory (RAM) Socket Address Spaces

RAM Memory Installation

The CPU Board is shipped with either one or four kilobytes of RAM installed. If the board has been been supplied with less than four kilobytes of RAM, more 2114-type RAM may be installed by the user if desired. Figure 1-3 shows the software addresses of each pair of RAM sockets. Consult the 6500 CPU Board layout diagram, Figure 1-10, if unsure of the location of a designated socket. Once again, all RAMs and ROMs are installed with pin #1 oriented in the same direction as pin #1 of all the other circuits on the board. Integrated circuits must not be inserted or removed from their sockets while power is being applied to the board.

Installation of the System

To install the CPU board for operation as part of a system, the board must be connected to each part of the system with which it must interact. These connections will vary considerably from one application to the next, but in each case, the connections may be described under each of the following categories:

- Power connection to the CPU Board
- I/O connection to the CPU Board
- Expansion module connection to the CPU board

The connection of power to the CPU Board is straightforward and is covered immediately below. The connection of input/output lines is more involved and is covered in the next section of this chapter. Finally, the connection of expansion modules to the CPU is discussed in a subsequent section of this chapter.

Power Connection

The 6500 CPU Board does not require a card cage. However, some provision must be made to provide +5 volts DC and a Ground connection to pins 21 and 22 of the expansion connector, J3. This is easily accomplished with a 44-pin edge connector which mates to the edge of the CPU Board. The expansion connector J3 is discussed more com-

pletely in the section which follows, entitled "Using the Expansion Bus". Figure 1-8 in that section contains a complete description of the signals on each pin of this connector.

If expansion modules are to be used in the system, a motherboard and typically a card cage are used to connect the expansion modules to the CPU Board's expansion bus. In this case, the motherboard or card cage will have provided for the connection of power to the computer system. The appropriate instructions supplied with the motherboard should be followed when connecting power to the system.

Before applying power to any newly-connected system, use an ohmmeter to check the continuity between power-supply ground and CPU-Board ground. This will ensure that the connectors have been properly connected.

The single +5 volts DC and Ground are the only power connections necessary to run the 6500 CPU Board. The +12v and -12v connectins on the expansion connector are not used by the computer.

The +5 volt supply should be regulated to within five percent of nominal voltage, with a capacity for up to two amperes of current. The actual current drawn by the system depends on the amount of RAM and ROM installed, and the number of expansion modules included in the system.

USING THE INPUT/OUTPUT CAPABILITIES

The 6500 CPU Board contains a wide assortment of I/O and timing capabilities, including eight programmable parallel I/O ports, two programmable shift registers, and five programmable interval timers. These functions are provided by four integrated circuits: two 6522 versatile interface adapters, one 6520 peripheral interface adapter, and one 6532 RAM-I/O-Timer.

Each of these circuits is discussed in lengthy detail in the Rockwell 6500 Hardware Manual.

All the data and control registers for these I/O functions are memory-mapped; that is, each register is accessed by the computer as an address in memory. This means that programming input/-output operations consists merely of writing and reading the appropriate memory locations. Figure 1-4 shows the particular memory addresses associated with the various I/O ports and operations. Once again, consult the Rockwell R6500 Hardware Manual for the meaning and use of each of the I/O commands and operations described in the Figure.

Memory Address	I/O Register Description	Device Number
A000	Device A-Port B Data Register Data I/O Signals A-PB0 through A-PB7.	Z1 (6522)
A001	Device A-Port A Data Register Data I/O Signals A-PA0 through A-PA7. (see also memory address A00F)	Z1 (6522)
A002	Data Direction Register; Device A-Port B 0 = data input 1 = data output for corresponding bit in data register	Z1 (6522)
A003	Data Direction Register; Device A-Port A 0 = data input 1 = data output for corresponding bit in data register	Z1 (6522)
A004	Device A-Timer 1 Low-Order Counter Read operations read low-order counter Write operations load low-order latch	Z1 (6522)
A005	Device A-Timer 1 High-Order Counter Read operations read the high-order counter Write operations load the high-order latch and load the counters from the low and high-order latches	Z1 (6522)
A006	Device A-Timer 1 Low-Order Latch Read or Write the low-order latch--these operations do not affect the counters	Z1 (6522)
A007	Device A-Timer 1 High-Order Latch Read or Write the high-order latch--these operations do not affect the counters	Z1 (6522)
A008	Device A-Timer 2 Low-Order Counter Read operations read low-order counter Write operations load low-order latch	Z1 (6522)

Figure 1-4. I/O Data and Control Register Memory Map

Memory Address	I/O Register Description	Device Number
A009	Device A-Timer 2 High-Order Counter Read operations read the high-order counter Write operations load the high-order latch and load the counters from the low and high-order latches	Z1 (6522)
A00A	Device A-Shift Register Data	Z1 (6522)
A00B	Device A-Auxilliary Control Register ACR7 - Timer 1 Output Enable ACR6 - Timer 1 One-Shot or Free Mode ACR5 - Timer 2 One-Shot or Pulse count Mode ACR4 - Shift Register Input-Output Select ACR3 - Shift Register Timing Select ACR2 - Shift Register Timing Select ACR1 - Port B Latch Enable ACR0 - Port A Latch Enable	Z1 (6522)
A00C	Device A Peripheral Control Register PCR7 - A-CB2 Control Bit PCR6 - " " " PCR5 - " " " PCR4 - A-CB1 Pos/Neg-Edge Select PCR3 - A-CA2 Control Bit PCR2 - " " " PCR1 - " " " PCR0 - A-CA1 Pos/Neg-Edge Select	Z1 (6522)
A00D	Device A Interrupt Flag Register 7 6 5 4 3 2 1 0 IRQ T1 T2 CB1 CB2 SR CA1 CA2 Read operations: 0 = flag cleared 1 = flag set Write operations: 0 = flag unchanged 1 = flag cleared except for IRQ (bit 7). See R6500 Hardware Manual for explanation.	Z1 (6522)

Figure 1-4. I/O Data and Control Register Memory Map (cont'd)

Memory Address	I/O Register Description	Device Number
A00E	Device A Interrupt Enable Register 7 6 5 4 3 2 1 0 S/C T1 T2 CB1 CB2 SR CA1 CA2 Read operations: 0 = flag disabled 1 = flag enabled Write operations; 0 = enable unchanged With bit 7=0; 1 = enable cleared With bit 7=1; 1 = enable set	Z1 (6522)
A00F	Device A-Port A Data Register (without Handshake Control; see also memory address A001)	Z1 (6522)
A400 -A47F	Read/Write Random Access Memory	Z33(6532)
A480	Device C-Port A Data Register	Z33(6532)
A481	Data Direction Register; Device C-Port A 0 = Data Input 1 = Data Output for corresponding bit in data register	Z33(6532)
A482	Device C-Port B Data Register	Z33(6532)
A483	Data Direction Register; Device C-Port B 0 = Data Input 1 = Data Output for corresponding bit in data register	Z33(6532)
A484	Disable Edge-Detecting Interrupt (C-PA7) Write operation disables interrupt; bus data is discarded.	Z33(6532)
A485	Disable Edge-Detecting Interrupt (C-PA7) This location functions identically to location A484.	Z33(6532)
A486	Enable Negative-Edge-Detecting Interrupt Write operation enables interrupt on negative transition of C-PA7. Read operation clears interrupt flag: bit 7 = timer flag bit 6 = C-PA7 flag	Z33(6532)

Figure 1-4. I/O Data and Control Register Memory Map (cont'd)

Memory Address	I/O Register Description	Device Number
A487	Enable Positive-Edge-Detecting Interrupt Write operation enables interrupt on positive transition of C-PA7. Read operation clears interrupt flag.	Z33(6532)
A494	Timer Counter, Divide-by-1; Disable interrupt. Clock input divided by 1 Write operations load the counter registers, disable interrupt. Read operations read the counter, disable counter interrupt.	Z33(6532)
A495	Timer Counter, Divide-by-8; Disable interrupt. Clock input divided by 8 Write operations load the counter registers, disable interrupt. Read operations read the counter, disable counter interrupt.	Z33(6532)
A496	Timer Counter, Divide-by-64; Disable interrupt. Clock input divided by 64	Z33(6532)
A497	Timer Counter, Divide-by-1024; Disable interrupt. Clock input divided by 1024	Z33(6532)
A49C	Timer Counter, Divide-by-1; Enable interrupt. Clock input divided by 1	Z33(6532)
A49D	Timer Counter, Divide-by-8; Enable interrupt. Clock input divided by 8	Z33(6532)
A49E	Timer Counter, Divide-by-64; Enable interrupt. Clock input divided by 64	Z33(6532)
A49F	Timer Counter, Divide-by-1024; Enable interrupt. Clock input divided by 1024	Z33(6532)
A800	Device B-Port B Data Register	Z32(6522)

* The device registers in locations A800-A80F have nearly duplicate functions to the registers in locations A000-A00F. The explanation of each register function is not reproduced here. You may refer to the explanations given previously in this table for locations A000-A00F.

Figure 1-4. I/O Data and Control Register Memory Map (cont'd)

Memory Address	I/O Register Description	Device Number
A801	Device B-Port A Data Register (see also memory address A80F)	Z32(6522)
A802	Data Direction Register; Device B-Port B	Z32(6522)
A803	Data Direction Register; Device B-port A	Z32(6522)
A804	Device B-Timer 1 Low-Order Counter	Z32(6522)
A805	Device B-Timer 1 High-Order Counter	Z32(6522)
A806	Device B-Timer 1 Low-Order Latch	Z32(6522)
A807	Device B-Timer 1 High-Order Latch	Z32(6522)
A808	Device B-Timer 2 Low-Order Counter	Z32(6522)
A809	Device B-Timer 2 High-Order Counter	Z32(6522)
A80A	Device B-Shift Register Data	Z32(6522)
A80B	Device B-Auxilliary Control Register	Z32(6522)
A80C	Device B-Peripheral Control Register	Z32(6522)
A80D	Device B-Interrupt Flag Register	Z32(6522)
A80E	Device B-Interrupt Enable Register	Z32(6522)
A80F	Device B-Port A Data Register (without Handshake Control; see also memory address A801)	Z32(6522)
AC00	Device D-Port A Data Register/Data Direction Register When Data Direction Register selected: 0 = data input 1 = data output for corresponding bit in Data Register	U1 (6520)

Figure 1-4. I/O Data and Control Register Memory Map (cont'd)

Memory Address	I/O Register Description	Device Number
AC01	Device D-Port A Control Register CRA7 - Interrupt flag set by D-CA1 CRA6 - Interrupt flag set by D-CA2 CRA5 - control bit selects D-CA2 operation; refer to Hardware Manual CRA4 - see CRA5 above. CRA3 - see CRA5 above. CRA2 - Data Direction Register Access 0 = select Data Direction Register 1 = select Port A Data Register CRA1 - control bit selects D-CA1 operation; refer to Hardware Manual CRA0 - see CRA1 above.	U1 (6520)
AC02	Device D-Port B Data Register/Data Direction Register When Data Direction Register selected: 0 = data input 1 = data output for corresponding bit in Data Register	U1 (6520)
AC03	Device D-Port B Control Register See explanation of Port A control register above.	U1 (6520)

Figure 1-4. I/O Data and Control Register Memory Map (cont'd)

I/O Connector Description

Each of the sixty-four data I/O lines and the eight handshake/control lines appears at one of three I/O connectors; J1, J2, and J4. Figures 1-5 through 1-7 document the pin assignments on each of these three connectors and their corresponding I/O lines or signals.

To avoid confusion when wiring I/O connections, the location of pin #1 for each of these connectors has been clearly silk-screened on the component side of the printed circuit board. To further avoid ambiguity, square solder pads have been used to denote pin #1 for each of these three connectors, whereas all other solder pads on the underside of the board are round. The CPU Board layout diagram, Figure 1-9, found at the end of this chapter, also denotes the position of pin #1 for each connector.

The lines on each of the three connectors have been organized so that connector J2 may be used to support the Cubit Model 6521 Printer/Plotter, and so that connector J4 may be used to support the Cubit Model 6520 Display, Model 6550 Keyboard, and Model 6551 Keyboard/Display. Each of these modules is covered individually in a later chapter of this manual. Of course, you may choose not to include these peripheral modules in a particular system for a given application. In this case, any of the seventy-two I/O lines may be used for user-defined purposes.

Configuring the Programmable Timers

The programmable timers provided on the CPU Board may be configured for use in a variety of ways. To generate external timing signals, both Device A-Timer 1 and Device B- Timer 1 may be programmed to generate square-wave signals on I/O lines A-PB7 and B-PB7 (pins 32 and 4 of the User Application I/O Connector J1, respectively). To count external events, Device A-Timer 2 and Device B-Timer 2 can be programmed to count negative transitions on I/O lines A-PB6 and B-PB6 (pins 31 and 3 of Connector J1, respectively). Pairs of these timers may be cascaded together by connecting

Connector Pin	Pin Signal	I/O Register Address	Device Number
1	GND	----	----
3	B-PB6	A800-bit 6	Z32 (6522)
5	B-PB4	A800-bit 4	Z32 (6522)
7	B-PB2	A800-bit 2	Z32 (6522)
9	$\overline{RES}$	----	Z15 (7433)
11	$\overline{RESIN}$	----	Z10 (8224)
13	no connection		
15	A-PA2	A001-bit 2	Z1 (6522)
17	A-PA3	A001-bit 3	Z1 (6522)
19	A-PA4	A001-bit 4	Z1 (6522)
21	A-PA5	A001-bit 5	Z1 (6522)
23	A-PA6	A001-bit 6	Z1 (6522)
25	A-PB0	A000-bit 0	Z1 (6522)
27	A-PB2	A000-bit 2	Z1 (6522)
29	A-PB4	A000-bit 4	Z1 (6522)
31	A-PB6	A000-bit 6	Z1 (6522)
33	A-CB1	----	Z1 (6522)
2	+5 VDC	----	----
4	B-PB7	A800-bit 7	Z32 (6522)
6	B-PB5	A800-bit 5	Z32 (6522)
8	B-PB3	A800-bit 3	Z32 (6522)
10	B-CA2	----	Z32 (6522)
12	no connection		
14	no connection		
16	A-PA0	A001-bit 0	Z1 (6522)
18	A-PA1	A001-bit 1	Z1 (6522)
20	A-CA2	----	Z1 (6522)
22	A-CA1	----	Z1 (6522)
24	A-PA7	A001-bit 7	Z1 (6522)
26	A-PB1	A000-bit 1	Z1 (6522)
28	A-PB3	A000-bit 3	Z1 (6522)
30	A-PB5	A000-bit 5	Z1 (6522)
32	A-PB7	A000-bit 7	Z1 (6522)
34	A-CB2	----	Z1 (6522)

Figure 1-5. User Application I/O Connector J1.

Connector Pin	Pin Signal	I/O Register Address	Device Number
1	GND	----	----
3	B-PA1	A801-bit 1	Z32 (6522)
5	B-PA2	A801-bit 2	Z32 (6522)
7	B-PA4	A801-bit 4	Z32 (6522)
9	B-PA6	A801-bit 6	Z32 (6522)
11	B-CA1	----	Z32 (6522)
13	B-PB1	A800-bit 1	Z32 (6522)
15	B-CB2	----	Z32 (6522)
2	+5 VDC	----	----
4	B-PA0	A801-bit 0	Z32 (6522)
6	no connection		
8	B-PA3	A801-bit 3	Z32 (6522)
10	B-PA5	A801-bit 5	Z32 (6522)
12	B-PA7	A801-bit 7	Z32 (6522)
14	B-PB0	A800-bit 0	Z32 (6522)
16	B-CB1	----	Z32 (6522)

Figure 1-6. Printer I/O Connector J2.

Connector Pin	Pin Signal	I/O Register Address	Device Number
1	GND	----	----
3	D-PB1	AC02-bit 1	U1 (6520)
5	D-PB3	AC02-bit 3	U1 (6520)
7	D-PB5	AC02-bit 5	U1 (6520)
9	D-PB7	AC02-bit 7	U1 (6520)
11	D-PA0	AC00-bit 0	U1 (6520)
13	D-PA1	AC00-bit 1	U1 (6520)
15	D-PA2	AC00-bit 2	U1 (6520)
17	D-PA3	AC00-bit 3	U1 (6520)
19	C-PB7	A482-bit 7	Z33 (6532)
21	C-PB1	A482-bit 1	Z33 (6532)
23	C-PA4	A480-bit 4	Z33 (6532)
25	C-PA5	A480-bit 5	Z33 (6532)
27	C-PB5	A482-bit 5	Z33 (6532)
29	C-PB4	A482-bit 4	Z33 (6532)
31	C-PB3	A482-bit 3	Z33 (6532)
33	C-PB2	A482-bit 2	Z33 (6532)
2	+5 VDC	----	----
4	D-PB0	AC02-bit 0	U1 (6520)
6	D-PB2	AC02-bit 2	U1 (6520)
8	D-PB4	AC02-bit 4	U1 (6520)
10	D-PB6	AC02-bit 6	U1 (6520)
12	D-PA4	AC00-bit 4	U1 (6520)
14	D-PA5	AC00-bit 5	U1 (6520)
16	D-PA6	AC00-bit 6	U1 (6520)
18	D-PA7	AC00-bit 7	U1 (6520)
20	C-PA2	A480-bit 2	Z33 (6532)
22	C-PA3	A480-bit 3	Z33 (6532)
24	C-PA1	A480-bit 1	Z33 (6532)
26	C-PA6	A480-bit 6	Z33 (6532)
28	C-PB6	A482-bit 6	Z33 (6532)
30	C-PA7	A480-bit 7	Z33 (6532)
32	C-PA0	A480-bit 0	Z33 (6532)
34	C-PB0	A482-bit 0	Z33 (6532)

Figure 1-7. Keyboard-Display I/O Connector J4.

pins 31 and 32, or pins 3 and 4, of the Application Connector J1. Each pair of timers cascaded in this manner can be programmed to operate as a 32-bit counter.

Interrupt Processing

The timers, handshake/control lines, and the shift register on Device A (6522-Z1), and the timer and edge-detecting circuit (C-PA7) of Device C (6532-Z33), are all capable of generating processor interrupts. Individual interrupts can be enabled and disabled by the processor under software control. Interrupt processing on the CPU Board is handled by the processor polling the interrupt flag registers of the active devices to determine which device is requesting attention. Interrupt processing is covered in detail in Chapter 11 of the Rockwell R6500 Programming Manual, including a sample interrupt handling routine.

USING THE EXPANSION BUS

The Model 6500 CPU Board can support considerable system expansion. Functions can be added to the system by connecting expansion modules to the expansion bus connector on the CPU Board. RAM memory, ROM memory, and I/O expansion modules are only a few of the expansion modules currently available.

When connecting multiple Cubit expansion boards to the CPU Board, a motherboard such as the Cubit Model 6540 or Model 6541 Motherboard is recommended. These Motherboards connect the Expansion bus signals of each board to the Expansion connector on the CPU Board. Chapter 9 of this manual discusses these motherboards in more detail.

Since most of the signals on the Expansion Bus are unbuffered, care should be used when attaching several boards to the system. The manufacturer does not recommend placing more than two LS TTL loads on any signal coming from the Expansion Bus.

Expansion boards from other manufacturers or user-designed circuitry for custom applications may also be attached to the CPU Board using the expansion bus. Since damage may result from using incompatible boards, users should make sure that any devices that are attached to the expansion bus are strictly compatible with the bus signals.

The Expansion Bus Connector

The expansion bus connector, J3, is located on the edge of the CPU Board. The entire internal system bus appears at this connector, including all the address, data, and control lines necessary to connect devices to the 6502 microprocessor. Since many of these signals are unbuffered and are driven directly by the 6502 microprocessor, proper care should be taken when handling the 6500 CPU Board. Never insert or remove a board from an edge connector while power is being applied to the connector.

Figure 1-8 describes the signals which appear on each pin of the expansion connector, J3. For a more complete description of the electrical and timing characteristics of these signals, see the Rockwell R6500 Hardware Manual, sections 1 and 2.

Three signals which appear on the expansion bus are not generated by the 6502 microprocessor and are not described in the Hardware Manual. These signals are the CS8, CS9, and CSA signals, which are chip-select signals generated by the address decode logic. These signals are driven low when memory addresses in the ranges 8000 to 8FFF, 9000 to 9FFF, and A000 to AFFF, respectively, are accessed by the 6502 processor. These signals are provided so that memory expansion modules can be implemented without requiring additional address decode logic.

Connector Pin	Pin Signal	Connector Pin	Pin Signal
1	SYNC	A	A0
2	RDY	B	A1
3	ø1	C	A2
4	IRQ	D	A3
5	S. O.	E	A4
6	NMI	F	A5
7	RES	H	A6
8	D7	J	A7
9	D6	K	A8
10	D5	L	A9
11	D4	M	A10
12	D3	N	A11
13	D2	P	A12
14	D1	R	A13
15	D0	S	A14
16	-12V	T	A15
17	+12V	U	SYS ø2
18	CS8	V	SYS R/W
19	CS9	W	R/W
20	CSA	X	no connect
21	+5VDC	Y	ø2
22	GND	Z	RAM R/W

Figure 1-8. Expansion Bus Connector J3.

USING AVAILABLE SOFTWARE WITH THE 6500 CPU BOARD

A variety of software for the 6500 CPU Board is available in ROM format, including a program monitor, with text editor, 6502 Assembler, and a number of languages, including BASIC, FORTH, PL/65, and PASCAL. Four of these available programs are briefly described below.

AIM-65 Monitor

The AIM-65 Monitor provides powerful software features and linkages, many of which are also available to user programs. Some of the principal features of this Monitor are summarized below:

- Peripheral driver routines handle the use of the keyboard, display and printer, and provide user programs with easy access to these peripherals.

- Entry and re-entry capabilities provide access to programs such as the Editor, Assembler, BASIC, and/or other user-programmed functions. Control may be returned to the Monitor by the programmed function or by pressing the RESET button on the CPU Board.

- Debugging capabilities including:

  - Display-and-alter commands allow access to any memory location or processor register.

  - Instruction-Entry-and-Disassembly allows mnemonic entry of instructions directly into memory and mnemonic disassembly of machine codes in memory.

The AIM-65 Monitor is described in detail in Section 3 of the Rockwell AIM-65 User's Manual, available from Cubit or from Rockwell. A companion manual is the AIM-65 Monitor Program Listing, available from the same sources. Users of the AIM-65 Monitor ROMs should consult these

manuals to obtain a complete explanation of the monitor commands and functions.

The Rockwell AIM-65 Monitor program is packaged on two R2332 4K ROMs, which are available from Cubit. If the 6500 CPU Board was not ordered from the manufacturer with these ROMs installed in sockets Z22 and Z23, complete instructions on how to install these ROMS may be found in the section "ROM Memory Installation" earlier in this chapter.

AIM-65 Text Editor

The AIM-65 Text Editor is a program included in the two 2332 ROMs containing the AIM-65 Monitor. The Text Editor allows the creation and editing of files of text, which may consist of source programs, data files or text characters. Many commands are available to insert, delete, search, and change strings of characters in the text file being edited. The commands and capabilities of the Text Editor are described in Section 4 of the Rockwell AIM-65 User's Guide, referred to earlier.

AIM-65 Assembler

The AIM-65 Assembler translates assembly-language source programs into machine instruction codes. The Assembler is a two-pass symbolic assembler, allowing both data and instruction addresses to be specified symbolically rather than as absolute addresses. The program does extensive error-checking and signals errors as they are found. A full assembly-listing may be generated, or if desired, an errors-only listing may be specified. Source programs for input to the Assembler may be created using the AIM-65 Text Editor.

The features and capabilities of the AIM-65 Assembler are described in Section 5 of the Rockwell AIM-65 User's Guide.

The AIM-65 Assembler is supplied on a single 4K R2332 ROM that plugs into socket Z24 on the 6500 CPU Board. Complete instructions on how to install ROMs on the CPU Board are found in the section "ROM Memory Installation" above.

AIM-65 BASIC

The Rockwell AIM-65 BASIC by Microsoft is an 8K interpreter which can be used to create and execute programs on the 6502 microprocessor. This interpreter uses the BASIC programming language, one of the most widely known programming languages.

The many features of this programming language are described in detail in the Rockwell Aim-65 BASIC Language Reference Manual, available from Rockwell.

The Rockwell BASIC program is contained on two 2332 ROMs, which must be installed on the CPU Board. To install these ROMs, consult the discussion on installation earlier in this chapter. ROM number R3225 is inserted in socket Z25 and ROM number R3226 is inserted into socket Z26 of the CPU Board.

TROUBLESHOOTING

When properly handled, the 6500 CPU Board will provide a long life of trouble-free operation. Like any piece of electronic equipment, however, there are several easy guidelines that should be followed to prevent damage.

General Hints on Handling

NEVER insert or remove boards from a system while power is being applied to the board. Delicate circuitry on the boards may be damaged by shorting contacts or exposing the circuits to excessive voltages. Always turn the power off before inserting or removing boards from a system.

Static electricity can easily damage integrated circuits and circuit boards. Always use care to prevent electrostatic discharge when inserting or removing chips from the board, and when handling the board itself.

Isolating Problems

In the event of problems in the operation of your 6500 CPU Board, it is important to localize the problem to a particular component of the system. If there are multiple boards in the system, try removing all the boards except the CPU Board to see if the CPU still functions.

The CPU Board may be exercised by itself with only a monitor ROM, keyboard and display. If the CPU Board does not operate in this standalone state, then the problem is likely to be found on the CPU Board. Usually, however, the problem can be traced to some component of the system other than the CPU Board. To isolate a problem with another board, try placing boards back in the system one at a time to discover which one stops the system from functioning.

In the ensuing discussion, we will assume that a problem has been discovered on the CPU Board. A typical problem condition occurs when the system simply does not appear to function. Symptoms of

this condition include the 6520 Display, if used, showing the message 'MODEL 6520 SELF TEST' (i.e., the display has not received any characters from the inoperative CPU Board). Another symptom may be no response to keyboard input. There are many conditions that may cause this problem, although several simple tests may be run to localize and possibly diagnose the source of the problem.

Each of the following tests may be done in sequence, to help identify the cause of a non-functioning CPU Board. If the board fails one of the tests in the sequence, then the source of the problem will have been identified. It is assumed that all other boards have been removed from the system; that is, the CPU Board is being tested in the standalone state.

1. The first item to check when diagnosing an inoperable board is to visually inspect the board for obvious shorts, or debris across the signal traces. Verify that each integrated circuit chip is firmly inserted into its socket, and that no pins on any of the chips have been bent or broken.

2. Next, verify that the power connections to the board are secure. With a voltmeter, verify that +5 volts D.C. is present between the +5V and GND traces on the CPU Board itself.

3. If the correct voltage is present on the CPU Board, check the flat cables between the CPU Board and any peripherals such as the keyboard and display. Faulty interface connections to these peripherals may make the CPU Board appear to be inoperative.

4. If the flat cables are making proper connections, then the next signal to check is the system clock. If the CPU clock signal is not present or is not of the correct frequency, then the board cannot operate. The CPU clock may be found at pin #37 on the 6502 CPU (Z9). Using an oscilloscope or logic analyzer, verify that this signal is a square-wave with a frequency of 1 MegaHertz. Also verify that a similar signal, the system clock, appears on pin #U of the J3 Expansion Connector.

5. If this clock signal is present, the next signal to test is the RESET signal. This signal appears on pin #40 of the 6502 CPU (Z9) and also at pin #7 of the J3 Expansion Connector. This signal should be in a TTL high state (+2.4V or greater). Depress the RESET switch (S1) on the 6500 CPU Board to verify that the RESET signal falls below +0.4V, and returns high when the switch is released.

6. If resetting the system does not solve the problem, then verify that the CPU is fetching and executing instructions. The SYNC signal (pin #7 of the CPU or pin #1 of the J3 Expansion Connector) goes momentarily high when the CPU fetches an instruction operation code from memory. When the CPU is functioning normally, this SYNC signal high state should appear every few clock cycles. In a malfunctioning system, where the microprocessor is not reading valid op codes from memory, or perhaps one of the address- or data-bus driver circuits has been damaged, the system 'hangs up' and this signal may not appear. In either case, this SYNC signal should always appear at least once immediately after activating the RESET switch.

7. If the microprocessor executes several fetches after a RESET, but then unaccountably 'hangs up', the problem may be related to software rather than the CPU Board hardware. Verify again that all the ROMs are correctly and fully inserted into their sockets, and that each ROM has been inserted into the correct socket. Other possible causes for this operation are that a 'dead' circuit somewhere on the board is tying up one of the data, address, or control lines.

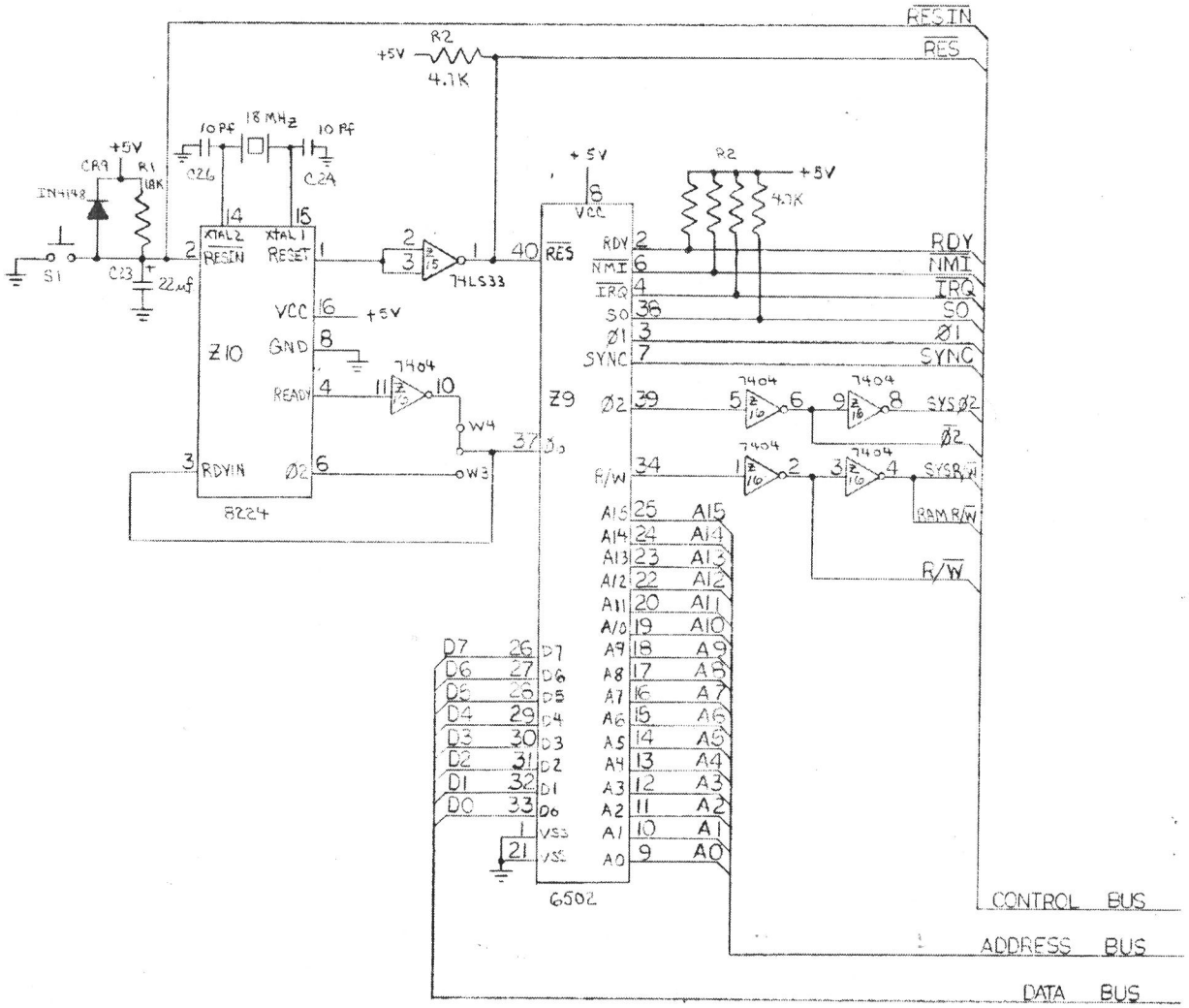
If a problem has been traced to the CPU board and this simple examination fails to identify the source of the problem, then you should return the CPU Board to Cubit for service. Additional tests that may be helpful in isolating the problem generally require specialized test equipment and are not described in this manual.

Memory Address	Device Description	Device Number
0000 -03FF	Random Access Memory (Read-Write)	Z2 (2114) Z3 (2114)
0400 -07FF	Random Access Memory (Read-Write)	Z6 (2114) Z7 (2114)
0800 -0BFF	Random Access Memory (Read-Write)	Z11 (2114) Z12 (2114)
0C00 -0FFF	Random Access Memory (Read-Write)	Z17 (2114) Z18 (2114)
1000 -9FFF	Available for system expansion using the J3 Expansion Connector.	- none -
A000 -A00F	Input/Output Device A Registers (see Fig. 1-4, I/O Register Memory Map, for a detailed description of the registers associated with each of these memory addresses).	Z1 (6522)
A010 -A3FF	- Not Available -	- none -
A400 -A47F	Random Access Memory (Read-Write)	Z33 (6532)
A480 -A49F	I/O Device C Data & Control Registers (see Fig. 1-4, I/O Register Memory Map, for a detailed description of the registers associated with each of these memory addresses).	Z33 (6532)
A4A0 -A7FF	- Not Available -	- none -
A800 -A80F	I/O Device B Data & Control Registers (see Fig. 1-4, I/O Register Memory Map, for a detailed description of the registers associated with each of these memory addresses).	Z32 (6522)
A810 -ABFF	- Not Available -	- none -

Figure 1-9. 6500 CPU Board Memory Map

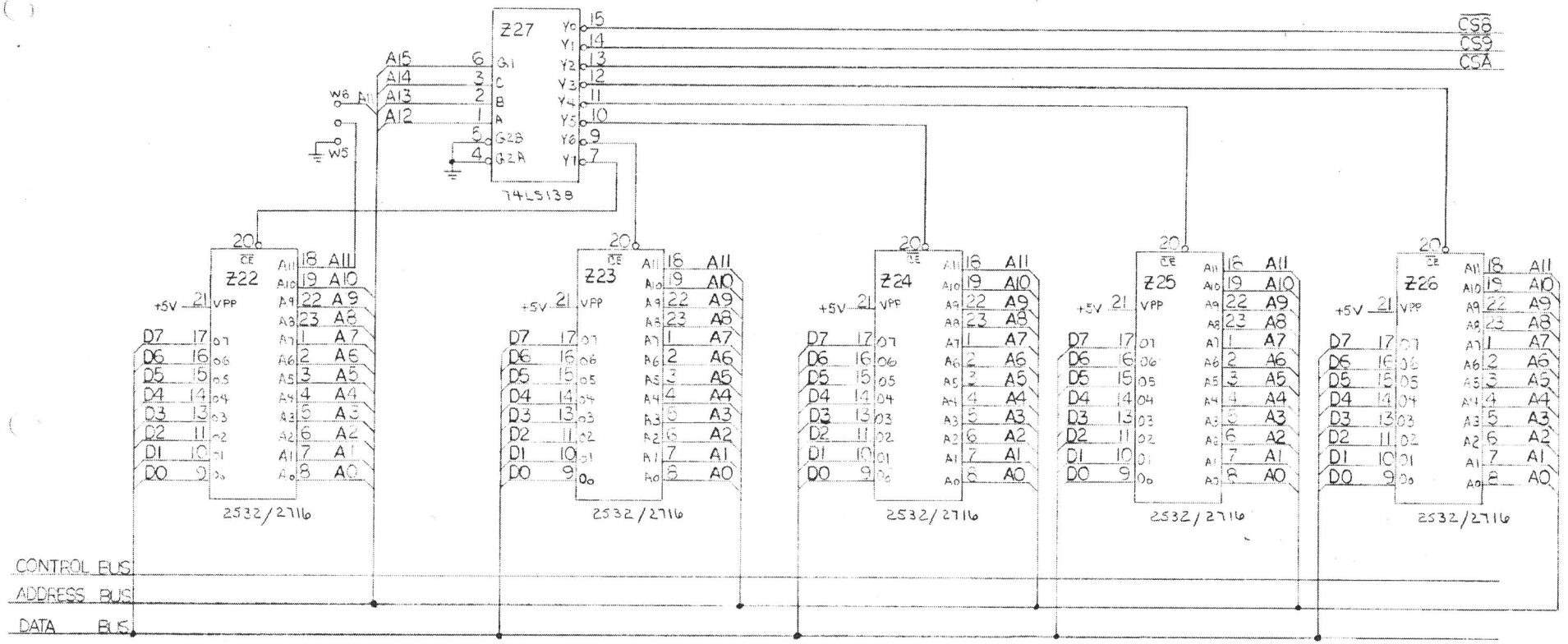
Memory Address	Device Description	Device Number
AC00 -AC03	I/O Device D Data & Control Registers (see Fig. 1-4, I/O Register Memory Map, for a detailed description of the registers associated with each of these memory addresses).	U1 (6520)
AC04 -AFFF	- Not Available -	- none -
B000 -BFFF	Program Memory (Read-Only)	Z26 (2716, 2532,2332)
C000 -CFFF	Program Memory (Read-Only)	Z25 (2716, 2532,2332)
D000 -DFFF	Program Memory (Read-Only)	Z24 (2716, 2532,2332)
E000 -EFFF	Program Memory (Read-Only)	Z23 (2716, 2532,2332)
F000 -FFF9	Program Memory (Read-Only)	Z22 (2532, 2332)
FFFA -FFFB	Non-Maskable Interrupt Vector	Z22 (2532, 2332)
FFFC -FFFD	Power-On Reset Vector Address	Z22 (2532, 2332)
FFFE -FFFF	Interrupt Request Vector Address	Z22 (2532, 2332)

Figure 1-9. 6500 CPU Board Memory Map (cont'd)



CUBIT INC.

TITLE: COMPUTER	
MODEL 6500	DATE 6-3-83
REV. B	SHT. 1 OF 4



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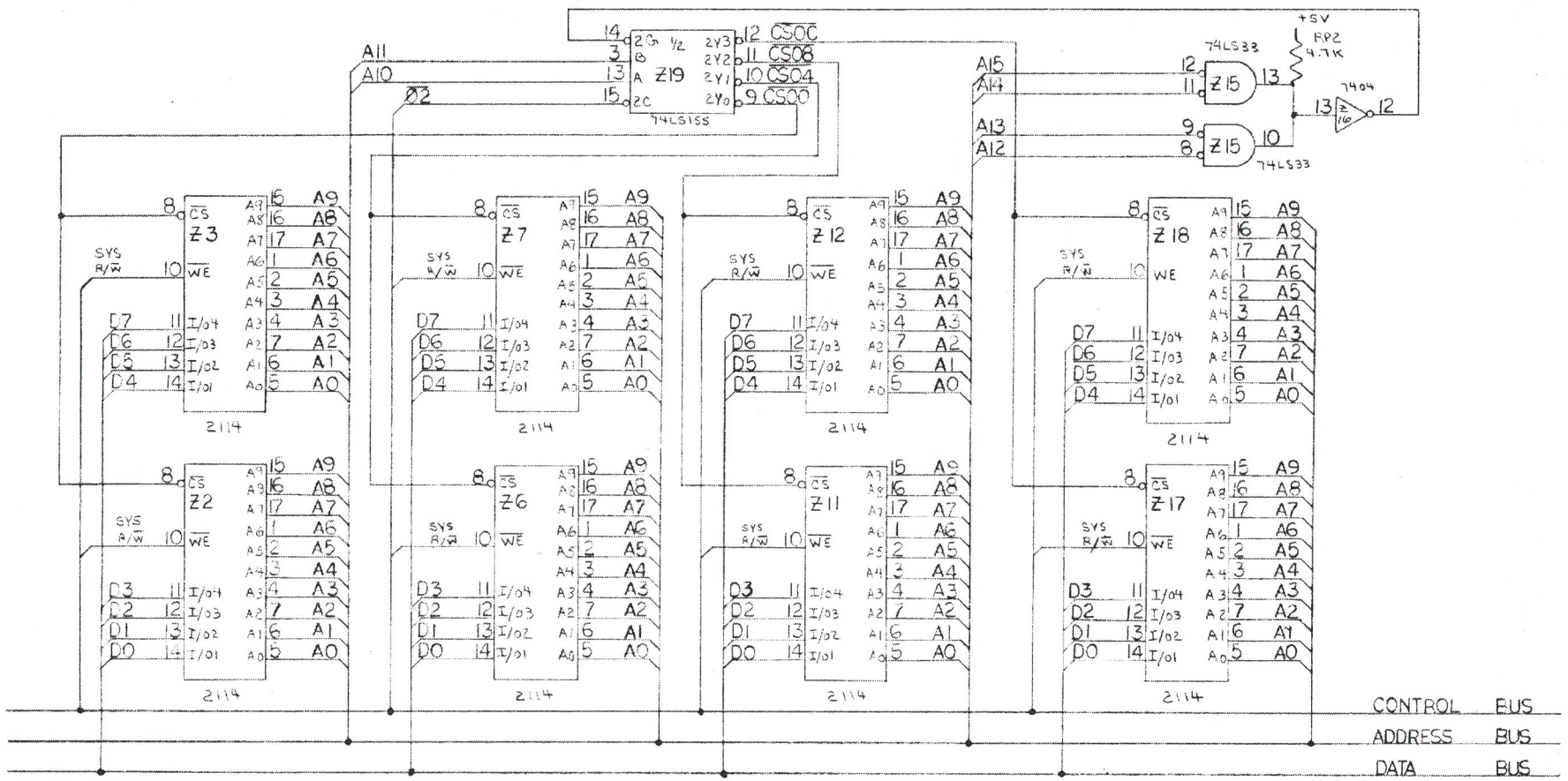
TITLE: COMPUTER	
MODEL 6500	DATE 6-3-83
REV. B	SHT. 2 OF 4

$\overline{RAM\ CE} = R/\overline{W} * PHI2$

$\overline{RAM\ WR} = \overline{R/W} * PHI2$

$\overline{ROM\ CE} = R/\overline{W} * PHI2$



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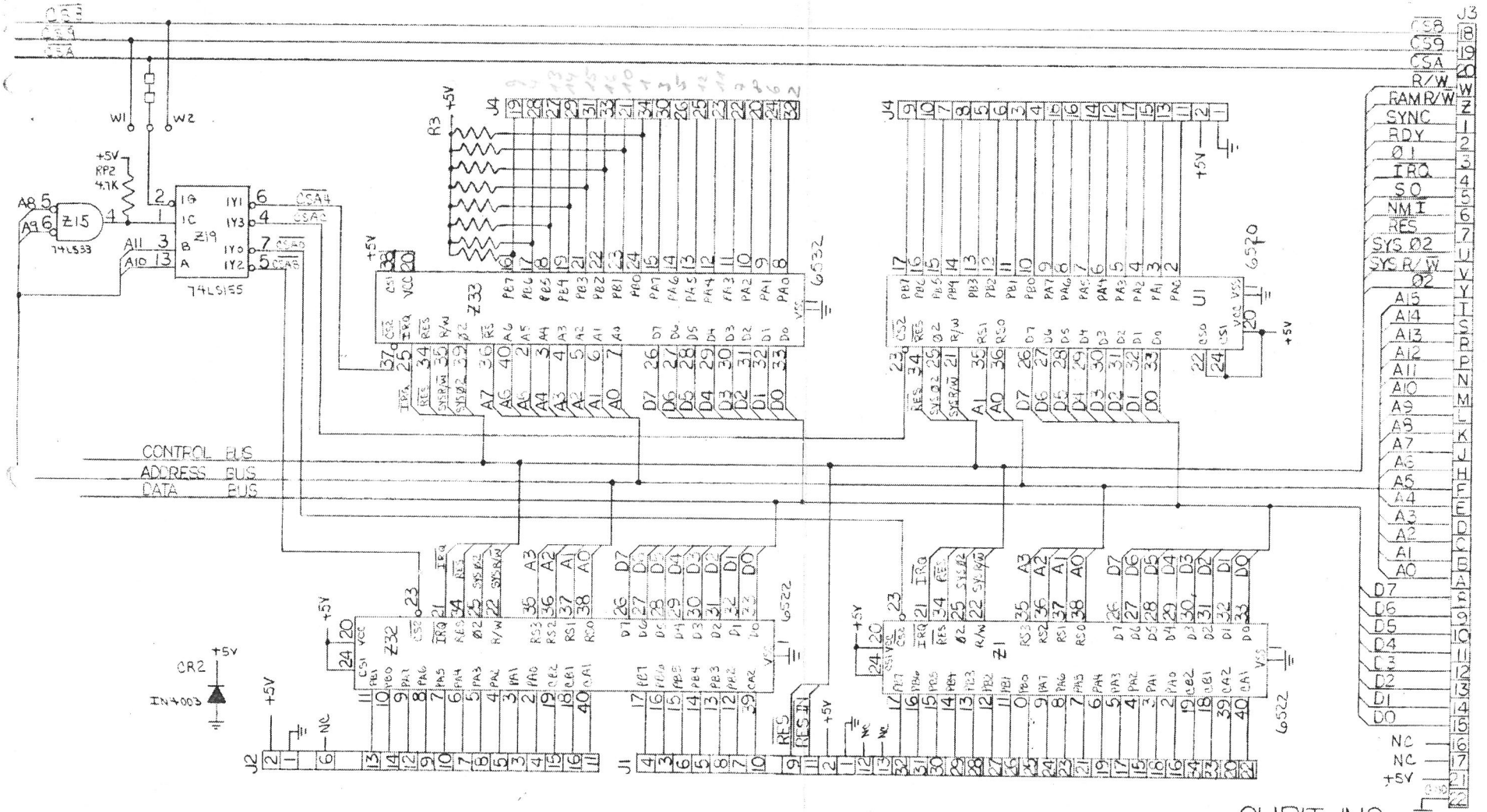
TITLE : COMPUTER	
MODEL 6500	DATE 6 -3 -83
REV. B	SHT. 3 OF 4



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