RM 65 FAMILY

16K PROM/ROM Module
USER'S MANUAL

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Rockwell International

Document No. 29801 N06
Order No. 806
Rev. 1 October 1982

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SECTION 1

INTRODUCTION

1.1 PURPOSE/FUNCTION

The RM 65 16K PROM/ROM Module provides the user with a means of increasing system PROM or ROM capacity by up to 16K bytes, in increments of 2K, 4K, or 8K. On-board jumpers allow the module to operate using different types of 2K, 4K, or 8K PROM or ROM devices. The 16K PROM/ROM module is designed to interface with a Rockwell RM 65 bus.

The 16K PROM/ROM module is available in a 72-pin Edge Connector version (RM65-3216) and a 64-pin Eurocard version (RM65-3216E). Both versions are shown in Figure 1-1. The pin assignments for the two versions are identical except the Edge Connector version has four additional pins connected to +5 Vdc and four unused pins (See Table 3-1 for the pin assignments).

1.2 FEATURES

- o Rockwell RM 65 Bus compatible.
- o Allows system PROM or ROM expansion up to 16K bytes in 2K, 4K, or 8K increments.
- o Maximum (16K) PROM expansion possible by installation of the following PROM/ROM devices or equivalent:
  - -- Eight 2516 or 2716 (INTEL or equivalent) 2K PROMS, or
  - -- Four 2532 or 2732 4K PROMS, or
  - -- Eight Rockwell 2316 ROMS, or
  - -- Four Rockwell 2332 ROMS, or
  - -- Two Rockwell 2364 ROMS.
- o Fully buffered bus interface.
- o Four separately addressable 4K byte memory sections.
- o Sixteen Base Address Select switches to assign each 4K memory section to one of 16 software addressed base addresses in the selected 65K memory bank.
- o One Bank Select switch to assign the module to one of two 65K memory banks.

- One Bank Select Enable switch to disable bank select control to one-half of the 16K PROM or ROM. This feature allows 8K of the PROM or ROM to be common to two 65K memory banks while the other 8K of the PROM or ROM is dedicated to one of the two 65K memory banks.

- On-board jumpers for configuring the module to operate with the installed PROM/ROM devices.

- Reduced power consumption operation for those PROM/ROM chip devices incorporating the power-down feature.

- Edge connector and Eurocard versions.

- Fully assembled, tested and warranted.

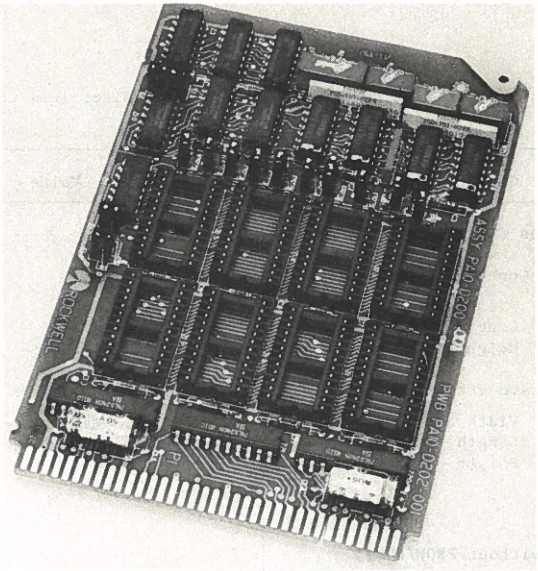
1.3 CHARACTERISTICS

The physical and electrical characteristics of the PROM/ROM module are listed in Table 1-1.

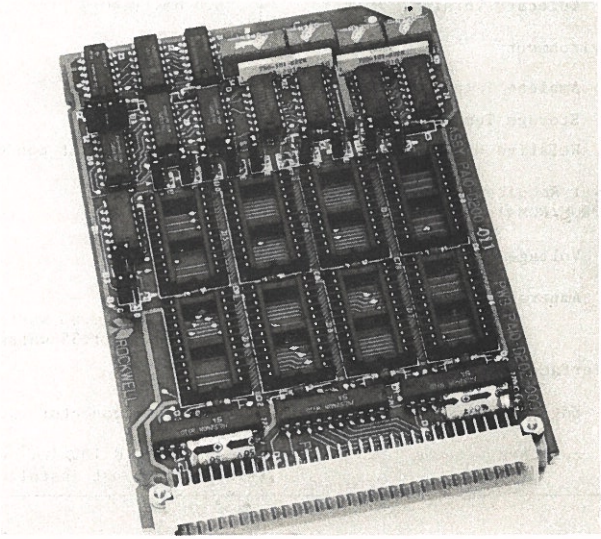
1.4 REFERENCE DOCUMENTS

Rockwell

Document No.	
29650N30	R6500 Programming Manual
29650N31	R6500 Hardware Manual
29650N36	AIM 65 Microcomputer User's Manual



a. Edge Connector Version



b. Eurocard Version

Figure 1-1. 16K PROM/ROM Module

Table 1-1. 16K PROM/ROM Module Physical and Electrical Characteristics

Characteristic	Value
Dimensions (See Figure 1-2)	
Edge Connector Version	
Width	3.9 in. (100 mm)
Length	6.5 in. (164 mm)
Height	0.56 in. (14 mm)
Eurocard Version	
Width	3.9 in. (100 mm)
Length	6.3 in. (160 mm)
Height	0.56 in. (14 mm)
Weight (without PROM/ROMs)	
Edge Connector	4.6 oz. (130g)
Eurocard Version	5.0 oz. (140g)
Environment	
Ambient Temperature	0°C to 70°C
Storage Temperature	-40°C to 85°C
Relative Humidity	0% to 85% (without condensation)
Power Requirements (without PROM/ROMs)	
Voltage	+5 Vdc $\pm$ 5%
Amperage and Power	0.17 amperes (0.85 watts) - typical 0.27 amperes (1.35 watts) - maximum
Interface Connector P1	
Edge Connector Version	72-pin edge connector (0.100 in. centers)
Eurocard Version	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)

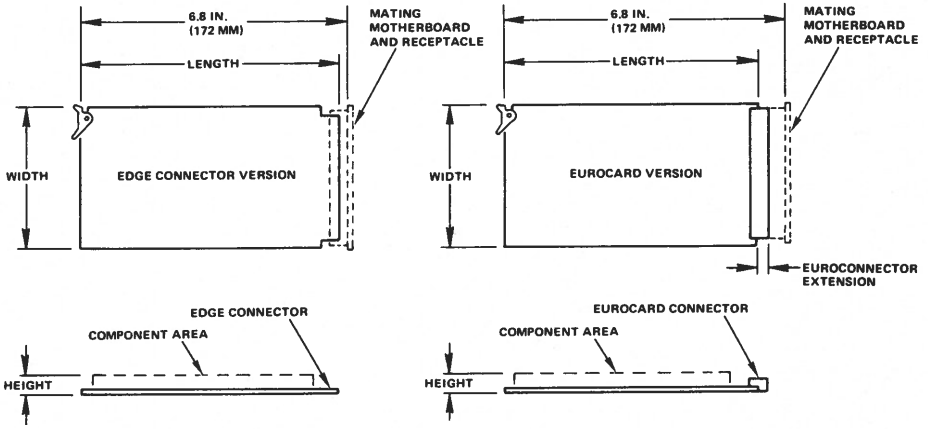


Figure 1-2. 16K PROM/ROM Module Outline

SECTION 2

INSTALLATION AND OPERATION

2.1 UNPACKING

Unpack the PROM/ROM module from its shipping carton and refer to the packing sheet to verify that all of the parts are included. Save the packing material for storing the module.

2.2 OPERATING OPTIONS

Four operating options are switch or jumper selectable:

- Base Address Selection
- Bank Selection
- Common versus Dedicated Memory Banks
- PROM/ROM Selection

Figure 2-1 identifies the switches, jumpers and sockets on the PROM/ROM module. The function of each switch and jumper is identified in Table 2-1 along with reference to the section and table that describes its use.

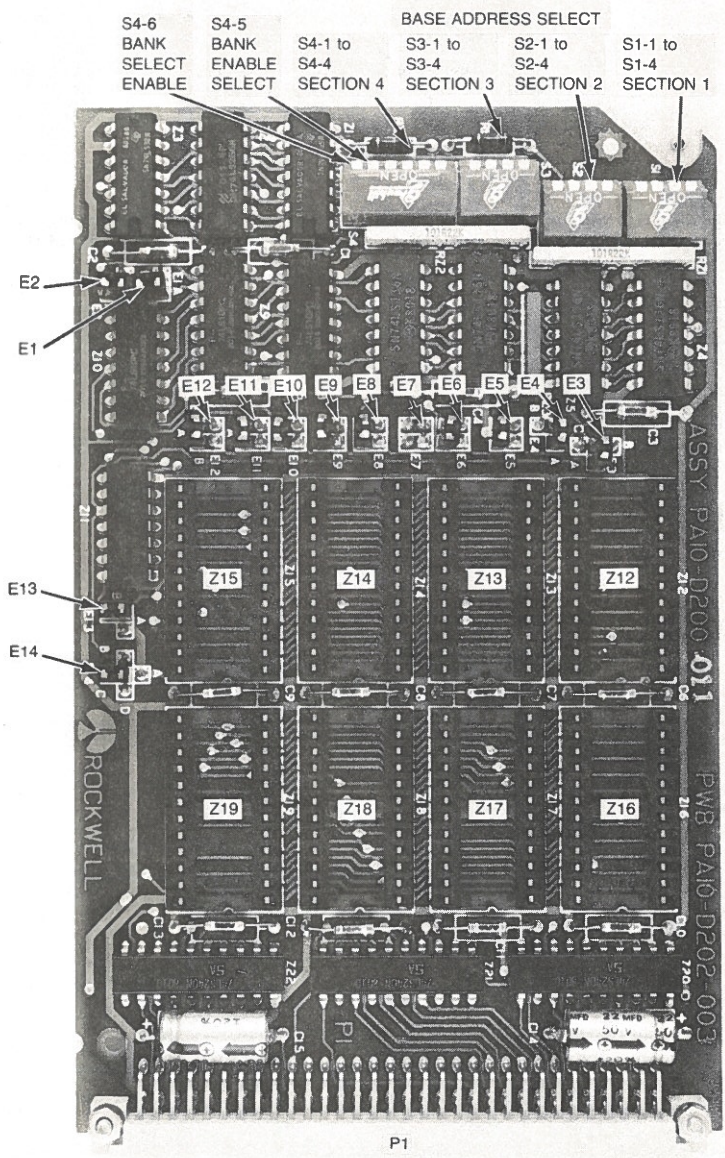


Figure 2-1. 16K PROM/ROM Module Detail

Table 2-1. 16K PROM/ROM Module Switches, Jumpers, and Sockets

Type	Item	Function	Reference
Switches	S1-1 through S1-4	Base Address Select for 4K Section 1	Section 2.2.1 Table 2-2
	S2-1 through S2-4	Base Address Select for 4K Section 2	
	S3-1 through S3-4	Base Address Select for 4K Section 3	
	S4-1 through S4-4	Base Address Select for 4K Section 4	
	S4-5	Bank Select	Section 2.2.2 Table 2-3
	S4-6	Bank Select Enable	
Jumpers	E1-E14	PROM/ROM Select	Section 2.3.2 Table 2-4
Sockets	Z12-Z19	PROM/ROM Sockets	Section 2.3.1 Figure 2-2

2.2.1 Base Address Selection

The PROM/ROM module is segmented into four independent 4096 byte sections, Section 1 through Section 4. Each 4K section must be assigned a unique base address within the system memory map. The positions of switches S1-1 through S1-4, S2-1 through S2-4, S3-1 through S3-4 and S4-1 through S4-4 select the base (starting) address for Sections 1, 2, 3 and 4, respectively. The switch positions are described in Table 2-2.

NOTES

1. If bank addressing is used (see Section 2.2.2) in the system, the base address will be the same for each bank.

2. When a 4K section of the module is not used (i.e. PROMS/ROMS are not installed) set the Base Address Select switches for the unused section to the same configuration as the Base Address Select switches for a used section of the module.

3. Ensure that the selected base address for a populated 4K PROM/ROM Section is not the same as the base address for another populated 4K PROM/ROM section on this module.

4. Ensure that the address range established in the selected base address and the device size (number of bytes) does not overlap any addresses assigned to devices or I/O on other modules.

5. In cases where 8K PROM or ROM devices are used assign a base address of 2000, 4000, 6000, 8000, A000, C000, or E000 to one 4K half of the device and a base address of 3000, 5000, 7000, 9000, B000, D000, or F000 to the other 4K half of the device.

Table 2-2. Base Address Select Switch Positions

4K Base Address (Hexadecimal)	Switch S4-S1 Positions			
	SX-4	SX-3	SX-2	SX-1
0000	OPEN	OPEN	OPEN	OPEN
1000	OPEN	OPEN	OPEN	CLOSED
2000	OPEN	OPEN	CLOSED	OPEN
3000	OPEN	OPEN	CLOSED	CLOSED
4000	OPEN	CLOSED	OPEN	OPEN
5000	OPEN	CLOSED	OPEN	CLOSED
6000	OPEN	CLOSED	CLOSED	OPEN
7000	OPEN	CLOSED	CLOSED	CLOSED
8000	CLOSED	OPEN	OPEN	OPEN
9000	CLOSED	OPEN	OPEN	CLOSED
A000	CLOSED	OPEN	CLOSED	OPEN
B000	CLOSED	OPEN	CLOSED	CLOSED
C000	CLOSED	CLOSED	OPEN	OPEN
D000	CLOSED	CLOSED	OPEN	CLOSED
E000	CLOSED	CLOSED	CLOSED	OPEN
F000	CLOSED	CLOSED	CLOSED	CLOSED

NOTE

SX corresponds to PROM/ROM sections:

X	PROM/ROM Section
1	1
2	2
3	3
4	4

2.2.2 Bank Selection

The Bank Select Enable switch (S4-6), in conjunction with the Bank Select switch (S4-5), allows 8K bytes of the PROM/ROM module (Section 1 & 2) to be assigned common to both 65K byte memory banks (Bank 0 and Bank 1) or to be dedicated to a selected memory bank (Bank 0 or Bank 1). The other 8K bytes (Sections 3 & 4) are always assigned dedicated to either Bank 0 or Bank 1 as determined by the Bank Select switch.

When OPEN, the Bank Select Enable switch assigns Sections 1 & 2 common to both banks regardless of the position of the Bank Select switch. When the Bank Select Enable switch is CLOSED, the assigned bank for Sections 1 & 2 is dedicated as determined by the position of the Bank Select switch. Sections 3 & 4 are always assigned to a dedicated bank regardless of the Bank Select Enable switch. See Table 2-3 for the switch positions.

In installations where the PROM/ROM module is addressed by a microcomputer that has bank addressing, i.e. BADR/ is driven as the 17th address line, the Bank Select switch may be positioned to select either Bank 0 or Bank 1. In installations where the PROM/ROM module is to be addressed by a microcomputer that does not have bank addressing; i.e. BADR/ is continually high, the Bank Select switch must be positioned to select Bank 0.

Table 2-3. Bank Select Switch Positions

Memory Bank Selected		Switch Position	
Sections 1 & 2 (Sockets Z12, Z13, Z16 & Z17)	Sections 3 & 4 (Sockets Z14, Z15, Z18 & Z19)	Bank Select Enable Switch S4-6	Bank Select Switch S4-5
BANK 0 & 1 (COMMON)	BANK 0 (LOWER 65K)	OPEN	OPEN
BANK 0 & 1 (COMMON)	BANK 1 (UPPER 65K)	OPEN	CLOSED
BANK 0 (LOWER 65K)	BANK 0	CLOSED	OPEN
BANK 1 (UPPER 65K)	BANK 1	CLOSED	CLOSED

2.3 PROM/ROM INSTALLATION AND SELECTION

2.3.1 PROM/ROM Device Installation

The following PROM/ROM devices or identically compatible devices may be installed:

Type	Manufacturer	Model	Size (Bytes)
PROM	TI	TMS2516	2K
PROM	Intel	I2716	2K
ROM	Rockwell	R2316	2K
PROM	TI	TMS2532	4K
PROM	Intel	I2732	4K
ROM	Rockwell	R2332	4K
ROM	Rockwell	R2364	8K

The PROM/ROM devices may be installed in any of the sockets shown in Figure 2-2 in accordance with the desired memory map.

NOTES

1. Mixing of different PROM and ROM sizes is prohibited; however, identically compatible devices of the same size may be substituted.

2. Module addressing prohibits installation of 8K devices in sockets Z13 and Z15. Sockets Z12 and Z14 must be used for 8K devices.

3. When jumpers are positioned for 4K or 8K device operation, devices installed in sockets Z16 - Z19 are not addressed and do not affect system operation.

2.3.2 PROM/ROM Jumper Installation

Jumpers E1 through E4, E13 and E14 must be installed in accordance with the installed PROM/ROM devices as shown in Table 2-4. The individual sockets have double jumpers, E5 through E12, that must be installed as shown for all populated sockets.

2.4 INSTALLING THE MODULE

Before installing the module, ensure that it is not damaged and is free of grease, dirt, liquid or other foreign matter.

CAUTION

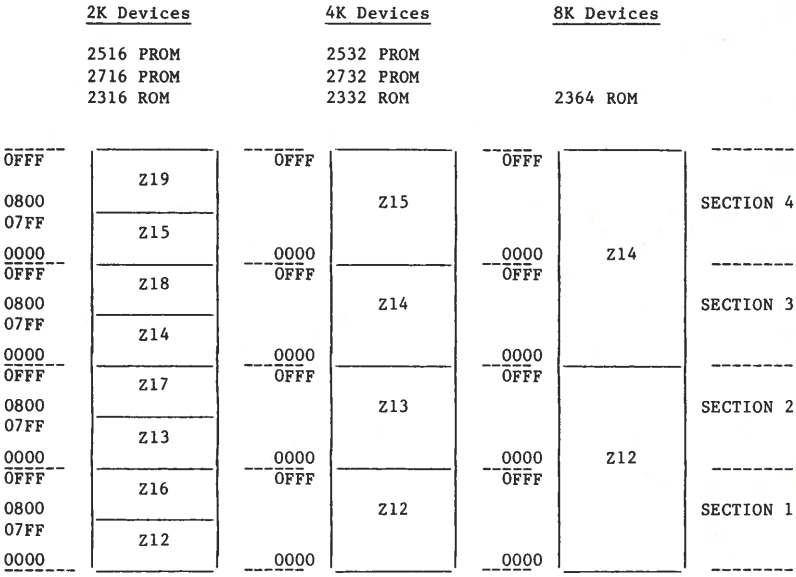
Prior to module installation turn off power to the RM 65 bus.

Also, turn off power to the RM 65 bus when the PROM/ROM module is installed prior to changing switch or jumper positions.

a. Based on the system memory map, select the proper module operation options as follows:

   1. Install PROM/ROM devices into sockets Z12-Z19 (refer to Figure 2-2).

   2. Configure the module jumpers to correspond to the installed PROMs/ROMs (refer to Table 2-4).



NOTES

1. The addresses shown are added to the selected base address for the given section.

2. If an 8K ROM is installed, the base address for both 4K sections must be contiguous.

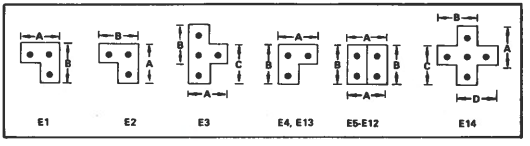
Figure 2-2. PROM/ROM Module Socket Memory Map

Table 2-4. Jumpering Configuration for PROM or ROM Devices

Jumper	Socket	Jumper Positions						
		PROM				ROM		
		2516 (2K)	2716 (2K)	2532 (4K)	2732 (4K)	2316 (2K)	2332 (4K)	2364 (8K)
E1		A	A	A	A	A	A	B
E2		A	A	A	A	A	A	B
E3		A	C	B	C	A	B	B
E4		B	B	A	A	B	A	A
E5	Z16	BB	AA	-	-	BB	-	-
E6	Z12	BB	AA	BB	AA	BB	BB	BB
E7	Z17	BB	AA	-	-	BB	-	-
E8	Z13	BB	AA	BB	AA	BB	BB	-
E9	Z18	BB	AA	-	-	BB	-	-
E10	Z14	BB	AA	BB	AA	BB	BB	BB
E11	Z19	BB	AA	-	-	BB	-	-
E12	Z15	BB	AA	BB	AA	BB	BB	-
E13		B	A	A	A	B	B	B
E14		A	A	A	C	B	A	D

NOTES

1. Jumper positions (A,B,C,D) are marked on component side of module's printed circuit board. A "-" (dash) for a jumper is a don't care and has no affect. Jumpers E5 through E12 are double jumpers and are shown with positon AA or BB.
2. Jumper locations are shown in Figure 2-1.
3. The jumper position shown in this table correspond to the PROM/ROM pin assignments listed in Appendix A.
4. Jumper positions shown with switches on the left:



3. Select module base addresses by positioning switches S1-S4 (refer to Table 2-2).

4. Select module bank address by positioning switch S4-5 (refer to Table 2-3).

5. Select common memory bank or dedicated memory bank operation for Sections 1 & 2 by positioning switch S4-6 (refer to Table 2-3).

b. Align pin Wa (for Edge Connector version) or pin 1a (for Eurocard version) of the module with the identical pin on the mating RM 65 bus receptacle.

> CAUTION
>
> RM 65 Bus connectors are keyed to prevent improper module connection. If the module does not insert into the receptacle with moderate pressure applied, check the orientation and the connector alignment of the module. Forcing the module improperly into the receptacle will damage the receptacle and/or the module.

c. Insert the PROM/ROM module into the desired card slot (if a card cage is used) and position it in front of the mating receptacle.

d. Press in firmly on the end of module until all pins are securely seated.

e. Reapply power to the RM 65 bus.

2.5 REMOVING THE MODULE

a. Turn-off power to the RM 65 bus.

b. If the module is installed in a card cage, lift up on the module ejector tab to release the module from the mating receptacle. Pull the module straight back until it is free from the module guides.

c. If the module is installed in a single card adapter, or in a motherboard without a card cage pull back on the module while moving it slightly from side to side until it is free from the mating receptacle.

SECTION 3

FUNCTIONAL AND INTERFACE DESCRIPTION

3.1 FUNCTIONAL DESCRIPTION

The PROM/ROM module has eight 24-pin sockets which can accept up to 16K of either 2K, 4K, or 8K PROM or ROM.

The Data Buffers invert and transfer 8 bits of parallel data (BD0/ - BD7/) from the selected PROM/ROM device to the RM 65 Bus during read of the PROM/ROM module. The Data Buffer Control uses the Read/Write (BR/$\bar{W}$), Clock (BØ2), and Chip Select circuitry to enable the Data Buffers whenever PROM/ROM is addressed. The Bus Active signal is generated to indicate that the Data Buffers are active.

The Address Buffers invert and transfer 16 parallel address lines (BA0/ - BA15/) from the RM 65 Bus to the Base Address Decoders, to the Chip Select Decode Jumpers and to the PROM/ROM devices.

The Control Buffers transfer control signals BØ2 and BR/$\bar{W}$ from the RM 65 bus to the Data Buffer Control and the PROM/ROM Type Jumper area. The Bus Active (BACT/) is buffered and transferred to the RM 65 Bus.

The Bank Select Control circuit detects when the PROM/ROM module's assigned memory bank is addressed by comparing the bank address signal (BADR/) from the RM 65 Bus to the Bank Select switch. The Bank Select Enable switch allows 8K of the PROM/ROM to be common memory (addressable in both Bank 0 and Bank 1) or dedicated to Bank 0 or Bank 1 while the remaining 8K is assigned to Bank 0 or Bank 1 as determined by the Bank Select switch.

Four Base Address Decoders allow 4K PROM/ROM sections to be independently addressed on any 4K boundary within the selected bank. When an address is within range of any section, as selected by the Base Address switches, an enable signal is sent to the Chip Select Decoder.

The Chip Select Decoder uses the Base Address Decoder output signals, the address lines, and the PROM/ROM size jumpers to generate chip selects for the PROM/ROM devices. The PROM/ROM type jumpers route the chip select lines to the correct pins on the PROM/ROM sockets.

3.2 INTERFACE DESCRIPTION

Table 3-1 identifies the pin assignments for connector P1. Table 3-2 defines the interface signals.

> **NOTE**
>
> "/" suffix denotes signal active at negative or low voltage level.

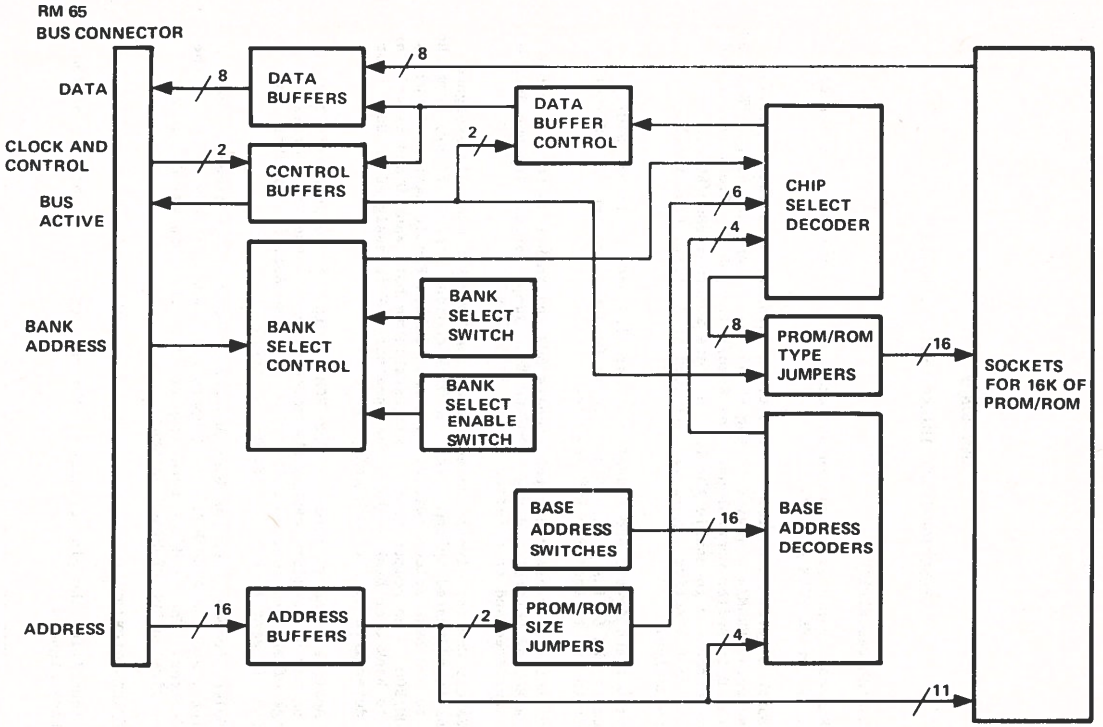


Figure 3-1. 16K PROM/ROM Module Block Diagram

Table 3-1. Connector P1 (RM 65 Bus) Pin Assignments

Pin	Signal Mnemonic	Signal Name	Input/Output
Wa		Not Connected (See Note)	
Wc		Not Connected (See Note)	
Xa	+5V	+5 Vdc (See Note)	
Xc	+5V	+5 Vdc (See Note)	
1a	GND	Ground	
1c	+5V	+5 Vdc	
2a	BADR/	Buffered Bank Address	I
2c	BA15/	Buffered Address Bit 15	I
3a	GND	Ground	
3c	BA14/	Buffered Address Bit 14	I
4a	BA13/	Buffered Address Bit 13	I
4c	BA12/	Buffered Address Bit 12	I
5a	BA11/	Buffered Address Bit 11	I
5c	GND	Ground	
6a	BA10/	Buffered Address Bit 10	I
6c	BA9/	Buffered Address Bit 9	I
7a	BA8/	Buffered Address Bit 8	I
7c	BA7/	Buffered Address Bit 7	I
8a	GND	Ground	
8c	BA6/	Buffered Address Bit 6	I
9a	BA5/	Buffered Address Bit 5	I
9c	BA4/	Buffered Address Bit 4	I
10a	BA3/	Buffered Address Bit 3	I
10c	GND	Ground	
11a	BA2/	Buffered Address Bit 2	I
11c	BA1/	Buffered Address Bit 1	I
12a	BA0/	Buffered Address Bit 0	I
12c		Not Used	
13a	GND	Ground	
13c		Not Used	

Table 3-1. Connector P1 (RM 65 Bus) Pin Assignments (Continued)

Pin	Signal Mnemonic	Signal Name	Input/Output
14a		Not Used	
14c		Not Used	
15a		Not Used	
15c	GND	Ground	
16a		Not used	
16c		Not Used	
17a		Not Used	
17c		Not Used	
18a	GND	Ground	
18c		Not Used	
19a		Not Used	
19c		Not Used	
20a		Not Used	
20c	GND	Ground	
21a		Not Used	
21c		Not Used	
22a		Not Used	
22c	BR/$\overline{W}$	Buffered Read/Write	I
23a	GND	Ground	
23c	BACT/	Buffered Bus Active	O
24a		Not Used	
24c		Not Used	
25a		Not Used	
25c	GND	Ground	
26a	BØ2	Buffered Phase 2 Clock	I
26c		Not Used	
27a	BD7/	Buffered Data Bit 7	O
27c	BD6/	Buffered Data Bit 6	O
28a	GND	Ground	
28c	BD5/	Buffered Data Bit 5	O

Table 3-1. Connector P1 (RM 65 Bus) Pin Assignments (Continued)

Pin	Signal Mnemonic	Signal Name	Input/Output
29a	BD4/	Buffered Data Bit 4	O
29c	BD3/	Buffered Data Bit 3	O
30a	BD2/	Buffered Data Bit 2	O
30c	GND	Ground	
31a	BD1/	Buffered Data Bit 1	O
31c	BD0/	Buffered Data Bit 0	O
32a	+5V	+5 Vdc	
32c	GND	Ground	
Ya	+5V	+5 Vdc (See Note)	
Yc	+5V	+5 Vdc (See Note)	
Za		Not Connected (See Note)	
Zc		Not Connected (See Note)	

NOTE

Pins Wa, Wc, Xa, Xc, Ya, Yc, Za and Zc are available on Edge Connector version only.

Table 3-2. Connector P1 (RM 65 Bus) Signal Descriptions

MNEMONIC P1	SIGNAL NAME AND SIGNAL DESCRIPTION	TYPE
	NOTE: All signals interfaced to and from the PROM/ROM module are driven at TTL voltage levels.	
+5V	+5 Vdc supplied to the PROM/ROM module via the RM 65 Bus.	
GND	Ground System ground.	
BA0/-BA15/	Buffered Address Bits 0-15 Sixteen address lines transfer an inverted 16-bit address from the RM 65 Bus to Address Buffers in the PROM/ROM module.	TS
BD0/-BD7/	Buffered Data Bits 0-7 Eight data lines transfer 8 bits of inverted data from the Data Buffers on the PROM/ROM module to the RM 65 Bus.	TS
BACT/	Buffered Bus Active A low BACT/ indicates that the PROM/ROM module has been addressed and the Data Buffers are enabled to transmit data onto the RM 65 Bus.	OC
BADR/	Buffered Bank Address A high BADR/ signal addresses the lower 65K (bank 0) memory bank; a low BADR/signal addresses the upper 65K (bank 1) memory bank.	TS
BR/$\overline{W}$	Buffered Read/Write A high BR/$\overline{W}$ signal provides one enable to the data buffers in the PROM/ROM module and also provides one enable to the PROM/ROM buffer that generates the BACT/ signal. Signal BR/$\overline{W}$ is high at all times except when the microcomputer is performing a write operation to another module.	TS

Table 3-2. Connector P1 (RM 65 Bus) Signal Descriptions

MNEMONIC P1	SIGNAL NAME AND SIGNAL DESCRIPTION	TYPE
BØ2	Buffered Phase 2 Clock PROM/ROM data enables and chip selects for all PROM or ROM devices are synchronized to the positive portion of the BØ2 clock. NOTE Driver Type: TS = Tri-State OC = Open Collector	TS

SECTION 4

PROGRAMMING CONSIDERATIONS

A system memory map should be constructed to include the address range for each of the four 4K sections of the PROM/ROM module that is to be used. The memory map must also reflect if the PROM or ROM installed in sockets Z12, Z13, Z16, and Z17 is to be dedicated to one memory bank or common to both 65K memory banks.

If bank addressing is used, BADR/ must be driven under software control. BADR/ must select the desired bank before that bank is addressed.

APPENDIX A

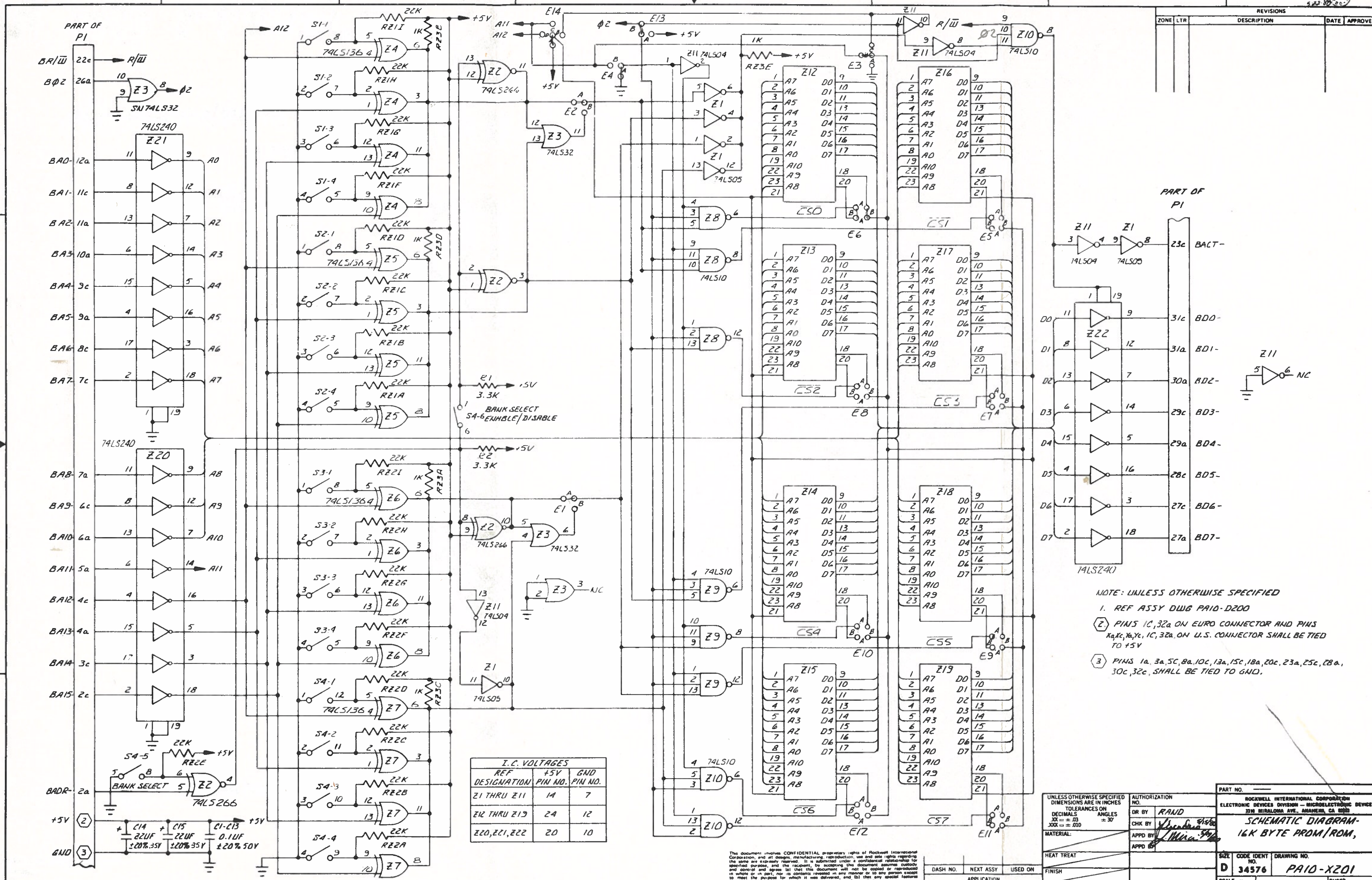
PROM/ROM PIN ASSIGNMENTS

Pin Number	PROM/ROM						
	2K			4K			8K
	2516 PROM	2716 PROM	2316 ROM	2532 PROM	2732 PROM	2332 ROM	2364 ROM
1	A7	A7	A7	A7	A7	A7	A7
2	A6	A6	A6	A6	A6	A6	A6
3	A5	A5	A5	A5	A5	A5	A5
4	A4	A4	A4	A4	A4	A4	A4
5	A3	A3	A3	A3	A3	A3	A3
6	A2	A2	A2	A2	A2	A2	A2
7	A1	A1	A1	A1	A1	A1	A1
8	A0	A0	A0	A0	A0	A0	A0
9	Q1	O0	Q0	Q1	O0	Q0	Q0
10	Q2	O1	Q1	Q2	O1	Q1	Q1
11	Q3	O2	Q2	Q3	O2	Q2	Q2
12	GND	GND	GND	VSS	GND	GND	GND
13	Q4	O3	Q3	Q4	O3	Q3	Q3
14	Q5	O4	Q4	Q5	O4	Q4	Q4
15	Q6	O5	Q5	Q6	O5	Q5	Q5
16	Q7	O6	Q6	Q7	O6	Q6	Q6
17	Q8	O7	Q7	Q8	O7	Q7	Q7
18	PD/PGM	$\overline{CE}$/PGM	CS2**	A11	$\overline{CE}$	A11	A11
19	A10	A10	A10	A10	A10	A10	A10
20	$\overline{CS}$	$\overline{OE}$	$\overline{CS1}$**	PD/$\overline{PGM}$	$\overline{OE}$/VPP	$\overline{S1}$**	$\overline{S1}$**
21	VPP	VPP	CS3*	VPP	A11	S2*	A12
22	A9	A9	A9	A9	A9	A9	A9
23	A8	A8	A8	A8	A8	A8	A8
24	VCC	VCC	VCC	VCC	VCC	VCC	VCC

NOTES

* Must be masked high enable

** Must be masked low enable



I.C. VOLTAGES		
REF DESIGNATION	+5V PIN NO.	GND PIN NO.
Z1 THRU Z11	14	7
Z12 THRU Z19	24	12
Z20, Z21, Z22	20	10

NOTE: UNLESS OTHERWISE SPECIFIED

1. REF ASSY DWG PA10-D200

(2) PINS 1C, 32a ON EURO CONNECTOR AND PINS Xa, Xc, Ya, Yc, 1C, 32a ON U.S. CONNECTOR SHALL BE TIED TO +5V

(3) PINS 1a, 3a, 5C, 8a, 10c, 13a, 15c, 18a, 20c, 23a, 25c, 28a, 30c, 32c, SHALL BE TIED TO GND.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON DECIMALS .XX = ± .03 .XXX = ± .010 ANGLES ± 30'

MATERIAL:

HEAT TREAT

FINISH

DASH NO. | NEXT ASSY | USED ON | APPLICATION

AUTHORIZATION NO.

DR BY RAND

CHK BY

APPD BY

PART NO.

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SCHEMATIC DIAGRAM- 16K BYTE PROM/ROM,

SIZE D | CODE IDENT NO. 34576 | DRAWING NO. PA10-X201

SCALE — | SHEET

PA10-X201

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