RM 65 FAMILY

32K Dynamic RAM Module

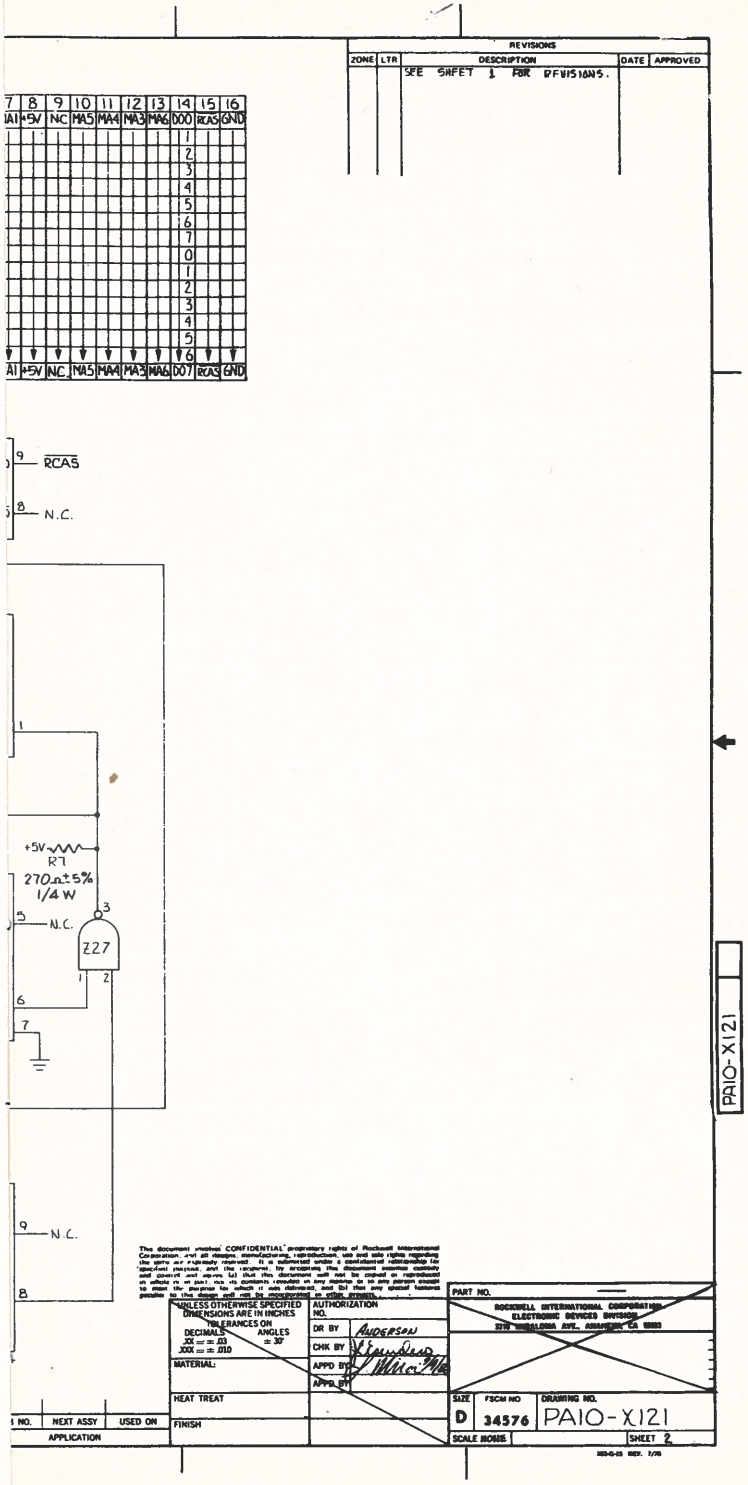
USER'S MANUAL

RM 65 FAMILY

Rockwell International

Document No.
29801 N08
Order No. 808
Rev. 1 October 1982

TABLE OF CONTENTS



LIST OF TABLES

LIST OF FIGURES

NOTES

SECTION 1

INTRODUCTION

1.1 PURPOSE/FUNCTION

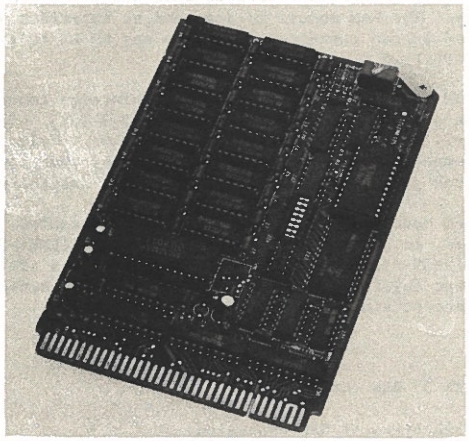
The RM 65 32K Dynamic RAM Module increases read and write memory capacity by 32,768 8-bit bytes. The RAM module is designed to interface with the Rockwell RM 65 bus. The module can connect directly to any RM 65 multi-slot card cage or single card adapter.

The 32K Dynamic RAM module is available in a 72-pin edge connector version (RM65-3132) and in a 64-pin Eurocard version (RM65-3132E). Both versions are shown in Figure 1-1. The pin assignments for the two versions are identical except the edge connector version has four additional pins connected to +5 Vdc, and four unused pins (see Table 3-1 for the pin assignments.)

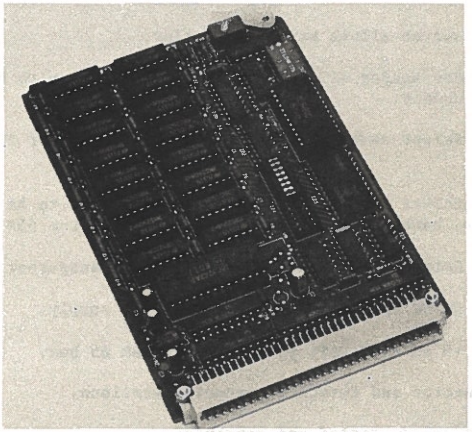
The 32K Dynamic RAM module is also available fully assembled, but without the Dynamic RAM devices, in both an edge connector version (RM65-3132N) and a Eurocard version (RM65-3132NE). The unpopulated versions are factory configured to accept multiple supply voltage dynamic RAM devices, but can also be configured to accept single +5 volt dynamic RAM devices.

1.2 FEATURES

- o Rockwell RM 65 Bus compatible.
- o Provides 32K bytes of RAM expansion.
- o Fully buffered bus interface.
- o Eight separately addressable 4K byte memory sections.
- o On-board switch allows Write Protection.
- o Base Address Header allows each 4K memory section to be assigned to any 4K boundary.
- o One Bank Select switch assigns the module to one of two 65K memory banks.
- o One Bank Select Enable switch allows the module to be common to both 65K memory banks or to be dedicated to one of the 65K memory banks.
- o Internal Refresh Controller is completely transparent to the RM 65 bus.
- o On-board DC/DC converter for -5 volt power supply.
- o Requires +5 and +12 volt power from the RM 65 bus.
- o Edge connector and Eurocard connector versions.
- o Fully assembled, tested and warranted.



a. Edge Connector Version



b. Eurocard Version

Figure 1-1. 32K Dynamic RAM Module

NOTES

NOTES

1.3 CHARACTERISTICS

The physical and electrical characteristics of the RAM module are listed in Table 1-1.

1.4 REFERENCE DOCUMENTS

Rockwell

Document No.	
29650N30	R6500 Programming Manual
29650N31	R6500 Hardware Manual
29650N36	AIM 65 Microcomputer User's Guide

Table 1-1. 32K Dynamic RAM Module Physical and Electrical Characteristics

Characteristic	Value
Dimensions (See Figure 1-2)	
Edge Connector Version	
Width	3.9 in. (100 mm)
Length	6.5 in. (164 mm)
Height	0.56 in. (14 mm)
Eurocard Version	
Width	3.9 in. (100 mm)
Length	6.3 in. (160 mm)
Height	0.56 in. (14 mm)
Weight	
Edge Connector	4.6 oz. (130 g)
Eurocard Version	4.9 oz. (140 g)
Service Condition	
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +85°C
Relative Humidity	0% to 85% (without condensation)
Power Requirements	
Populated with 16 multiple Supply Voltage Dynamic RAMs	+5 Vdc ± 5% 1.4a (7.4W) - Maximum +12 Vdc ±5% 170mA (2.0W) - Maximum
Unpopulated Module	+5Vdc ±5% 550mA (2.9W) - Maximum
Interface Connector P1	
Edge Connector Version	72-pin edge connector (0.100 in centers)
Eurocard Version	64-pin plug (0.100 in centers) per DIN 41612 (Row b not installed)

NOTES

NOTES

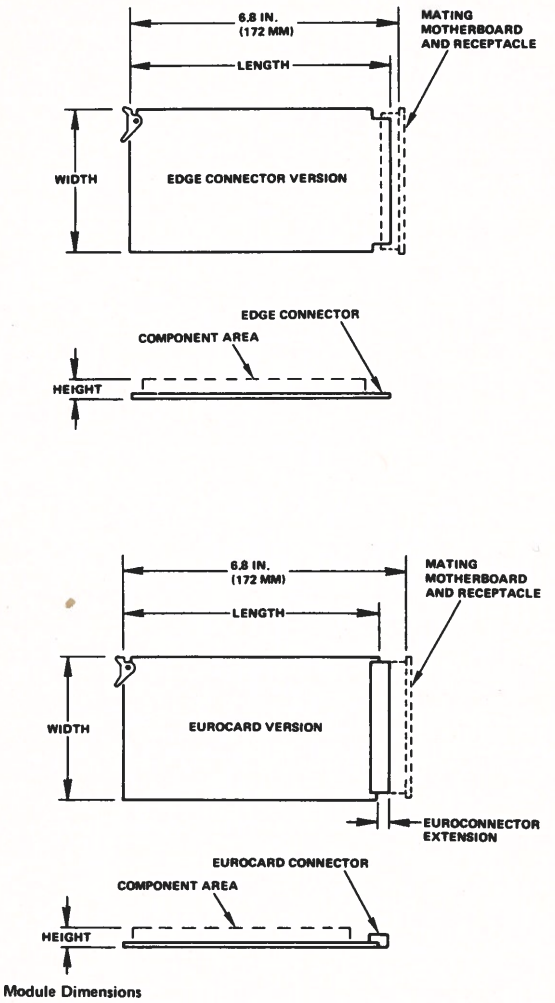


Figure 1-2. 32K Dynamic RAM Module Outline

SECTION 4

PROGRAMMING CONSIDERATIONS

A system memory map should be constructed or modified to include the address range for each of the eight 4K sections of the RAM module that are used. The map should reflect if the memory is included in a dedicated bank or common bank.

If less than the full 32K is desired, then the unused 4K sections must be disabled by connecting the corresponding Section pin to +5V (shown as DISABLE pin on Z24).

If bank addressing is used, BADR/ must be driven under software control. BADR/ must be controlled to select the desired bank before that bank is addressed.

Table 3-2. 32K Dynamic RAM Module I/O Signal Descriptions (Continued)

Mnemonic	Signal Name and Signal Description	Type
BR/$\overline{W}$/	Buffered Read/Write "NOT" A high BR/$\overline{W}$/ to an addressed RAM module provides a write enable to the Memory Controller (subject to write protect switch control).	TS
BØ2/	Buffered Phase 2 Clock "NOT" RAM addressing and data transfers are synchronized to the negative portion of the BØ2/ clock. Refresh is generated during the positive portion of the BØ2/ clock, which makes it transparent to the RM 65 bus.	TS

NOTE

Driver Type:
TS = Tri-State
OC = Open Collector

SECTION 2

INSTALLATION AND OPERATION

2.1 UNPACKING

Unpack the RAM module from its shipping carton and save the carton and packing material for storing the module. Referring to the packing sheet, verify that all of the parts are included.

2.2 OPERATING OPTIONS

Four operating options are selectable:

- o Base address selection header
- o Bank selection switch
- o Common versus Dedicated Memory switch
- o Write Protection switch

Figure 2-1 identifies the detail on the RAM module. The function of each switch and header is identified in Table 2-1 along with reference to the section and table that describes its use.

Table 2-1. RAM Module Switches and Header

Switch/Header	Function	References
Z24	Base Address Select for individual 4K RAM Sections	Section 2.2.1 Table 2-2
S1-2	Write Protect Switch	Section 2.2.3 Table 2-4
S1-3	Bank Select	Section 2.2.2 Table 2-3
S1-4	Bank Select Enable	Section 2.2.2 Table 2-3

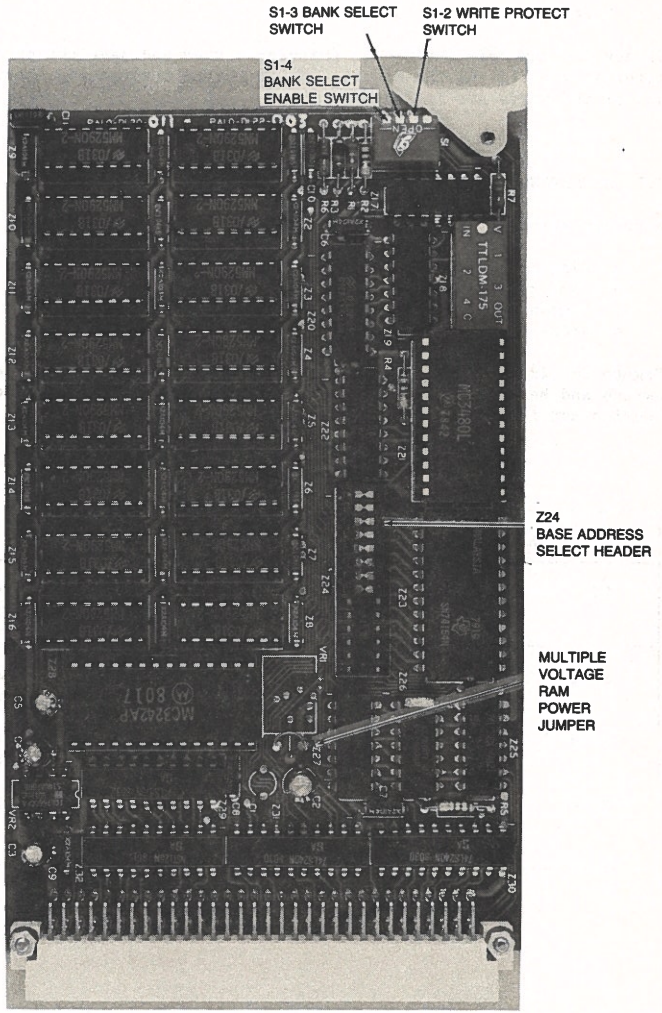


Figure 2-1. 32K RAM Module Detail

Table 3-2. 32K Dynamic RAM Module I/O Signal Descriptions

Mnemonic	Signal Name and Signal Description	Type
	NOTE: All signals interfaced to and from the RAM module are driven at TTL voltage levels.	
+5V	+5V dc supplied to the RAM module from the RM 65 Bus.	
+12V	+12V dc supplied to the RAM module from the RM 65 Bus.	
GND	Ground System ground.	
BA0/ - BA15/	Buffered Address Bits 0-15 Sixteen address lines transfer a 16-bit address from the RM 65 Bus to Address Buffers in the RAM module.	TS
BD0/ - BD7/	Buffered Data Bits 0-7 Eight bidirectional data lines transfer 8-bit data bytes between tri-state Data Transceivers and Latch in the RAM module and the RM 65 Bus.	TS
BACT/	Buffered Bus Active A low BACT/ indicates that the RAM module has been addressed and the Data Transceivers are enabled in either the receive (write operation) or transmit (read operation) direction.	OC
BADR/	Buffered Bank Address A high BADR/ addresses the lower 65K (Bank 0) memory bank; a low BADR/ addresses the upper 65K (Bank 1) memory bank.	TS
BR/$\overline{W}$	Buffered Read/Write A high BR/$\overline{W}$ (read operation) to an addressed RAM module enables the Data Transceivers to transfer the 8-bit data from the RAM module onto the RM 65 Bus. A low BR/$\overline{W}$ (write operation) to an addressed RAM module enables the Data Transceivers to transfer data from the RM 65 Bus into the RAM module.	TS

Table 3-1. Connector P1 (RM 65 Bus) Pin Assignments (Continued)

Pin	Signal Mnemonic	Signal Name	Input/Output
30a	BD2/	Buffered Data Bit 2	I/O
30c	GND	Ground	
31a	BD1/	Buffered Data Bit 1	I/O
31c	BD0/	Buffered Data Bit 0	I/O
32a	+5V	+5 Vdc	
32c	GND	Ground	
Ya	+5V	+5 Vdc (See Note)	
Yc	+5V	+5 Vdc (See Note)	
Za		Not Connected (See Note)	
Zc		Not Connected (See Note)	

NOTE

Pins Wa, Wc, Xa, Xc, Ya, Yc, Za and Zc are available on Edge Connector version only.

2.2.1 Base Address Selection

The RAM module is segmented into eight independent 4096 byte sections, Section 1 through Section 8. Each 4K section must be assigned a unique base address within the system memory map.

To configure the memory board for use, there must be eight address jumpers, one for each 4K section with a corresponding section pin number on Z24 as shown in Table 2-2a. Each of the eight section pins must be either assigned to one of the 16 base addresses or disabled, by connecting the jumper to the corresponding base address pin number on Z24 as shown in Table 2-2b. The section and base address pin numbers are shown on Z24 in Figure 2-2. The eight jumpers are soldered to the provided 28 pin Header for user configuration.

NOTE

Except for the four disable pins, no pin on Z24 should have more than one jumper connected. Wiring these jumpers improperly can cause damage to the module.

Table 2-2. Base Address Selection Pins

a. Pins for given Sections.

Section	Section Pin Number
1	28
2	27
3	26
4	25
5	24
6	23
7	22
8	21

b. Pins for given Base Address.

4K Base Address (Hexadecimal)	Base Address Pin Number
0000	17
1000	1
2000	2
3000	3
4000	4
5000	5
6000	6
7000	7
8000	8
9000	10
A000	11
B000	12
C000	13
D000	14
E000	15
F000	16
Disabled	9 or 18 or 19 or 20

Each of the eight Section pins must be connected to a unique Base Address pin, or disabled.

Table 3-1. Connector P1 (RM 65 Bus) Pin Assignments (Continued)

Pin	Signal Mnemonic	Signal Name	Input/Output
14c		Not Used	
15a		Not Used	
15c	GND	Ground	
16a		Not used	
16c		Not Used	
17a	+12V/+V	+12 Vdc	
17c		Not Used	
18a	GND	Ground	
18c		Not Used	
19a		Not Used	
19c		Not Used	
20a		Not Used	
20c	GND	Ground	
21a	BR/$\overline{W}$/	Buffered Read/Write "Not"	I
21c		Not Used	
22a		Not Used	
22c	BR/$\overline{W}$	Buffered Read/Write	I
23a	GND	Ground	
23c	BACT/	Buffered Bus Active	O
24a		Not Used	
24c		Not Used	
25a	BØ2/	Buffered Phase 2 "Not" Clock	I
25c	GND	Ground	
26a		Not Used	
26c		Not Used	
27a	BD7/	Buffered Data Bit 7	I/O
27c	BD6/	Buffered Data Bit 6	I/O
28a	GND	Ground	
28c	BD5/	Buffered Data Bit 5	I/O
29a	BD4/	Buffered Data Bit 4	I/O
29c	BD3/	Buffered Data Bit 3	I/O

Table 3-1. Connector P1 (RM 65 Bus) Pin Assignments

Pin	Signal Mnemonic	Signal Name	Input/Output
Wa		Not Connected (See Note)	
Wc		Not Connected (See Note)	
Xa	+5V	+5 Vdc (See Note 1)	
Xc	+5V	+5 Vdc (See Note 1)	
1a	GND	Ground	
1c	+5V	+5 Vdc	
2a	BADR/	Buffered Bank Address	I
2c	BA15/	Buffered Address Bit 15	I
3a	GND	Ground	
3c	BA14/	Buffered Address Bit 14	I
4a	BA13/	Buffered Address Bit 13	I
4c	BA12/	Buffered Address Bit 12	I
5a	BA11/	Buffered Address Bit 11	I
5c	GND	Ground	
6a	BA10/	Buffered Address Bit 10	I
6c	BA9/	Buffered Address Bit 9	I
7a	BA8/	Buffered Address Bit 8	I
7c	BA7/	Buffered Address Bit 7	I
8a	GND	Ground	
8c	BA6/	Buffered Address Bit 6	I
9a	BA5/	Buffered Address Bit 5	I
9c	BA4/	Buffered Address Bit 4	I
10a	BA3/	Buffered Address Bit 3	I
10c	GND	Ground	
11a	BA2/	Buffered Address Bit 2	I
11c	BA1/	Buffered Address Bit 1	I
12a	BA0/	Buffered Address Bit 0	I
12c		Not Used	
13a	GND	Ground	
13c		Not Used	
14a		Not Used	

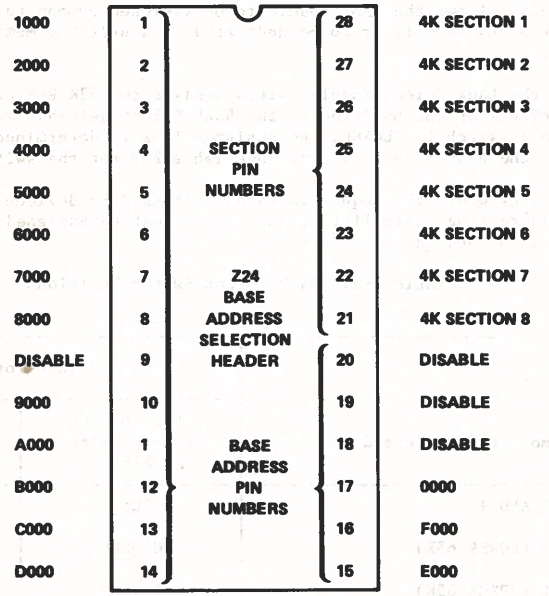


Figure 2-2. Base Address Selection Header Pin Assignments

> **NOTE**
>
> If bank addressing is used (see Section 2.2.2) in the system, the base address will be the same for each bank.

2.2.2 Bank Selection

The Bank Select Enable switch (S1-4), in conjunction with the Bank Select switch (S1-3), allows the RAM module to be assigned common to both memory banks (Bank 0 and Bank 1) or to be dedicated to a selected memory bank (Bank 0 or Bank 1).

When OPEN, the Bank Select Enable switch assigns the 32K RAM common to both banks regardless of the position of the Bank Select switch. When the Bank Select Enable switch is CLOSED, the assigned bank is determined by the position of the Bank Select switch. See Table 2-3 for the switch positions.

In applications where the module is to be addressed by devices that do not have bank addressing capabilities, the module must be assigned common to Bank 0 and Bank 1, or dedicated to Bank 0.

Table 2-3. Bank Select Switch Positions

Memory Bank Selected	Switch Position	
	Bank Select Enable Switch S1-4	Bank Select Switch S1-3
BANK 0 AND 1	OPEN	EITHER
BANK 0 (LOWER 65K)	CLOSED	OPEN
BANK 1 (UPPER 65K)	CLOSED	CLOSED

2.2.3 Write Protect Switch Selection

The Write Protect switch (S1-2) allows the entire 32K byte RAM to be write protected, i.e., data can be read from but data cannot be written into the RAM Module.

Memory Controller. If the Board Select and the Bank Select signals are both active, an enable is generated for the Memory Controller, the Data Transceivers and to drive the bus active signal.

The Write Control logic uses the Write Protect switch (S1-2) and the read/write signal to enable writing into the RAM. If the Write Protect switch is off, the Read/Write signal will be transferred directly to the Memory Controller. If the Write Protect switch is on, the Memory Controller will always be forced to a Read so that the contents of the RAM will not be altered.

The Timing Control generates all the clocks required by the Memory Controller, Memory Address Multiplexer, and the Refresh Clock. The Refresh Clock produces a single refresh strobe to the Refresh Counter for every seven RM 65 clock cycles.

The Memory Controller uses the clocks derived in the Timing Control to sequence the signals to the RAM devices. During the normal Read or Write cycles, the Memory Controller generates the Row and Column Address Strobes (RAS1, RAS2, CCAS) and the select signals for the Address Multiplexer (ROW EN) during a refresh cycle, the Memory Controller generates the select signal to place the Refresh Counter on the Address Multiplexer (REF EN) and Row Address Strobes for all RAM chips.

The Memory Address Multiplexer takes the fourteen LSB address lines and a seven bit Refresh Count and multiplexes then onto the 7 RAM address lines (MA0 - MA6). The ROW EN and REF EN signals from the Memory Controller determine whether the row address (BA0 - BA6), column address (BA7 - BA13) or refresh count are passed to the dynamic RAM devices.

The Refresh Counter is a modulo 128 counter which provides the row address for refresh purposes. The Refresh Clock provides a refresh strobe every seven BØ2 clock cycles, which increments the Refresh Counter. This provides a full refresh of all 128 rows of the dynamic RAM devices approximately every 0.9 milliseconds.

The RAM devices are 16,384 x 1 dynamic RAMs. Sixteen RAM devices are arranged as two-eight device blocks, with each device in a block corresponding to a data bit. The two blocks are enabled separately by the Row Address Strobes (RAS1, RAS2).

3.2 INTERFACE DESCRIPTION

Table 3-1 summarizes the pin assignments for connector P1. Table 3-2 defines the interface signals.

> **NOTE**
>
> "/" suffix denotes signal active at negative or low voltage level.

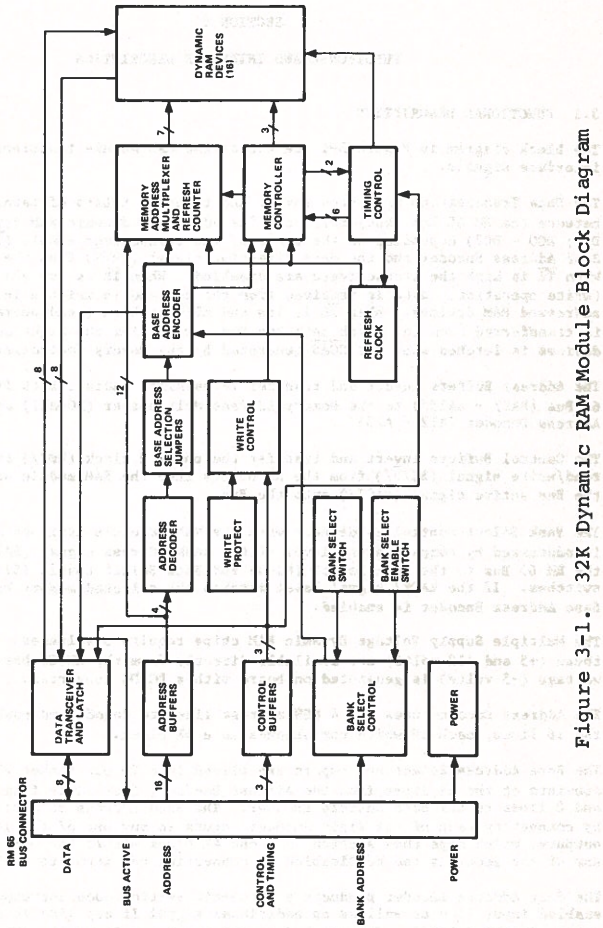


Figure 3-1. 32K Dynamic RAM Module Block Diagram

When CLOSED, the Write Protect switch prohibits writing into the RAM module. When OPEN, a Write Protect switch enables writing to the RAM module. Refer to Table 2-4 for Write Protect switch positions.

Table 2-4. Write Protect Switch Positions

Write Protect Selection	S1-2 Switch Position
WRITE PROTECT RAM MODULE	CLOSED
DISABLE WRITE PROTECT	OPEN

2.3 INSTALLING THE MODULE

Before installing the module, ensure that it is not damaged and is free of grease, dirt, liquid or other foreign material.

CAUTION

Prior to module installation turn off power to the interfacing RM 65 bus.

a. Based on the system memory map, select the proper module operation options as follows:

1. Select module base addresses with header Z24 (refer to Table 2-2).

NOTE

The 32K RAM is factory programmed for base address of $1000 through $8FFF contiguous. For any other memory map, this jumper must be removed from Z24 and replaced with a header programmed as described in Section 2.2.1.

2. Select common memory bank or dedicated memory bank operation and bank address by positioning switches S1-3 and S1-4 (refer to Table 2-3).

b. Align pin Wa (Edge Connector version) or pin 1a (Eurocard version) of the module with the corresponding pin on the mating RM 65 bus receptacle.

> **CAUTION**
>
> RM 65 connectors are keyed to prevent improper module connection. If the module does not insert into the receptacle with moderate pressure applied, check the orientation and connector alignment of the module. Forcing module improperly into the receptacle will damage the receptacle and/or the module.

c. Insert the RAM module into the desired card slot (if a card cage is used) and position it in front of the mating receptacle.

d. Press in firmly on the end of module until all pins are securely seated.

e. Reapply power to the RM 65 bus.

> **CAUTION**
>
> The 32K Dynamic RAM module requires both +5V and +12V power from the RM 65 bus when multiple supply voltage Dynamic RAM devices are used. The +5 volt power supply must always be applied before or at the same time as the +12 volt supply.

2.4 REMOVING THE MODULE

a. Turn-off power to the RM 65 bus.

> **CAUTION**
>
> The +12V power supply must always be turned off before or at the same time as the +5V supply.

b. If the module is installed in a card cage, lift up on the module ejector tab to release the module from the mating receptacle. Pull the module straight back until it is free from the card slot guides.

c. If the module is installed in a single card adapter, or in a motherboard without a card cage, pull back on the module while moving it slightly from side to side until it is free from the mating receptacle.

SECTION 3

FUNCTIONAL AND INTERFACE DESCRIPTION

3.1 FUNCTIONAL DESCRIPTION

The block diagram in Figure 3-1 identifies the RAM module functions and interface signals.

The Data Transceivers and Latch invert and transfer 8-bits of parallel data between the RM 65 Bus (BD0/-BD7/) and the addressed dynamic RAM devices (DI0 - DI7; DO0 - DO7) depending on the state of the transceiver enable ($\overline{TE}$) from the Base Address Encoder and the data direction signal (BR/$\overline{W}$) from the RM 65 bus. When $\overline{TE}$ is high the transceivers are disabled. When $\overline{TE}$ is low and BR/$\overline{W}$ is low (write operation), data is received from the Bus and is written into the eight addressed RAM devices. When $\overline{TE}$ is low and BR/$\overline{W}$ is high (read operation), data is transferred from the latch onto the Bus. Data from the eight addressed RAM devices is latched when the $\overline{CCAS}$ generated by the Memory Controller goes low.

The Address Buffers invert and transfer 16 parallel address bits from the RM 65 Bus (BA0/ - BA15/) to the Memory Address Multiplexer (A0-A11) and the Address Decoder (A12 - A15).

The Control Buffers invert and transfer the phase 2 clock (BØ2/) and read/write signal (BR/$\overline{W}$/) from the RM 65 Bus into the RAM module and drives the Bus active signal (BACT/) onto the Bus.

The Bank Select Controller detects when the RAM module's assigned memory bank is addressed by comparing the level of the bank address signal (BADR/) from the RM 65 Bus to the Bank Select (S1-3) and Bank Select Enable (S1-4) switches. If the BADR/ signal level matches the selected memory bank, the Base Address Encoder is enabled.

The Multiple Supply Voltage Dynamic RAM chips require 3 voltages. Two of these (+5 and +12 volts) are available directly from the RM 65 bus. The third voltage (-5 volts) is generated on board with a DC/DC converter.

The Address Decoder uses the 4 MSB address lines to decode and enable one of the 16 lines, each of which corresponds to a 4K block.

The Base Address Selection Jumpers are placed in a 28 pin socket which consists of the 16 lines from the Address Decoder, four lines from +5 volts, and 8 lines to the Base Address Encoder. The Base Address selection is made by connecting each of the eight encoder inputs to any one of the 16 decoder outputs, which maps that section into one 4K block within the 64K memory bank. Any of the sections can be disabled by connecting the input to a +5 volt pin.

The Base Address Encoder produces a three-bit section code corresponding to an enabled input line as well as an additional signal if any line is enabled column (Board Select). The two LSB of the section code become the two MSB of the address for the RAM devices, going into the Memory Address Multiplexer. The MSB of the section code becomes the select line for RAS strobe from the

2.5 INSTALLING THE RAM

The 32K Dynamic RAM Module unpopulated version is not supplied with RAM devices. The RAM devices must be installed in multiples of eight, so the module may be half populated (16K bytes) or fully populated (32K bytes). The eight sockets Z9-Z16 correspond to 4K Section 1 to 4, while the Z1-Z8 sockets correspond to Section 5 to 8. The board may be populated with either multiple voltage 16K Dynamic RAMs, or with the newer single voltage 16K Dynamic RAMs with pin assignments as shown in Table 2-5.

2.5.1 Multiple Voltage Dynamic RAM Devices

The factory installed Multiple Voltage RAM Power jumper is shown in Figure 2-3.

The multiple voltage devices must be of the following types, or equivalents:

Fairchild	F16K2
Motorola	MCM4116L-15
National	MM5290-2
TI	TMS4116-15

Install 8 or 16 Dynamic RAM devices, observing proper device type and polarity. The module may now be installed (refer to Section 2.3).

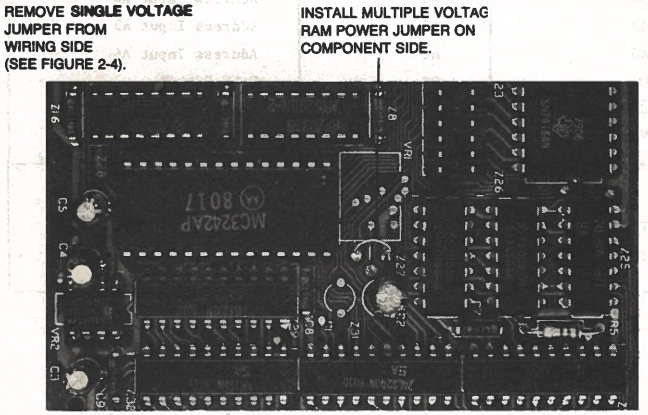


Figure 2-3. Multiple Voltage RAM Power Jumper Location

Table 2-5. Dynamic RAM Pin Assignments

Pin No.	Multiple Voltage RAM	Single Voltage RAM	Pin Signal Name
1	VBB (-5V)	NC	Supply Voltage
2	DI	DI	Data Input
3	$\overline{WE}$	$\overline{WE}$	Write Enable
4	$\overline{RAS}$	$\overline{RAS}$	Row Address Strobe
5	A0	AØ	Address Input AØ
6	A2	A2	Address Input A2
7	A1	A1	Address Input A1
8	VDD (+12V)	VCC (+5V)	Supply Voltage
9	VCC (+5V)	NC	Supply Voltage
10	A5	A5	Address Input A5
11	A4	A4	Address Input A4
12	A3	A3	Address Input A3
13	A6	A6	Address Input A6
14	DO	DO	Data Output
15	$\overline{CAS}$	$\overline{CAS}$	Column Address Strobe
16	VSS	VSS	Ground (GND)

NOTES

1. Tri-voltage and single-voltage RAM devices may not be mixed.
2. The RAM must be added a physical row (16K bytes) at a time.

2.5.2 Single Voltage Dynamic RAM Devices

To use the module with the single voltage Dynamic RAM devices, the board must be modified. The factory installed multiple voltage RAM power jumper (see Figure 2-3) must be removed. After removing this jumper, the single voltage RAM power jumper must be installed on the backside of the module as shown in Figure 2-4.

> **CAUTION**
>
> Power must not be applied to the module with both the multiple voltage RAM power jumper and the Single Voltage RAM power jumper installed, as this may result in damage to the module and/or other equipment connected to the RM 65 bus.

The Single Voltage RAM devices must be of the following types, or equivalents:

Intel	2118
Motorola	MCM4517
National	NMC5295

Install 8 or 16 Dynamic RAM devices, observing the proper device type and polarity. The module may now be installed (refer to Section 2.3).

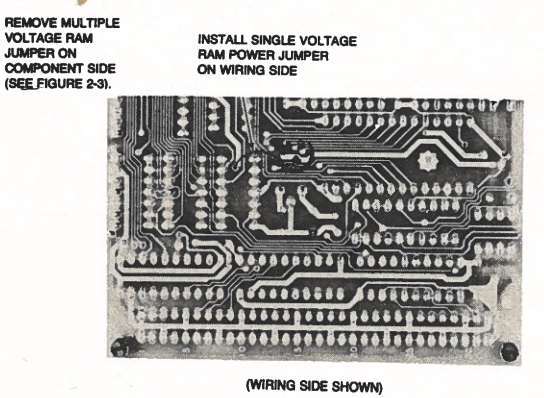


Figure 2-4. Single Voltage RAM Power Jumper Location