RM 65 FAMILY

8K Static RAM Module
USER'S MANUAL

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Rockwell International

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SECTION 1

INTRODUCTION

1.1 PURPOSE/FUNCTION

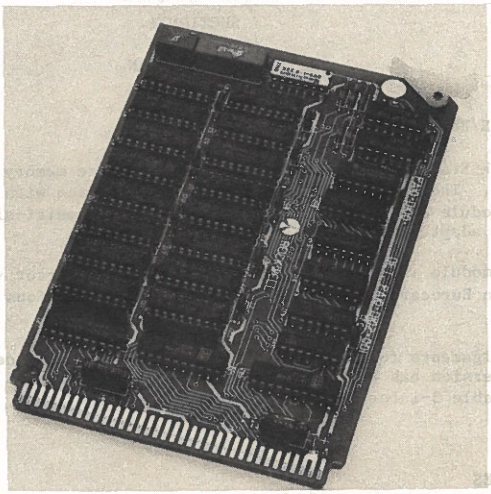
The RM 65 8K Static RAM Module increases read/write memory capacity by 8,192 8-bit bytes. The RAM module is designed to interface with the Rockwell RM 65 bus. The module can connect directly to any RM 65 multi-slot card cage or single card adapter.

The 8K RAM module is available in a 72-pin Edge Connector version (RM65-3108) and a 64-pin Eurocard version (RM65-3108E). Both versions are shown in Figure 1-1.

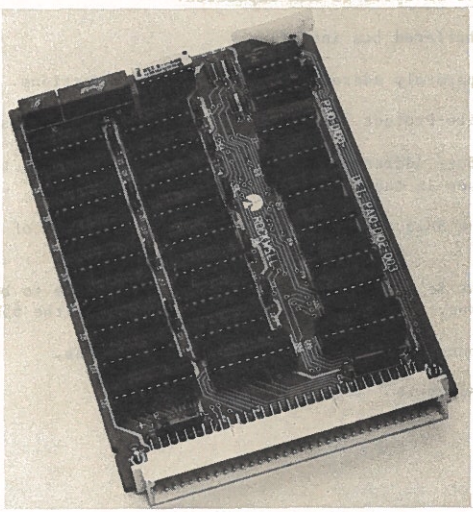
The pin assignments for the two versions are identical except the Edge Connector version has four additional pins connected to +5 Vdc and four unused pins (See Table 3-1 for the pin assignments).

1.2 FEATURES

- o Rockwell RM 65 Bus compatible.
- o Provides 8K bytes of RAM expansion.
- o Fully buffered bus interface.
- o Two separately addressable 4K byte memory sections.
- o Two Write-Protect switches, one for each 4K memory section.
- o Eight Base Address switches assign each 4K section to one of 16 base addresses in the selected 65K-byte memory bank.
- o One Bank Select switch assigns the module to one of two 65K memory banks.
- o One Bank Select Enable switch allows the module to be common to both 65K memory banks or to be dedicated to one of the 65K memory banks.
- o Edge connector and Eurocard connector versions.
- o Fully assembled, tested and warranted.



Edge Connector Version



b. Eurocard Version

Figure 1-1. 8K Static RAM Module

1.3 CHARACTERISTICS

The physical and electrical characteristics of the RAM module are listed in Table 1-1.

1.4 REFERENCE DOCUMENTS

Rockwell

Document No.	
29650N30	R6500 Programming Manual
29650N31	R6500 Hardware Manual
29650N36	AIM 65 Microcomputer User's Guide
29650N82	RM 65 Bus Description

Table 1-1. 8K Static RAM Module Physical and Electrical Characteristics

Characteristic	Value
Dimensions (See Figure 1-2)	
Edge Connector Version	
Width	3.9 in. (100 mm)
Length	6.5 in. (164 mm)
Height	0.56 in. (14 mm)
Eurocard Version	
Width	3.9 in. (100 mm)
Length	6.3 in. (160 mm)
Height	0.56 in. (14 mm)
Weight	
Edge Connector	4.9 oz. (135g)
Eurocard Version	5.3 oz. (145g)
Service Condition	
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +85°C
Relative Humidity	0% to 85% (without condensation)
Power Requirements	
Voltage	+5 Vdc $\pm$ 5%
Amperage and Power	1.0 amperes (5.0 watts) - typical 1.9 amperes (9.5 watts) - maximum
Interface Connector P1	
Edge Connector Version	72-pin edge connector (0.100 in. centers)
Eurocard Version	64-pin plug (0.100 in. centers) per DIN 41612 (Row b not installed)

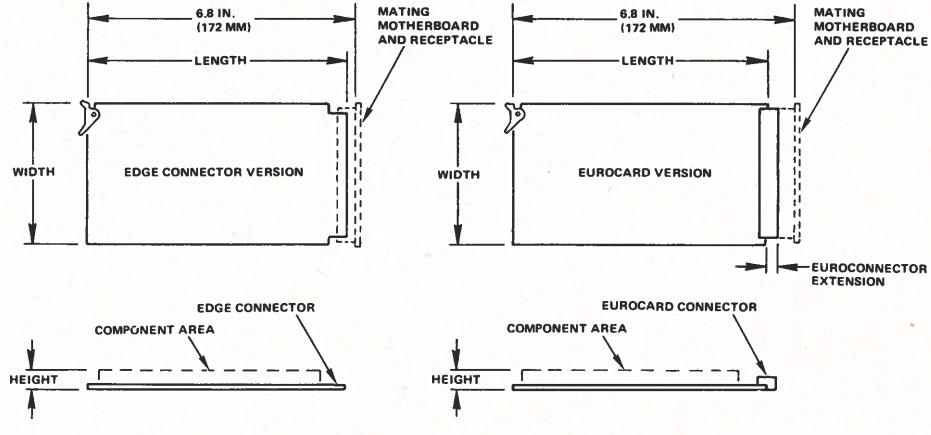


Figure 1-2. 8K Static RAM Module Outline

SECTION 2

INSTALLATION AND OPERATION

2.1 UNPACKING

Unpack the RAM module from its shipping carton and save the carton and packing material for storing the module. Referring to the packing sheet, verify that all of the parts are included.

2.2 OPERATING OPTIONS

Four operating options are switch selectable:

- o Base address selection
- o Bank selection
- o Common Versus Dedicated Memory Banks
- o Write Protection

Figure 2-1 identifies the switches on the RAM module. The function of each switch is identified in Table 2-1 along with reference to the section and table that describes its use.

Table 2-1. 8K Static RAM Module Switches

Switch	Function	References
S1-1 through S1-4	Base Address Select for 4K RAM Section 1	Section 2.2.1 Table 2-2
S1-5 through S1-8	Base Address Select for 4K RAM Section 2	
S2-1	Bank Select	Section 2.2.2 Table 2-3
S2-2	Bank Select Enable	
S2-3	Write Protect Switch for 4K RAM Section 1	Section 2.2.3 Table 2-4
S2-4	Write Protect Switch for 4K RAM Section 2	

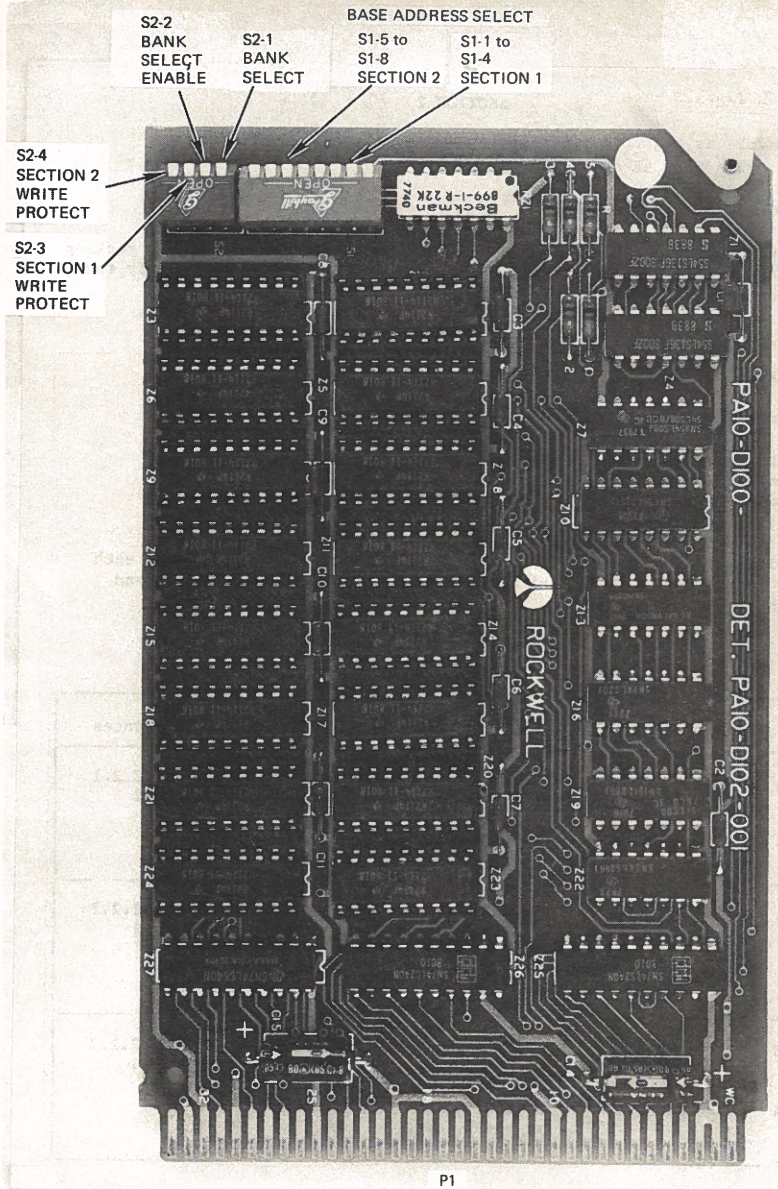


Figure 2-1. 8K RAM Module Switches

2.2.1 Base Address Selection

The RAM module is segmented into two independent 4096 byte sections, Section 1 and Section 2. Each 4K section must be assigned a unique base address within the system memory map.

The positions of switches S1-1 through S1-4 and S1-5 through S1-8 select the starting (base) address for Sections 1 and 2, respectively. The switch positions are described in Table 2-2.

Table 2-2. Base Address Select Switch Positions

4K Base Address (Hexadecimal)	Switch S1 Positions							
	4K RAM Section 1				4K RAM Section 2			
	S1-4	S1-3	S1-2	S1-1	S1-8	S1-7	S1-6	S1-5
0000	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN
1000	OPEN	OPEN	OPEN	CLOSED	OPEN	OPEN	OPEN	CLOSED
2000	OPEN	OPEN	CLOSED	OPEN	OPEN	OPEN	CLOSED	OPEN
3000	OPEN	OPEN	CLOSED	CLOSED	OPEN	OPEN	CLOSED	CLOSED
4000	OPEN	CLOSED	OPEN	OPEN	OPEN	CLOSED	OPEN	OPEN
5000	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED
6000	OPEN	CLOSED	CLOSED	OPEN	OPEN	CLOSED	CLOSED	OPEN
7000	OPEN	CLOSED	CLOSED	CLOSED	OPEN	CLOSED	CLOSED	CLOSED
8000	CLOSED	OPEN	OPEN	OPEN	CLOSED	OPEN	OPEN	OPEN
9000	CLOSED	OPEN	OPEN	CLOSED	CLOSED	OPEN	OPEN	CLOSED
A000	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN
B000	CLOSED	OPEN	CLOSED	CLOSED	CLOSED	OPEN	CLOSED	CLOSED
C000	CLOSED	CLOSED	OPEN	OPEN	CLOSED	CLOSED	OPEN	OPEN
D00C	CLOSED	CLOSED	OPEN	CLOSED	CLOSED	CLOSED	OPEN	CLOSED
E000	CLOSED	CLOSED	CLOSED	OPEN	CLOSED	CLOSED	CLOSED	OPEN
F000	CLOSED	CLOSED	CLOSED	CLOSED	CLOSED	CLOSED	CLOSED	CLOSED

NOTE

If bank addressing is used (see Section 2.2.2) in the system, the base address will be the same for each bank.

2.2.2 Bank Selection

The Bank Select Enable switch (S2-2), in conjunction with the Bank Select switch (S2-1), allows the RAM module to be assigned common to both memory banks (Bank 0 and Bank 1) or to be dedicated to a selected memory bank (Bank 0 or Bank 1).

When OPEN, the Bank Select Enable switch assigns the 8K RAM common to both banks regardless of the position of the Bank Select switch. When the Bank Select Enable switch is CLOSED, the assigned bank is determined by the position of the Bank Select switch. See Table 2-3 for the switch positions.

In applications where the module is to be addressed by devices that do not have bank addressing capabilities, the module must be assigned common to Bank 0 and Bank 1, or dedicated to Bank 0.

Table 2-3. Bank Select Switch Positions

Memory Bank Selected	Switch Position	
	Bank Select Enable Switch S2-2	Bank Select Switch S2-1
BANK 0 AND 1	OPEN	EITHER
BANK 0 (LOWER 65K)	CLOSED	OPEN
BANK 1 (UPPER 65K)	CLOSED	CLOSED

2.2.3 Write Protect Switch Selection

The two Write Protect switches (S2-3 and S2-4) allow the two 4K byte RAM sections to be individually write protected, i.e., data can be read from but data cannot be written into the corresponding 4K section.

When CLOSED, a Write Protect switch prohibits writing into the corresponding 4K section. When OPEN, a Write Protect switch enables writing to the corresponding 4K section. Refer to Table 2-4 for Write Protect switch positions.

Table 2-4. Write Protect Option Selection Procedures

Write Protect Selection	Switch	Switch Position
WRITE PROTECT 4K RAM SECTION 1	S2-3	CLOSED
WRITE PROTECT 4K RAM SECTION 2	S2-4	CLOSED

2.3 INSTALLING THE MODULE

Before installing the module, ensure that it is not damaged and is free of grease, dirt, liquid or other foreign material.

CAUTION

Prior to module installation turn off power to the interfacing RM 65 bus.

a. Based on the system memory map, select the proper module operation options as follows:

   1. Select module base addresses by positioning switches S1-1 through S1-8 (refer to Table 2-2).

   2. Select common memory bank or dedicated memory bank operation by positioning switches S2-1 and S2-2 (refer to Table 2-3).

b. Align pin Wa (Edge Connector version) or pin 1a (Eurocard version) of the module with the corresponding pin on the mating RM 65 bus receptacle.

CAUTION

RM 65 Bus connectors are keyed to prevent improper module connection. If the module does not insert into the receptacle with moderate pressure applied, check the orientation and connector alignment of the module. Forcing module improperly into the receptacle will damage the receptacle and/or the module.

c. Insert the RAM module into the desired card slot (if a card cage is used) and position it in front of the mating receptacle.

d. Press in firmly on the end of module until all pins are securely seated.

e. Reapply power to the RM 65 bus.

2.4 REMOVING THE MODULE

a. Turn-off power to the RM 65 bus.

b. If the module is installed in a card cage, lift up on the module ejector tab to release the module from the mating receptacle. Pull the module straight back until it is free from the card slot guides.

c. If the module is installed in a single card adapter, or in a motherboard without a card cage, pull back on the module while moving it slightly from side to side until it is free from the mating receptacle.

SECTION 3

FUNCTIONAL AND INTERFACE DESCRIPTION

3.1 FUNCTIONAL DESCRIPTION

The block diagram in Figure 3-1 identifies the RAM module functions and interface signals.

The Data Transceivers invert and transfer 8-bits of parallel data between the addressed 2114 RAM devices (D0 - D7) and the RM 65 Bus (BD0/ - BD7/) depending on the state of the transceiver enable ($\overline{DBEN}$) and data direction ($\overline{DFMEM}$) signals from the Data Transceiver control circuit. When $\overline{DBEN}$ is high, the transceivers are disabled. When $\overline{DBEN}$ is low and $\overline{DFMEM}$ is high (write operation), data is received from the bus and is written into two addressed 2114 RAM devices. When $\overline{DBEN}$ is low and $\overline{DFMEM}$ is low (read operation), data is read from two addressed 2114 RAM devices and transmitted onto the bus.

The Address Buffers invert and transfer 16 parallel address bits from the RM 65 Bus (BA0/ - BA15/) to the 2114 RAM devices (A0 - A9), the Chip Select Decoder (A10 and A11) and to the Base Address Decoders (A12 - A15).

The Control Buffers invert and transfer control signals BØ2/ and BR/$\overline{W}$/ from the RM 65 Bus onto the RAM module and drives BACT/ onto the RM 65 Bus.

The Bank Select Controller detects when the RAM module's assigned memory bank is addressed by comparing the level of the bank address signal (BADR/) from the RM 65 Bus to the Bank Select (S2-1) and Bank Select Enable (S2-2) switches. If the BADR/ signal level matches the selected memory bank and the Bank Select Enable switch is enabled, BKSEL is set low to enable chip select decoding, otherwise BKSEL is high to disable decoding. If Bank Select Enable Switch is disabled, BKSEL is always low.

Two Base Address Decoders detect when either 4K RAM Section 1 or 2 is addressed by comparing address lines A15-A12 to the positions set on the Section 1 (S1-1 through S1-4) and Section 2 (S1-5 through S1-8) Base Address Select switches. When a match occurs, select signal 4KSELA or 4KSELB is set low to also enable chip select decoding, otherwise 4KSELA and 4KSELB are reset high to disable chip select decoding.

The Section 1 and Section 2 Chip Select Decoder is enabled by outputs from the Bank Select Controller (BKSEL) and the Base Address Decoders (4KSELA and 4KSELB). When enabled by a low BKSEL and either a low 4KSELA or 4KSELB, address lines A11 and A10 are decoded to generate one of the chip select lines ($\overline{CS0}$ - $\overline{CS7}$) to enable two of the 1K x 4 bit 2114 RAM devices. Signal SELA or SELB is generated to indicate when a chip select line is active for use by the Write Control and Data Transceiver Control Circuits.

The Write Control circuit generates the $\overline{WENA}$ and $\overline{WENB}$ write enable signals to the 4K Section 1 and the 4K Section 2 RAM devices, respectively, and to the Data Transceiver Control circuit. The appropriate write enable line is set low during Ø2 high of a write operation (BR/$\overline{W}$ low) to write the data on the

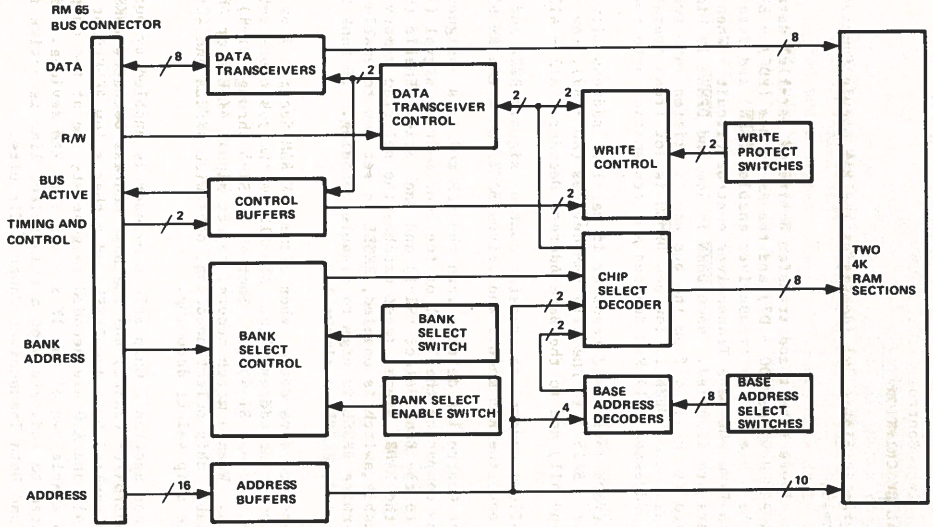


Figure 3-1. 8K RAM Module Block Diagram

D0 - D7 lines into the RAM devices, if the corresponding Write Protect switch (S2-3 or S2-4) is off. If the Write Protect switch is on, the write enable line remains high and the Data Transceivers are disabled ($\overline{DBEN}$ is high).

The Data Transceiver Control Circuit determines when an on-board read or write operation is in progress and outputs transceiver enable ($\overline{DBEN}$) and data direction ($\overline{DFMEN}$) signals. $\overline{DBEN}$ is set low to enable the transceivers and to drive the bus active signal (BACT/) when either 4K Section 1 or 4K Section 2 is selected (SELA or SELB is high from the Chip Select Decoder). A high $\overline{DFMEM}$ is generated when BR/$\overline{W}$ is low to indicate receive to the Data Transceivers (write operation) otherwise a low $\overline{DFMEM}$ is generated when BR/$\overline{W}$ is high to indicate transmit to the Data Transceivers (read operation).

Sixteen 2114 Static RAM devices are divided into two separately addressable 4K byte sections. Chip select signals $\overline{CS0}$ - $\overline{CS3}$ are input to 4K Section 1 while $\overline{CS4}$ - $\overline{CS7}$ are input to 4K Section 2.

3.2 INTERFACE DESCRIPTION

Table 3-1 summarizes the pin assignments for connector P1. Table 3-2 defines the interface signals.

> **NOTE**
>
> "/" suffix denotes signal active at negative or low voltage level.

Table 3-1. Connector P1 (RM 65 Bus) Pin Assignments

Pin	Signal Mnemonic	Signal Name	Input/Output
Wa		Not Connected (See Note)	
Wc		Not Connected (See Note)	
Xa	+5V	+5 Vdc (See Note)	
Xc	+5V	+5 Vdc (See Note)	
1a	GND	Ground	
1c	+5V	+5 Vdc	
2a	BADR/	Buffered Bank Address	I
2c	BA15/	Buffered Address Bit 15	I
3a	GND	Ground	
3c	BA14/	Buffered Address Bit 14	I
4a	BA13/	Buffered Address Bit 13	I
4c	BA12/	Buffered Address Bit 12	I
5a	BA11/	Buffered Address Bit 11	I
5c	GND	Ground	
6a	BA10/	Buffered Address Bit 10	I
6c	BA9/	Buffered Address Bit 9	I
7a	BA8/	Buffered Address Bit 8	I
7c	BA7/	Buffered Address Bit 7	I
8a	GND	Ground	
8c	BA6/	Buffered Address Bit 6	I
9a	BA5/	Buffered Address Bit 5	I
9c	BA4/	Buffered Address Bit 4	I
10a	BA3/	Buffered Address Bit 3	I
10c	GND	Ground	
11a	BA2/	Buffered Address Bit 2	I
11c	BA1/	Buffered Address Bit 1	I
12a	BA0/	Buffered Address Bit 0	I
12c		Not Used	
13a	GND	Ground	
13c		Not Used	

Table 3-1. Connector P1 (RM 65 Bus) Pin Assignments (Continued)

Pin	Signal Mnemonic	Signal Name	Input/Output
14a		Not Used	
14c		Not Used	
15a		Not Used	
15c	GND	Ground	
16a		Not used	
16c		Not Used	
17a		Not Used	
17c		Not Used	
18a	GND	Ground	
18c		Not Used	
19a		Not Used	
19c		Not Used	
20a		Not Used	
20c	GND	Ground	
21a	BR/$\overline{W}$/	Buffered Read/Write "Not"	I
21c		Not Used	
22a		Not Used	
22c	BR/$\overline{W}$	Buffered Read/Write	I
23a	GND	Ground	
23c	BACT/	Buffered Bus Active	O
24a		Not Used	
24c		Not Used	
25a	BØ2/	Buffered Phase 2 "Not" Clock	I
25c	GND	Ground	
26a		Not Used	
26c		Not Used	
27a	BD7/	Buffered Data Bit 7	I/O
27c	BD6/	Buffered Data Bit 6	I/O
28a	GND	Ground	
28c	BD5/	Buffered Data Bit 5	I/O

Table 3-1. Connector P1 (RM 65 Bus) Pin Assignments (Continued)

Pin	Signal Mnemonic	Signal Name	Input/Output
29a	BD4/	Buffered Data Bit 4	I/O
29c	BD3/	Buffered Data Bit 3	I/O
30a	BD2/	Buffered Data Bit 2	I/O
30c	GND	Ground	
31a	BD1/	Buffered Data Bit 1	I/O
31c	BD0/	Buffered Data Bit 0	I/O
32a	+5V	+5 Vdc	
32c	GND	Ground	
Ya	+5V	+5 Vdc (See Note)	
Yc	+5V	+5 Vdc (See Note)	
Za		Not Connected (See Note)	
Zc		Not Connected (See Note)	

NOTE

Pins Wa, Wc, Xa, Xc, Ya, Yc, Za and Zc are available on Edge Connector version only.

Table 3-2. Connector P1 (RM 65 Bus) Signal Descriptions

MNEMONIC	SIGNAL NAME AND SIGNAL DESCRIPTION	TYPE
	NOTE: All signals interfaced to and from the RAM module are driven at TTL voltage levels.	
+5V	+5V dc supplied to the RAM module via the RM 65 Bus.	
GND	Ground System ground.	
BA0/ - BA15/	Buffered Address Bits 0-15 Sixteen address lines transfer a 16-bit address from the RM 65 Bus to Address Buffers in the RAM module.	TS
BD0/ - BD7/	Buffered Data Bits 7-0 Eight bidirectional data lines transfer 8-bit data bytes between tri-state Data Transceivers in the RAM module and the RM 65 Bus.	TS
BACT/	Buffered Bus Active A low BACT/ indicates that the RAM module has been addressed and the Data Transceivers are enabled in either the receive (write operation) or transmit (read operation) direction.	OC
BADR/	Buffered Bank Address A high BADR/ addresses the lower 65K (Bank 0) memory bank; a low BADR/ addresses the upper 65K (Bank 1) memory bank.	TS
BR/$\overline{W}$	Buffered Read/Write A high BR/$\overline{W}$ (read operation) to an addressed RAM module enables the Data Tranceivers to transfer the 8-bit data from the RAM module onto the RM 65 Bus. A low BR/$\overline{W}$ (write operation) to an addressed RAM module enables the Data Transreceivers to transfer data from the RM 65 Bus onto the RAM module (subject to Write Protect switch control).	TS

Table 3-2. Connector P1 (RM 65 Bus) Signal Descriptions

MNEMONIC	SIGNAL NAME AND SIGNAL DESCRIPTION	TYPE
BR/$\overline{W}$/	Buffered Read/Write "NOT" A high BR/$\overline{W}$/ to an addressed RAM module provides a write enable to the RAM devices (subject to Write Protect switch control).	TS
BØ2/	Buffered Phase 2 Clock "NOT" RAM addressing and data transfers are synchronized to the negative portion of the BØ2/ clock.	TS

NOTE

Driver Type:
TS = Tri-State
OC = Open Collector

SECTION 4

PROGRAMMING CONSIDERATIONS

A system memory map should be constructed to include the address range for each of the two 4K sections of the RAM module that are used. The map should reflect if the memory is included in a dedicated bank or common bank.

If bank addressing is used, BADR/ must be driven under software control. BADR/ must select the desired bank before that bank is addressed.

APPENDIX A

RAM MODULE TEST PROGRAM

This appendix describes a RAM test program that may be run using the AIM 65 microcomputer. An assembly listing of the test program is included.

The procedure to run the test is:

a. Set up the base address of the RAM module(s). Note that contiguous addressing must be provided from the first RAM address through the last RAM address.

b. Load the test program object code into RAM.

c. Type F1 to initiate the test. AIM 65 will display:

```
<[>
NO. OF RAM MODULES?
```

d. Enter the number of installed RAM modules (from 1 to 4). AIM 65 will ask for the base address:

```
FIRST ADDRESS? =
```

e. Enter the lowest module base address, in hexadecimal, e.g., $1000. End the input with RETURN. AIM 65 will initiate the test.

f. If any errors are detected, the error heading will be displayed followed by the address of each error and the associated actual (IS) and expected (SB) data values:

```
ERROR LIST
ADDR IS SB
1022 04 0C      (Example)
```

g. At the completion of the test, the number of errors are displayed in decimal:

```
0001 ERRORS     (Example)
```

h. The socket containing the erroneous RAM may be determined from the address of the error in Section 1 or Section 2:

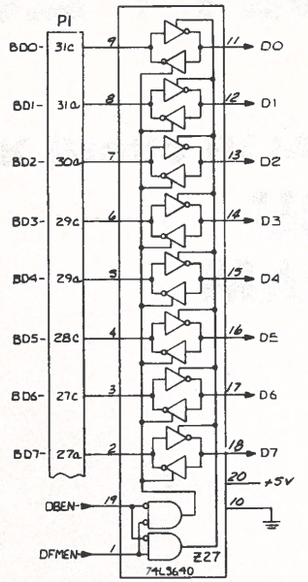
ADDRESS	FAILED BYTE			
	SECTION 1		SECTION 2	
	HIGH	LOW	HIGH	LOW
X000 - X3FF	Z2	Z3	Z14	Z15
X400 - X7FF	Z5	Z6	Z17	Z18
X800 - XBFF	Z8	Z9	Z20	Z21
XC00 - XFFF	Z11	Z12	Z23	Z24

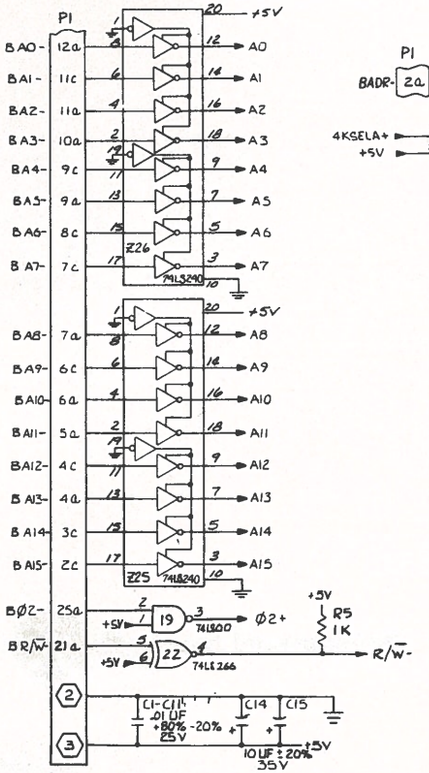
```
PAGE 0001                    8K STATIC RAM MODULE TEST      8/5/80

0002  0000              ; AIM 65 MONITOR LINKAGE
0003  E1A1=             COMIN   =$E1A1          ;RETURN TO MONITOR
0004  E973=             REDOUT  =$E973          ;DISPLAY CURSOR; READ 1 CHAR
0005  EA46=             NUMA    =$EA46          ;PRINT A BYTE AS TWO HEX DIGITS
0006  E83E=             BLANK   =$E83E          ;PRINT A BLANK
0007  E97A=             OUTPUT  =$E97A          ;OUTPUT TO D/P
0008  EA13=             CRLOW   =$EA13          ;CR TO D/P
0009  EAAE=             ADDIN   =$EAAE          ;READ IN ADDR

0011  A41C=             ADDR    =$A41C          ;RAM USED BY ADDIN

0013  0000              ;PAGE 0 VARIABLES
0014  0000                      *=$00
0015  0000              AD1     *=*+2
0016  0002              AD2     *=*+2
0017  0004              END     *=*+1
0018  0005              ERRS    *=*+2
0019  0007              SB      *=*+1
0020  0008              FLAG    *=*+1
0021  0009              IS      *=*+1


0023  000A              ;F1 KEY LINKAGE
0024  000A                      *=$10C
0025  010C  4C 00 02            JMP F1          ;RAM TEST

0027  010F              ;MAIN PROGRAM
0028  010F                      *=$200
0029  0200  20 13 EA    F1      JSR CRLOW
0030  0203  A2 00               LDX #00
0031  0205  86 06               STX ERRS+1
0032  0207  86 05               STX ERRS
0033  0209  86 08               STX FLAG
0034  020B  20 E0 02            JSR MSG         ;'NO. OF RAM MODULES?'
0035  020E  20 73 E9            JSR REDOUT      ;GET A KEY
0036  0211  20 13 EA            JSR CRLOW       ;CLEAR LINE
0037  0214  C9 31               CMP #$31        ;<1?
0038  0216  90 E8               BCC F1          ;BETWEEN 1 AND 4 BOARDS ONLY
0039  0218  C9 35               CMP #$35        ;>4?
0040  021A  B0 E4               BCS F1
0041  021C  29 0F               AND #$0F        ;MAKE A HEX NO.
0042  021E  A2 05               LDX #05
0043  0220  0A          ROLL    ASL A           ;TIMES 16 GIVES RAM LEN
0044  0221  CA                  DEX
0045  0222  D0 FC               BNE ROLL
0046  0224  85 04               STA END
0047  0226  A2 13       ADDRGT  LDX #MSG2-MSG1
0048  0228  20 E0 02            JSR MSG         ;'FIRST ADDRESS?'
0049  022B  20 AE EA            JSR ADDIN       ;GET 4 DIGITS
0050  022E  B0 F6               BCS ADDRGT      ;ERROR
0051  0230  20 13 EA            JSR CRLOW
0052  0233  AD 1C A4            LDA ADDR
0053  0236  D0 EE               BNE ADDRGT
0054  0238  AD 1D A4            LDA ADDR+1
0055  023B  C9 10               CMP #$10        ;HAS TO BE OFF BOARD
0056  023D  90 E7               BCC ADDRGT
0057  023F  18                  CLC             ;ADD TO LEN TO GET END
0058  0240  65 04               ADC END
```

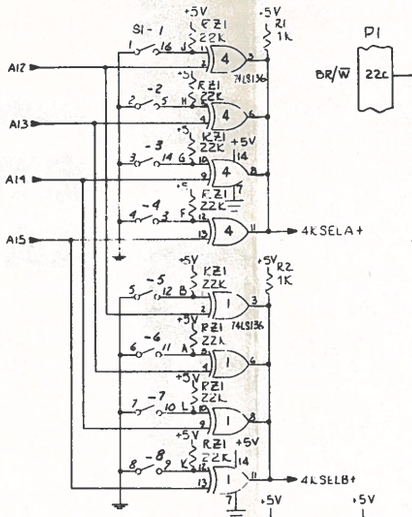
```
0059  0242  85 04           STA END
0060  0244  A2 03           LDX #03          ;SET PATTERN COUNT
0061  0246  20 EE 02  NPAT   JSR SET         ;MOVE START TO AD1 & AD2
0062  0249  A0 00           LDY #00
0063  024B  BD 39 03  GSTORE LDA PAT,X       ;GET PATTERN
0064  024E  85 07           STA SB           ;SAVE FOR ERRORS
0065  0250  91 00     STORE  STA (AD1),Y     ;AND FILL MEMORY
0066  0252  C8              INY              ;WITH IT
0067  0253  D0 FB           BNE STORE
0068  0255  E6 01           INC AD1+1
0069  0257  A5 01           LDA AD1+1
0070  0259  C5 04           CMP END
0071  025B  D0 EE           BNE GSTORE       ;NEED TO RELOAD PATTERN
0072  025D  B1 02     COMPAR LDA (AD2),Y     ;CHECK BYTE POINTED TO
0073  025F  C5 07           CMP SB           ;IS IT OKAY?
0074  0261  F0 05           BEQ NEXT
0075  0263  85 09           STA IS           ;NO, SAVE VALUE
0076  0265  20 99 02        JSR ERROR        ;AND RECORD ERROR
0077  0268  BD 38 03  NEXT   LDA PAT-1,X     ;STORE NEXT PATTERN
0078  026B  91 02           STA (AD2),Y
0079  026D  E6 02           INC AD2          ;ADD 1 TO AD2 & AD2+1
0080  026F  D0 EC           BNE COMPAR
0081  0271  E6 03           INC AD2+1
0082  0273  A5 03           LDA AD2+1        ;CHECK FOR END
0083  0275  C5 04           CMP END
0084  0277  D0 E4           BNE COMPAR       ;RTN IF NOT DONE
0085  0279  20 EE 02        JSR SET
0086  027C  BD 38 03        LDA PAT-1,X
0087  027F  85 07           STA SB
0088  0281  CA              DEX              ;NEXT PATTERN
0089  0282  10 D9           BPL COMPAR
0090  0284  20 13 EA        JSR CRLOW        ;DONE
0091  0287  A5 06           LDA ERRS+1       ;PRINT ERROR COUNT
0092  0289  20 46 EA        JSR NUMA
0093  028C  A5 05           LDA ERRS
0094  028E  20 46 EA        JSR NUMA
0095  0291  A2 21           LDX #MSG3-MSG1
0096  0293  20 DA 02        JSR MSGCR        ;'ERRORS'
0097  0296  4C A1 E1        JMP COMIN        ;RTN TO MONITOR

0099  0299  8A        ERROR  TXA
0100  029A  48              PHA
0101  029B  A5 08           LDA FLAG
0102  029D  D0 0D           BNE NOHD         ;ZERO FIRST TIME ONLY
0103  029F  E6 08           INC FLAG
0104  02A1  20 13 EA        JSR CRLOW
0105  02A4  A2 2B           LDX #MSG4-MSG1
0106  02A6  20 DA 02        JSR MSGCR        ;'ERROR LIST'
0107  02A9  20 DA 02        JSR MSGCR        ;'ADDR IS SB'
0108  02AC  A5 03     NOHD  LDA AD2+1
0109  02AE  20 46 EA        JSR NUMA         ;PRINT CURRENT ADDR
0110  02B1  A5 02           LDA AD2
0111  02B3  20 D4 02        JSR NUMBLK
0112  02B6  A5 09           LDA IS           ;DISPLAY CURRENT CONTENTS
0113  02B8  20 D4 02        JSR NUMBLK
0114  02BB  A5 07           LDA SB           ;DISPLAY WHAT SHOULD BE
0115  02BD  20 46 EA        JSR NUMA
0116  02C0  F8              SED              ;INC ERRS
```

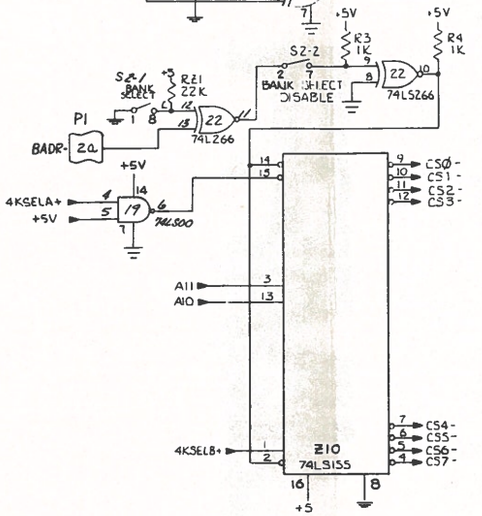
```
PAGE 0003                    8K STATIC RAM MODULE TEST      8/5/80

0117  02C1  18                    CLC
0118  02C2  A9 01                 LDA #01
0119  02C4  65 05                 ADC ERRS
0120  02C6  85 05                 STA ERRS
0121  02C8  A9 00                 LDA #00
0122  02CA  65 06                 ADC ERRS+1
0123  02CC  85 06                 STA ERRS+1
0124  02CE  D8                    CLD
0125  02CF  68                    PLA
0126  02D0  AA                    TAX
0127  02D1  4C 13 EA              JMP CRLOW

0129  02D4  20 46 EA    NUMBLK    JSR NUMA          ;PRINT BYTE THEN BLANK
0130  02D7  4C 3E E8              JMP BLANK

0132  02DA  20 E0 02    MSGCR     JSR MSG           ;PRINT MSG THEN CR
0133  02DD  4C 13 EA              JMP CRLOW

0135  02E0  BD FD 02    MSG       LDA MSG1,X
0136  02E3  48                    PHA
0137  02E4  29 7F                 AND #$7F
0138  02E6  20 7A E9              JSR OUTPUT
0139  02E9  E8                    INX
0140  02EA  68                    PLA
0141  02EB  10 F3                 BPL MSG
0142  02ED  60                    RTS

0144  02EE  AD 1C A4    SET       LDA ADDR          ;GET START LOW
0145  02F1  85 00                 STA AD1
0146  02F3  85 02                 STA AD2
0147  02F5  AD 1D A4              LDA ADDR+1        ;GET START HI
0148  02F8  85 01                 STA AD1+1
0149  02FA  85 03                 STA AD2+1
0150  02FC  60                    RTS

0152  02FD  4E 4F       MSG1     .BYT 'NO. OF RAM MODULES', $BF
0152  030F  BF
0153  0310  46 49       MSG2     .BYT 'FIRST ADDRESS', $BF
0153  031D  BF
0154  031E  20 45       MSG3     .BYT ' ERROR', $D3
0154  0324  D3
0155  0325  45 52       MSG4     .BYT 'ERROR LIS', $D4
0155  032E  D4
0156  032F  41 44                .BYT 'ADDR IS S', $C2
0156  0338  C2
0157  0339  FF          PAT      .BYT $FF, $AA, $55, $00
0157  033A  AA
0157  033B  55
0157  033C  00
0158  033D                       .END

ERRORS=0000 <0000>
```

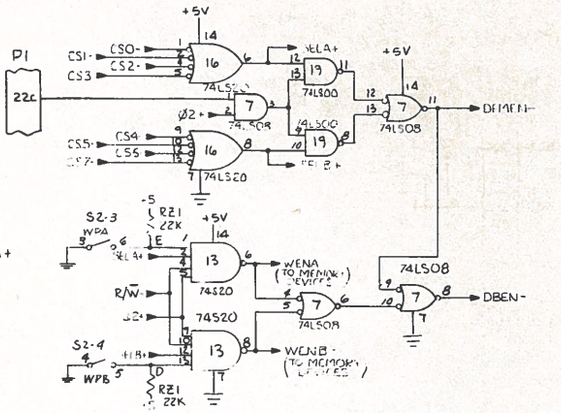
```
PAGE 0004                    8K STATIC RAM MODULE TEST        8/5/80

SYMBOL TABLE

AD1       0000   AD2       0002   ADDIN     EAAE   ADDR      A41C
ADDRGT    0226   BLANK     E83E   COMIN     E1A1   COMPAR    025D
CRLOW     EA13   END       0004   ERROR     0299   ERRS      0005
F1        0200   FLAG      0008   GSTORE    024B   IS        0009
MSG       02E0   MSG1      02FD   MSG2      0310   MSG3      031E
MSG4      0325   MSGCR     02DA   NEXT      0268   NOHD      02AC
NPAT      0246   NUMA      EA46   NUMBLK    02D4   OUTPUT    E97A
PAT       0339   REDOUT    E973   ROLL      0220   SB        0007
SET       02EE   STORE     0250
END OF ASSEMBLY
```











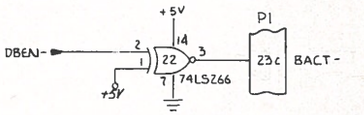
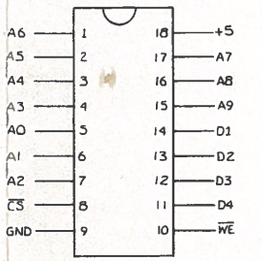


TABLE A - MEMORY DEVICE CONNECTIONS

REF. DES.	IC DEVICE PIN/FUNCTION 1 A6	2 A5	3 A4	4 A3	5 A0	6 A1	7 A2	8 $\overline{CS}$	9 GND	10 $\overline{WE}$	11 D4	12 D3	13 D2	14 D1	15 A9	16 A8	17 A7	18 VCC
Z3								CSØ-		WENA-	D3+	D2+	D1+	DO+				
Z6								CS1-										
Z9								CS2-										
Z12								CS3-		WENA-								
Z15								CS4-		WENB-								
Z18								CS5-										
Z21								CS6-										
Z24								CS7-		WENB-	D3+	D2+	D1+	DO+				
Z2								CSØ-		WENA-	D7+	D6+	D5+	D4+				
Z5								CS1-										
Z8								CS2-										
Z11								CS3-		WENA-								
Z14								CS4-		WENB-								
Z17								CS5-										
Z20								CS6-										
Z23								CS7-		WENB-	D7+	D6+	D5+	D4+				



TYPICAL OF DEVICE (2114)

NOTE: UNLESS OTHERWISE SPECIFIED

1. REF ASSY DWG PAIO-D100
2. PINS 3a,5c,8a,10c,13a,15c,18a,20c,23a,25c,28a,1A,B2C 30c SHALL BE CONNECTED TO GROUND
3. PINS 1c,32a ,ON EURO. CONN AND PINS Xa,Xc,Ya,Yc, 1c,32a ON U.S. CONNECTOR SHALL BE TIED TO +5V

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

DASH NO.	NEXT ASSY	USED ON
APPLICATION		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS .XX ± .03 .XXX ± .020 ANGLES ± 30'
MATERIAL
HEAT-TREAT
FINISH

AUTHORIZATION	
NO.	
DR BY	ANDERSON 11-13-79
CHK BY	
APPD BY	
APPD BY	

PART NO. ——

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