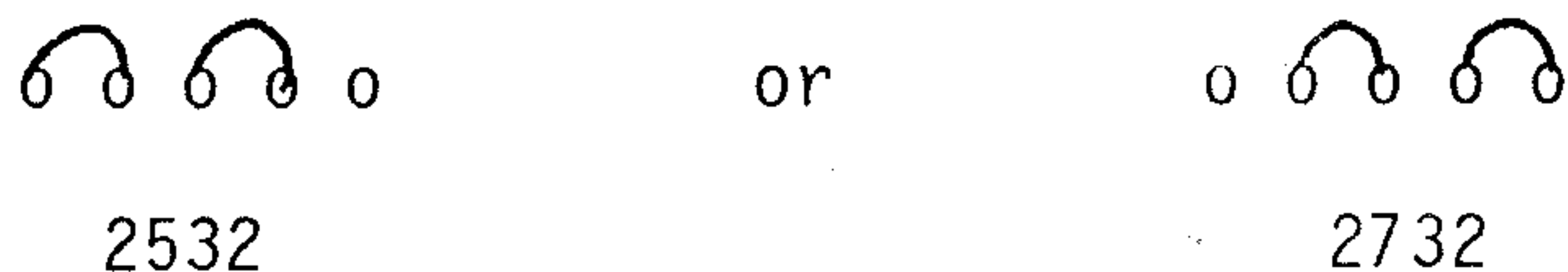


AIM 65 REVISIONS

1. PROM/ROM Sockets

Due to lack of availability of 2532 PROM devices, the 5 PROM/ROM sockets will be modified to accept 2732 PROMs as a jumper selectable option. This change will be implemented with a five node jumper for each PROM/ROM socket as indicated.



Note: The 2332 ROMs are pin-out compatible to the 2532 PROMs.

Because of the device situation, this modification must be made. Each socket may be configured independently of the others.

2. Clock Generation

To provide increased clock start up reliability across a range of power supplies, the crystal/oscillator circuit will be replaced with a 1 MHz hybrid clock oscillator.

3. RAM Memory

A change in the RAM memory design is planned to accomplish two goals: a) replace to old 2114 design and b) expand the RAM capacity. Using a different device as well as expanding the capacity, will affect how the memory address selection is made.

The modification will replace the eight 2114 RAM sockets with two 28-pin sockets. The first socket is for RAM only and will accept two different devices,

- a) 6264 or equivalent 28 pin, 8K byte static RAM, or
- b) 62256 or equivalent 28-pin, 32K byte static RAM.

Address assignments will also be jumper selectable in five ranges,

- a) no on-board memory.
- b) 4K selected on-board, \$0000 - \$0FFF, corresponding to the current AIM 65.

- c) 8K selected on-board, \$0000 - \$1FFF.
- d) 28K selected on-board, \$0000 - \$6FFF, with 32K byte device installed.
- e) 32K selected on-board, \$0000-\$7FFF, with 32K byte device installed.

The second socket will accept either an 8K byte RAM, 6264, or an 8K byte PROM, 2764. Jumpers are required to select the address ranges, which are:

- a) no on-board memory in this socket,
- b) 4K bytes selected, \$8000 - \$8FFF,
- c) 4K bytes selected, \$9000 - \$9FFF,
- d) 8K bytes selected, \$8000 - \$9FFF.

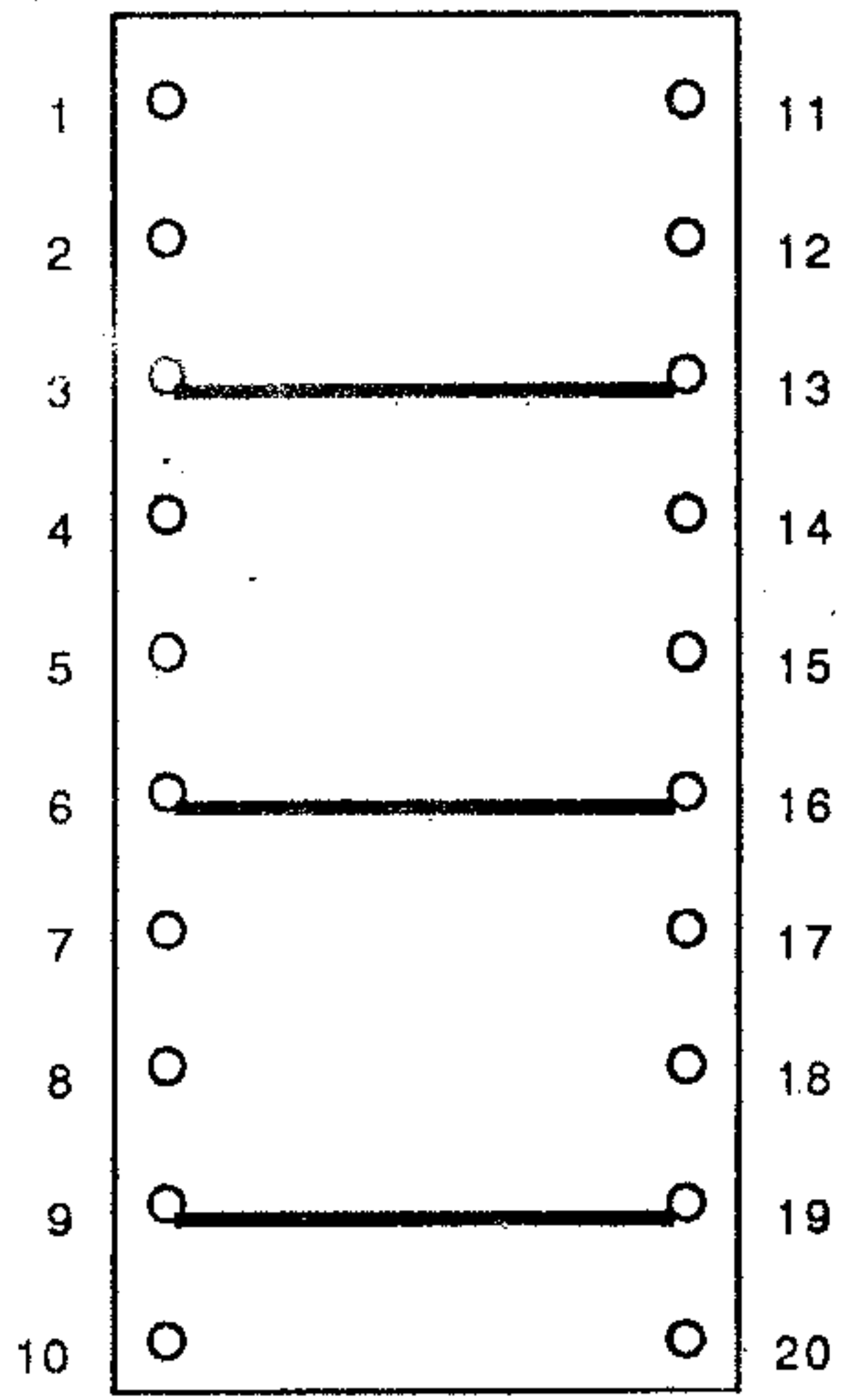
The figure on the following page illustrates how switch JB1 should be set to select the available memory ranges.

4. I/O Address Assignments

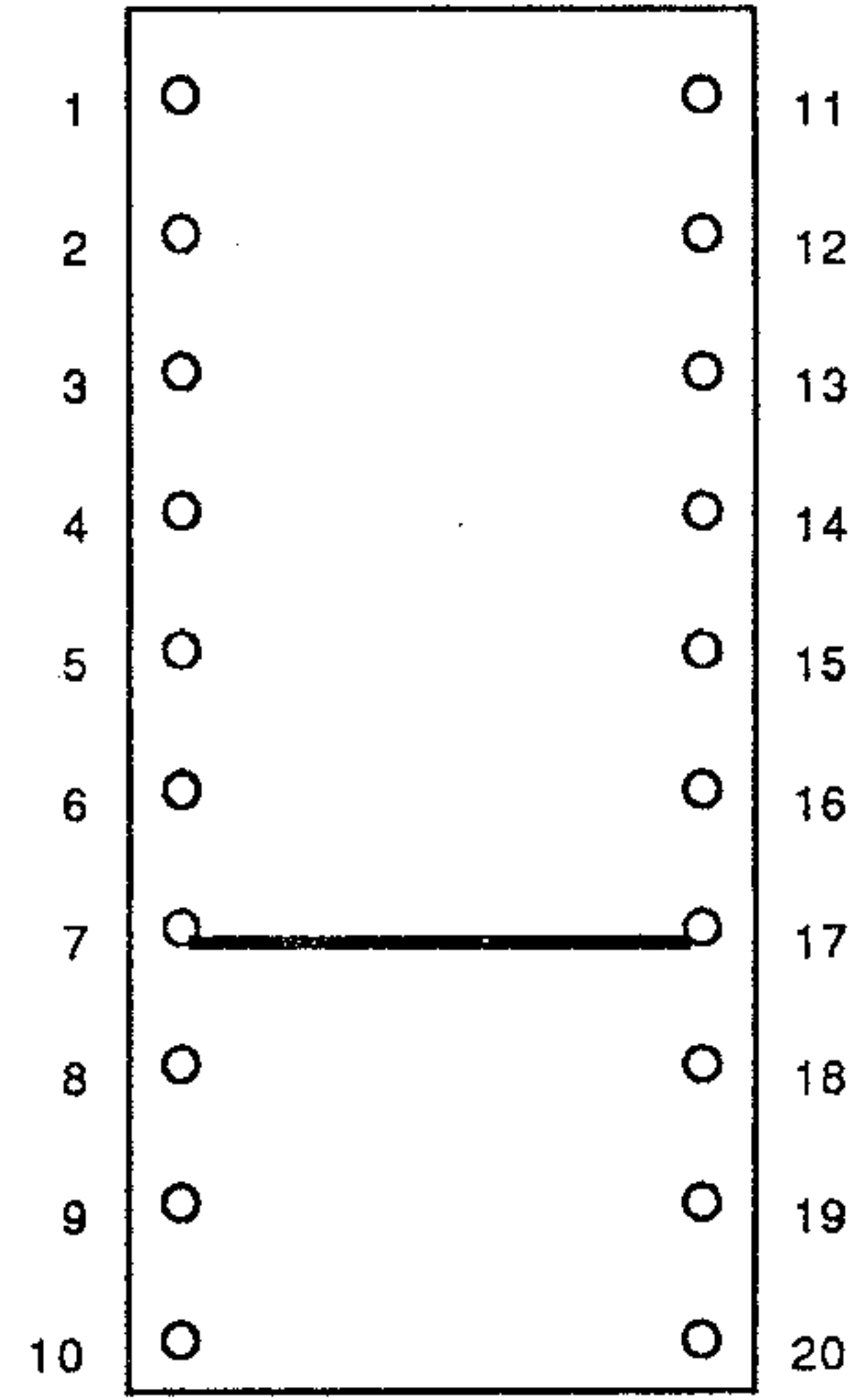
Finer decoding of I/O addresses will free up portions of the 4K byte address range, \$AXXX, for assignment of many of the add-on RM 65 I/O modules. The new decoding will be:

- a) User on-board 6522 address page, \$A000 - \$A0FF
- b) Available off-board pages, \$A100 - \$A3FF
- c) On-board 6532 RAM and I/O page, \$A400 - \$A4FF
- d) Available off-board pages, \$A500 - \$A7FF
- e) On-board system 6522 page, \$A800 - \$A8FF
- f) Available off-board pages, \$A900 - \$ABFF
- g) On-board display 6520 page, \$AC00 - \$ACFF
- h) Available off-board pages, \$AD00 - \$AFFF

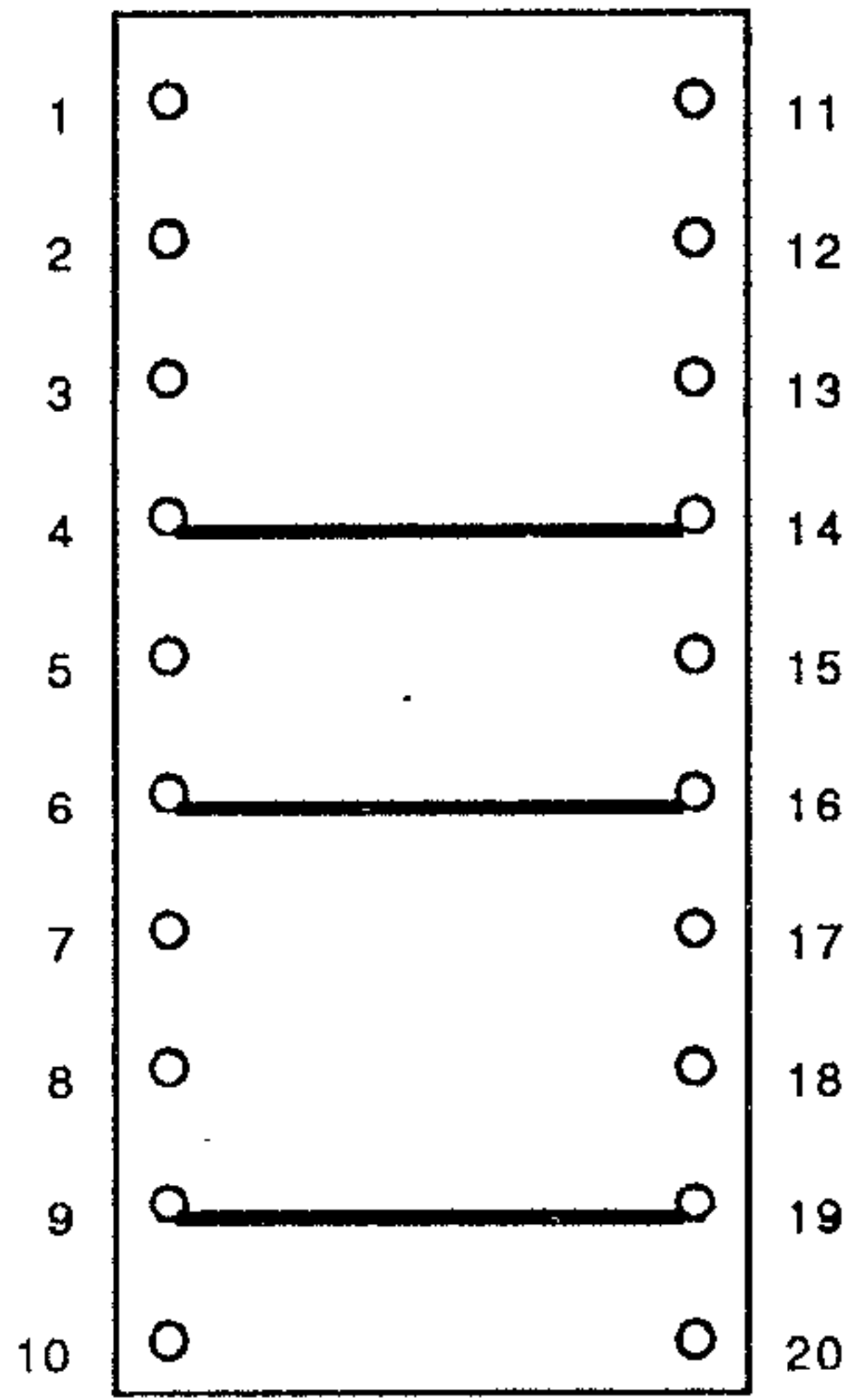
JB1 Setting For Expanded Memory



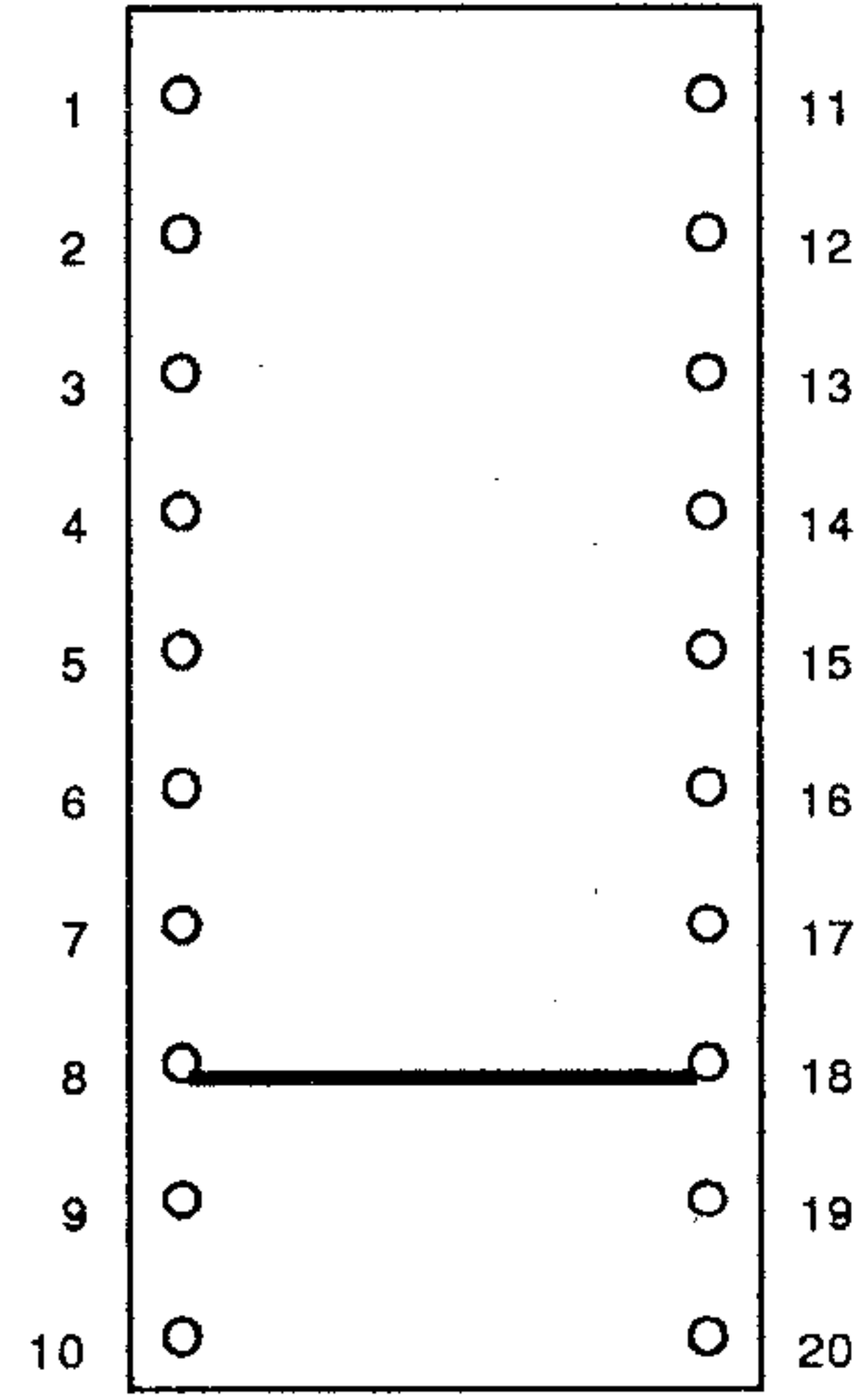
RAM 0-7FFF
Z3 is a 62256



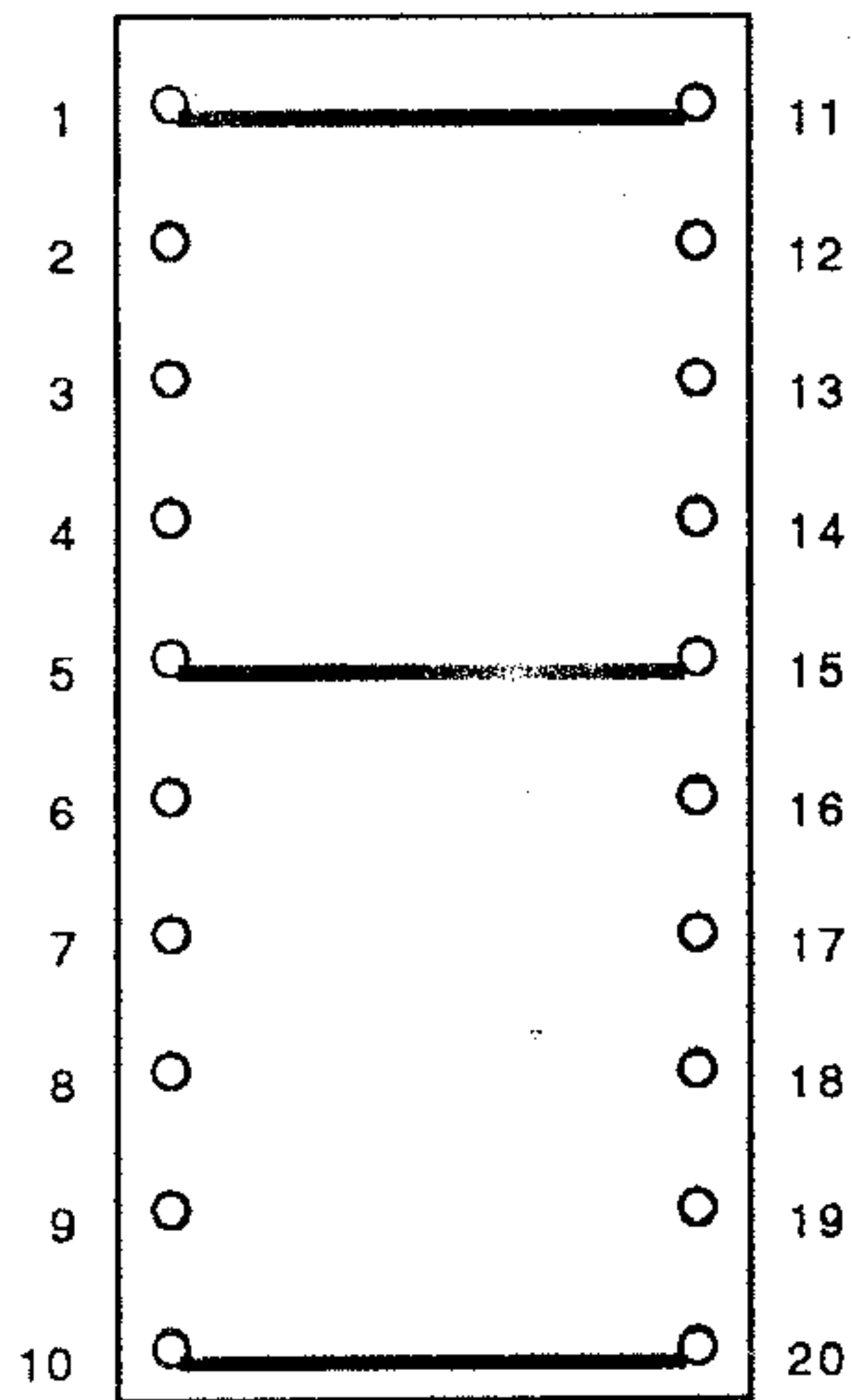
RAM/ROM 8000-8FFF
Z2 is a 6264 or a 2764



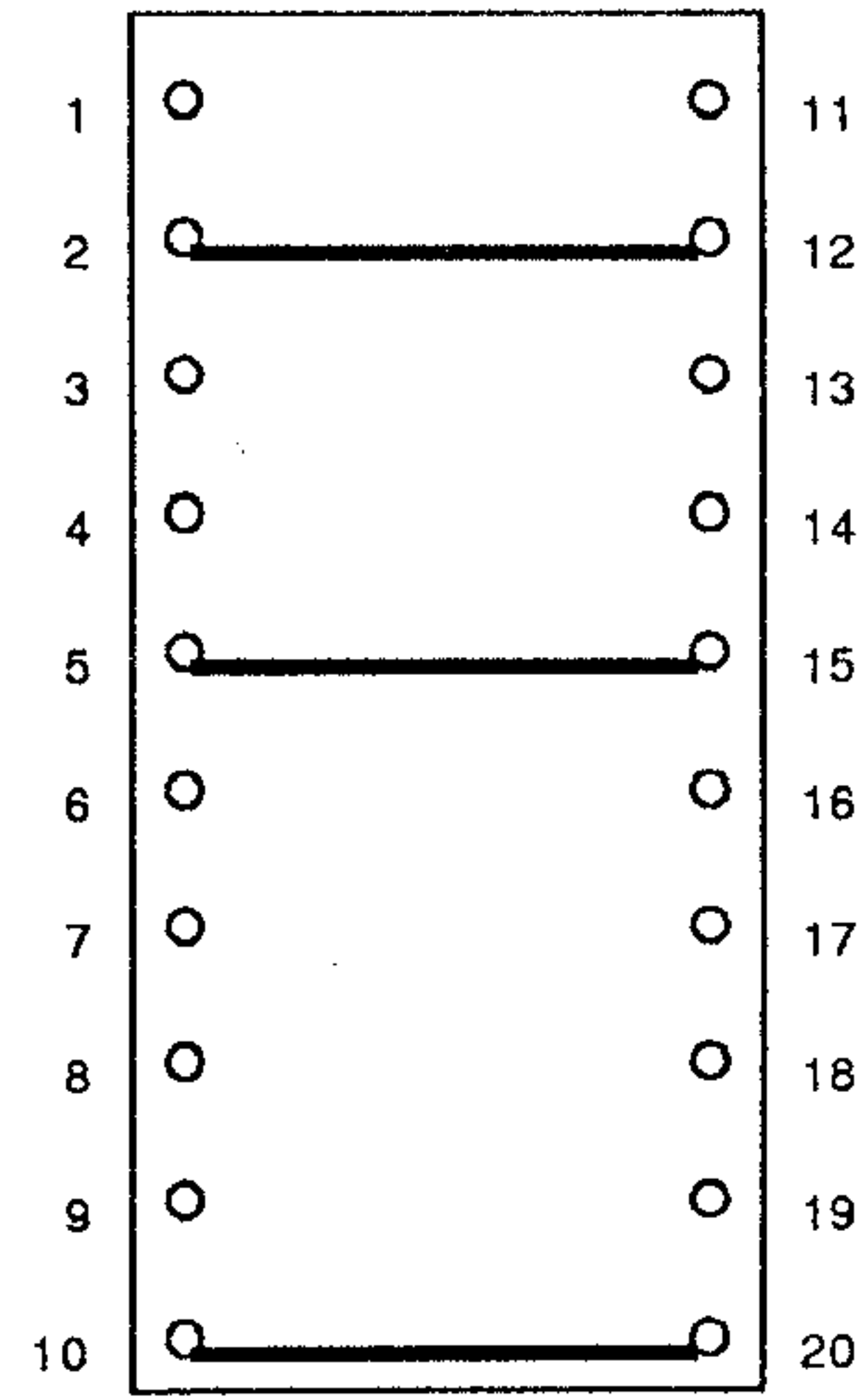
RAM 0-6FFF
Z3 is a 62256



RAM/ROM 9000-9FFF
Z2 is a 6264 or a 2764

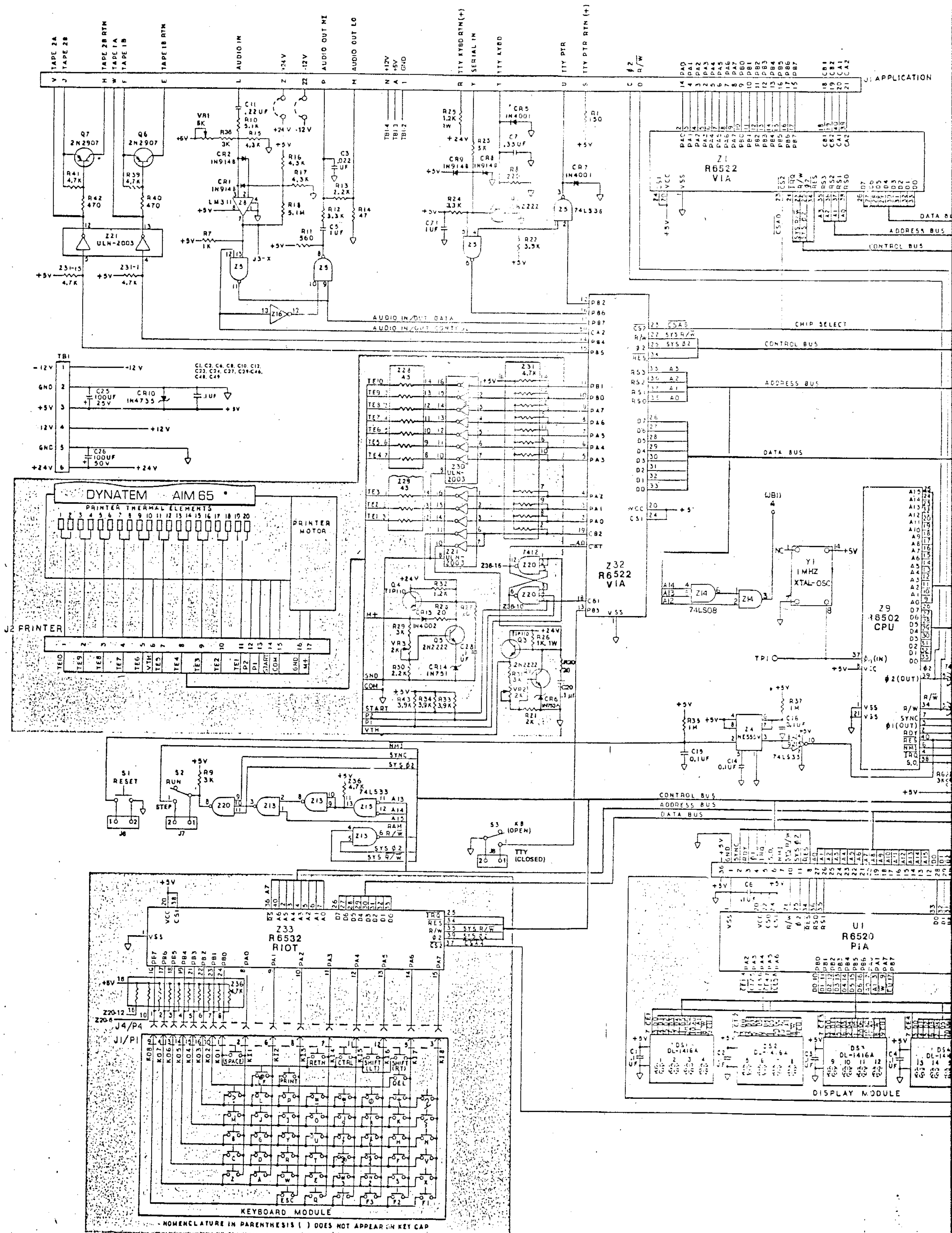


RAM 0-0FFF
Z3 is a 6264



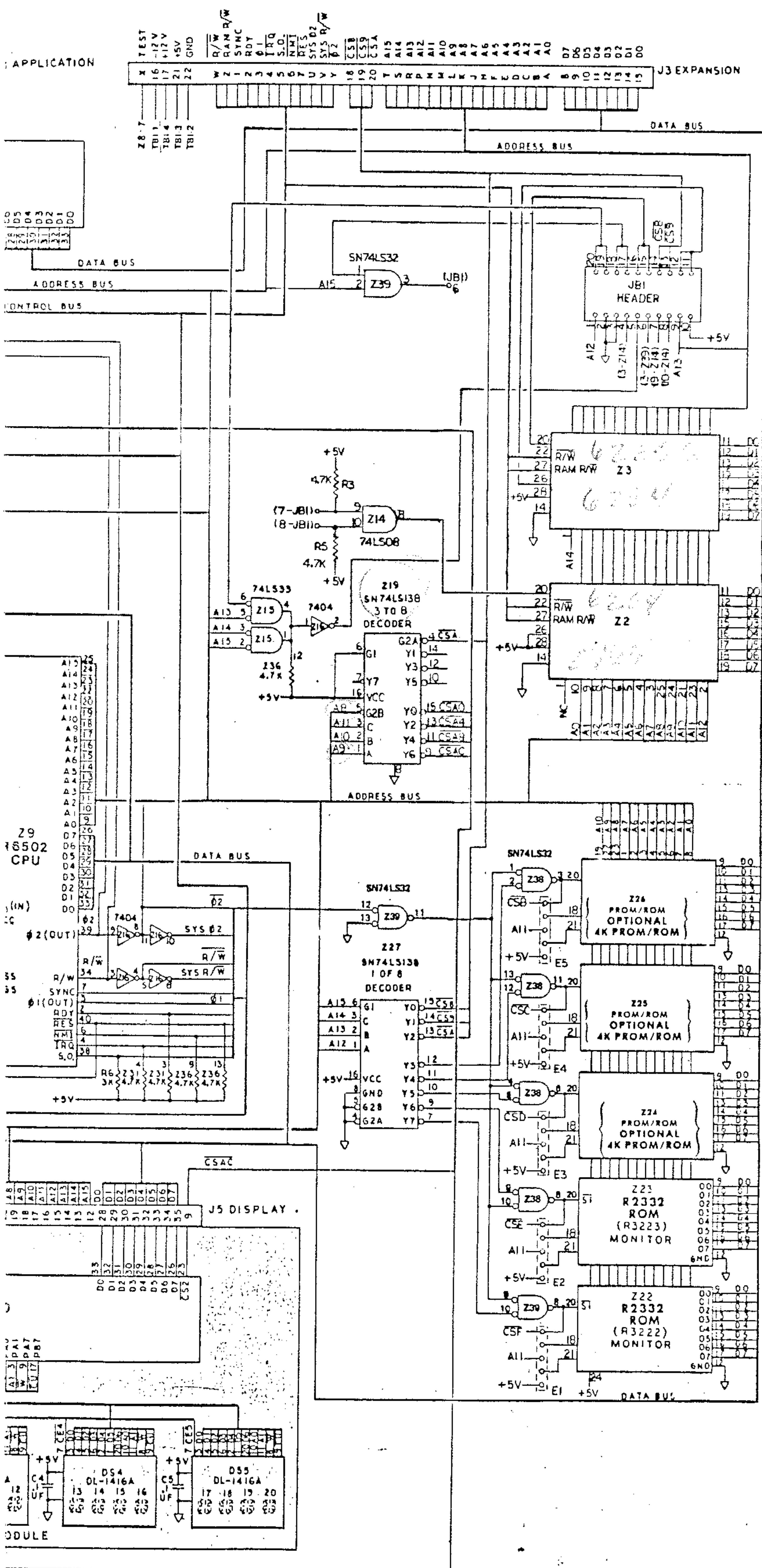
RAM 0-1FFF
Z3 is a 6264

DYNATEM AIM 65 Advanced Interactive M



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ve Microcomputer



*Crystal etc.
Y1 - 5.4433?*

*1100-1100 6400 use
1100-1100 Available
1100-1100 6400
1100-1100 Available
1100-1100 6400 use
1100-1100 Available
1100-1100 6400
1100-1100 Available
Z19 Y1, Y3, Y5, Y7 not used
74LS138 6400 use*