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Rockwell

R6500 Microcomputer System
APPLICATION NOTE

Interfacing R6500 Microprocessors To a Floppy Disk Controller

PURPOSE

Microprocessors in the R6500 family can operate with a wide variety of special-purpose peripheral controller devices. This Application Note describes the interface between an R6500 microprocessor and either of two Western Digital Floppy Disk Formatter/Controller devices, FDC 1781 and FDC 1791. The interface to the FDC 1781 requires a pair of one-shots, whereas the FDC 1791 can be interfaced directly. In both cases, the processor access time is one cycle.

DESCRIPTION

The basic interface for both Western Digital devices is shown in Figure 1. Data is passed between the R6500 microprocessor and the floppy disk controller on an 8-bit, bi-directional data bus. Address bus lines A0 and A1 select the FDC registers to be accessed. The remaining Address Bus lines, A2 through A15, can be used to generate a Chip Select signal ($\overline{CS}$) when the FDC has been addressed. The $\phi 2$ clock from the processor is used to generate strobes $\overline{RE}$ and $\overline{WE}$, for reading and writing the FDC registers.

TIMING

R6500 processors that run on a 1-MHz clock with 50-percent duty cycle will produce ϕ_2 clock up and down times (PHWϕ_2) of 470 ns minimum. Since the Western Digital FDC 1791 device requires Read and Write pulse widths ($\overline{RE}$ and $\overline{WE}$, respectively) of 400 ns, the ϕ_2 clock is adequate to generate these pulses directly. However, the FDC 1781 requires a minimum pulse width of 500 ns for both $\overline{RE}$ and $\overline{WE}$, so some additional strobe-generation circuitry must be included in that interface.

This circuitry is comprised of two one-shots, t_{W1} and t_{W2}, in which t_{W1} determines the start of the pulse and t_{W2} determines the width of the pulse. The limiting equation for t_{W1} is:

$$T_{ADS} + T_{ADD} + 50 < t_{W1} < 475 \text{ ns} \quad \text{(Equation 1)}$$

where T_{ADS} = Address Setup Time from R6500 (225 ns max)

T_{ADD} = Address Detect Delay Time

and the limiting equation for t_{W2} is:

$$500 \text{ ns} < t_{W2} < 1000 \text{ ns} - t_{W1} \quad \text{(Equation 2)}$$

A simple way to guarantee that the timing requirements are met is to make t_{W1} and t_{W2} approach their respective

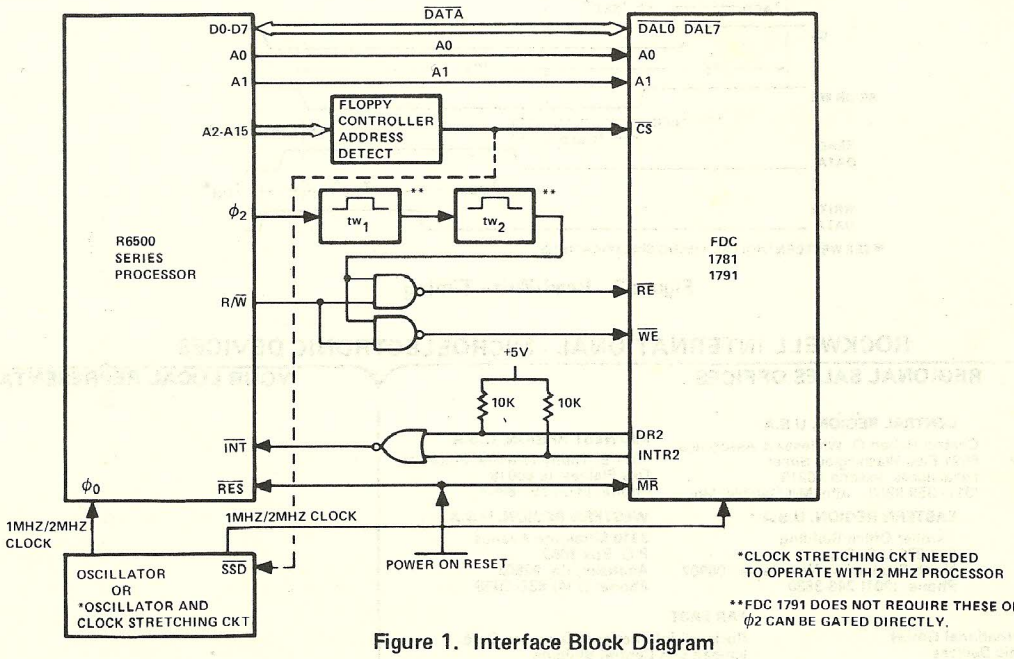

Figure 1. Interface Block Diagram