IO4

2 Parallel and 2 Serial I/O Board

Instruction Manual

USER'S MANUAL

104
2 Parallel and 2 Serial I/O Board

Instruction Manual

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CONTENTS

1.0 Introduction

1.1 General Description
1.2 Assembly Instructions

2.0 Functional Check

3.0 Set-up

3.1 Serial Interfaces
3.1.1 Internal switch set-up
3.1.2 Baud rate selection
3.1.3 Status word strap-up
3.1.4 Addressing
3.1.5 20ma/60ma Current loop strap-up
3.1.6 EIA interface strap-up

3.2 Parallel Interfaces
3.2.1 Simple parallel I/O
3.2.2 Status/Data configuration
3.2.3 Addressing

3.3 Interrupt Set-up

4.0 Applications

4.1 8251 Emulation of status
4.2 Altair Rev. 1 Interface
4.3 Altair Rev. 0 Interface
4.4 Processor Technology Interface
4.5 Imsai Interface
4.6 EIA RS232 Interconnection
4.7 Selectric Baud Rate
4.8 Serial-TTL Input/EIA Output
4.9 RS232 Interconnection-Busy, pin 4
4.10 RS232 Interconnection-Clear-to-Send, pin 5
4.11 Baud-rate for Poly Morphic System

5.0 Warranty

Assembly Drawing
Parts List
Schematic (INSERT)

1.0 INTRODUCTION

1.1 General Description

The SSM 10-4, 2P + 2S Interface board, is capable of meeting most small computer system I/O interface requirements. Its application is uncomplicated, requiring minimum software overhead.

The serial section is a dual port asynchronous serial interface, meeting both current loop and EIA level specifications. Interrupt capability is jumper selectable (header W4) for each receiver/transmitter pair independently. Status bit position is jumper selectable (header W1, W2) with bit sense reversable by changing U16, U18 which is a SN74367 (positive sensing) to a SN74368 for negative sensing. Data/Status port addresses for each serial interface are independently reversable (switch S1-PR, S2-PR). Parity odd/even, parity enable, number of stop bits, and word length are all selectable and are controlled by switches S1 & S2. The current loop interfaces will source or sink current for either 20ma or 60ma. Baud rates are jumper selectable (header W3) for the transmitter and receiver for each serial interface independently, covering most baud rates. The serial section is addressable as a four port address group starting on any four port boundary by switch S3.

The parallel section is a dual port (2 inputs & 2 outputs) parallel interface. Interrupt capability is jumper selectable (header W4) for each input port independently. +5Vdc and -12Vdc are available on each I/O socket. The parallel section is addressable as a two port address group starting on any two port boundary by switch S4.

Addressing of the serial and parallel sections are independent and exclusive; i.e., if both sections should be inadvertently addressed to the same position, neither section will be selected.

1.0 INTRODUCTION (continued)

1.2 Assembly Instructions (refer to assembly drawing)

- ☐ Check kit contents against parts list.
- ☐ Check PC board for possible warpage and straighten if required. To straighten the board, bend with the hands (not a vise) against the warp. Sight down the edge of the board after bending to check if the warp was removed, if not then try bending again.
- ☐ Remove the center pins (4 & 11) from 2-14 pin sockets and insert them in positions U2/U3 and U6/U7 with the pin 1 index toward the top of the board.
- ☐ Insert 20-14 pin (U4,5,15,17,20 thru 23,28,29,30,33,34, J1 thru J6). 14-16 pin (W1 thru W4,U16,18,19,24,25,26,31,32,35,36), 4-24 pin (U10 thru U13), & 2-40 pin (U8,9) sockets into the component side of the board with the pin 1 index toward the top or left of the board. (On the component side "Solid State Music" is printed.) DON'T SOLDER! NOTE: Switches do not use sockets.
- ☐ Place a flat piece of stiff cardboard of appropriate size on top of the sockets to hold them in place.
- ☐ Holding the cardboard in place against the sockets, turn the board over and lay it on a flat surface. (Be sure that all of the sockets pins are through the holes.)

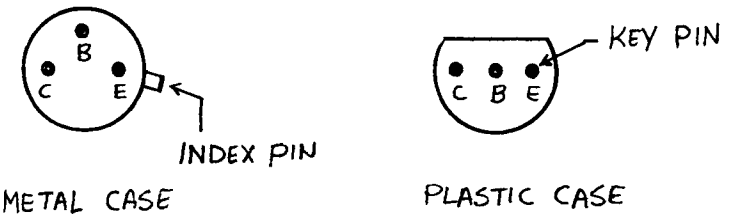
  NOTE: Keep soldering iron tip clean to prevent rosin and sludge from being deposited on traces. Wipe tip frequently on a damp cloth or sponge.
- ☐ On each socket, solder two of the corner pins, choosing two that are diagonally opposite of each other.
- ☐ Once the sockets are secured, lift the board and check to see if they are flat against the board. If not, seat the sockets by pressing on top while reheating each soldered pin.
- ☐ Complete soldering the remaining pins of each socket. Touch pin and pad with soldering-iron tip, allowing enough solder to flow to form a filet between pin and pad. Keep the tip against the pin and pad just long enough to produce the filet. Too much heat can cause separation of pad and trace from the board. A 600 degree iron tip is recommended.
- ☐ Insert and solder 27 ¼W resistors in their respective locations (refer to Assy. Dwg.). DO NOT install R6 or R12 (47ohm) at this time.
- ☐ Insert and solder 2 SIP resistor packs (R15.18) with the index marks toward the top of the board.

1.2 Assembly Instructions (continued)

☐ Observing polarity, insert and solder diodes D1 thru D4 in their respective locations.

☐ Align emitter to index mark and insert & solder each of 4 transistors. (Q1,2,3,4).

TOP VIEW (X-RAY VIEW)



METAL CASE PLASTIC CASE

☐ Observing polarity, insert and solder 7 tantalum capacitors (C1,3,4, 9,10,11,12).

☐ Insert and solder 5-0.1uf ceramic capacitors (C2,5,6,7,8).

☐ Insert and solder 4 DIP switches with the OPEN position toward the right of the board. (The numbered side of the switch to the left.)

☐ Place regulators on the board so the mounting hole in the regulator is in line with the hole in the board. Mark leads for proper bending position to match the board holes--allow for a bend radius.

☐ Bend regulator leads to match holes in board.

If available, apply thermal compound to the back side of each regulator case (the part that lies flat against the board).

☐ Position 2 heatsinks (for U1 & U37), drop 4 regulators in place on front of board, insert #6 screws from behind and secure firmly with lock washers and nuts.

☐ Solder regulator leads to pads on back of board. Do not use excessive heat.

2.0 FUNCTIONAL CHECK

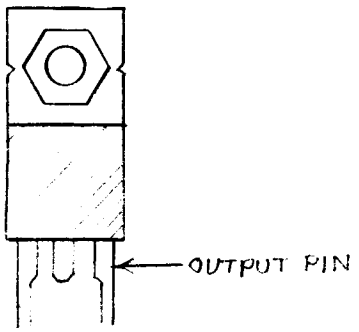
WARNING! DO NOT INSTALL OR REMOVE BOARD WITH POWER ON. DAMAGE TO THIS AND OTHER BOARDS COULD OCCUR.

2.1 If an ohmmeter is available, measure the resistance between the following pins:

Negative Probe		Positive Probe	Resistance
Bus pin 50	to	Bus pin 1	greater than 20
Bus pin 50	to	Bus pin 2	greater than 20
Bus pin 52	to	Bus pin 50	greater than 30

If your reading is below these values check for electrical shorts on your card.

2.2 Apply power (+8v to +10v) to board by plugging into computer or by connection to a suitable power supply. Measure the outputs of the +5V regulators.



The voltage should be between +4.8v and +5.2v at U1 & U37. If the regulator doesn't meet this test, then check the board for shorts or errors.

CAUTION: WHILE IT HAS NEVER HAPPENED TO US, SHORTED REGULATORS HAVE BEEN KNOWN TO EXPLODE WITH POSSIBLE INJURY TO EYES OR HANDS. BETTER SAFE THAN SORRY--KEEP FACE AND HANDS CLEAR OF THE REGULATOR SIDE OF THE BOARD DURING THIS AND SUBSEQUENT TESTS!

2.3 Apply power (+16 volts) to the board by plugging into computer or by connection to a suitable power supply. Verify that the output of the +12V regulator (U27) is between +11.5 & +12.5 Vdc.

2.4 Apply power (-16 volts) to the board by plugging into computer or by connection to a suitable power supply. Verify that the output of the -12V regulator (U14) is between -11.5 & -12.5Vdc.

2.5 Now look the board over carefully. Check for poor solder joints or bridges. Using the component layout drawing, look for improper part locations or polarity. A few minutes of careful inspection may save a few hours of troubleshooting.

2.6 Observing polarity, insert chips into their sockets as per assembly drawing.

3.0 SET-UP

3.1 Serial Interfaces

3.1.1 Internal switch set-up

The Universal Asynchronous Receiver Transmitter (UART) is internally controlled by switch S2 for serial A and S1 for Serial B. The switch functions are as follows:

Parity Control	Serial B	Serial A
A. No Parity Bit (NPB) Turn switch *off for no parity bit. (Most common setting of the switch is off.) (*"Off" may be labeled on the switch as "open", also "on" may be called "closed".)	S1-NPB	S2-NPB =OFF
B. Parity Odd or Even (POE) Turn switch on for odd parity. Turn switch off for even parity.	S1-POE	S2-POE (DON'T CARE)

Word Length

A. Number of Data Bits (NDB)
The number of data bits in the serial word can be controlled by S1-3,4 and S2-3,4 (NDB1,NDB2).

Number of Bits	NDB1	NDB2	
5	ON	ON	
6	OFF	ON	
7	ON	OFF	
8	OFF	OFF	(most typical number of bits)

B. Number of Stop Bits (NSB)
The number of stop bits at the end of a serial word can be controlled by S1-NSB and S2-NSB.

1 Stop bits = switch NSB set to ON. (300 Baud & up)
1.5 Stop bits = switch NSB set to OFF. (Word length =5)
2 Stop bits = switch NSB set to OFF. (Most typical)

Port Reversal (PR)

The Status and Data port addresses can be exchanged (reversed) for matching most of the Status/Data port configurations by using S1-PR and S2-PR.

A*. Status first, data port last with switch OFF.
B**. Data first, status port last with switch ON.

*Most common with MITS, Processor Technology, etc. software.
**Most common with IMSAI software.

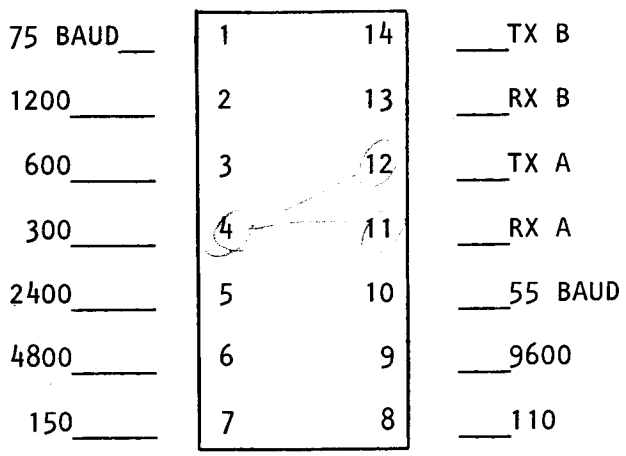
3.1.2 Baud Rate Selection

The baud rate divider is capable of supplying any of the ten most common baud rates to each of the UART's receiver and transmitter clock lines independently. The clock frequency is 16 times the baud rate coming from header W3. To set the serial interface's baud rate, run a wire from the pin on W3 with the desired frequency over to pins TX and RX of the UART being used.

Baud Rate	Clock Frequency	Header Pin Number	% Error
55	874Hz	10	-.68%
75	1.202KHz	1	+.16%
110	1.748KHz	8	-.68%
150	2.404KHz	7	+.16%
300	4.807KHz	4	+.16%
600	9.615KHz	3	+.16%
1200	19.231KHz	2	+.16%
2400	38.461KHz	5	+.16%
4800	76.973KHz	6	+.16%
9600	153.846KHz	9	+.16%

UART Function	Header Pin No.
Receiver (RX) A	11
Transmitter (TX) A	12
Receiver (RX) B	13
Transmitter (TX) B	14

W3
BAUD RATE HEADER



3.1.3 Status Word Strap-Up

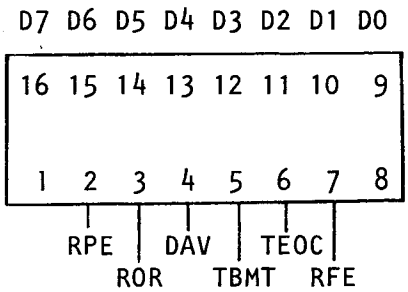
The status word (6 bits) is strapable on header W2 for Serial A and W1 for Serial B into any exclusive positive or negative logic pattern as required. Logic sense is determined by U18 for Serial A and U16 for Serial B. The sense polarity is active high for a 74367, or active low for a 74368 at U16 or U18. The wanted status signal is jumpered over on W1 or W2 to the wanted data bit from D0 to D7 on a header.

Output Status	Pin No. (W1,W2)
Output Data Available (Dav) or (ODA)	4
Receiver Over Run (ROR)	3
Receiver Parity Error (RPE)	2
Receiver Framing Error (RFE)	7
Transmitter End of Character (TEOC)	6
Transmitter Buffer Empty (TBMT)	5

Data Lines	Pin No. (W1,W2)
Data Bus D0	9
Data Bus D1	10
Data Bus D2	11
Data Bus D3	12
Data Bus D4	13
Data Bus D5	14
Data Bus D6	15
Data Bus D7	16

W1 (SERIAL B)
W2 (SERIAL A)

STATUS WORD HEADER



3.1.4 Addressing

The IO-4 serial and parallel sections are addressable independently and exclusively. If an overlay does occur, Nothing will be active in the area of contention.

3.1.4 Addressing (Continued)

The serial section is addressable to any consecutive four port block increment beginning on any four port block boundary. A typical four port block would be addressing ports 0 thru 3 by setting all positions of S3 closed (on). The status ports would be at port 0 & 2, and Data ports at 1 & 3 for serial interfaces A & B. Data and Status ports may be reversed independently of the other port pair.

Serial Addressing Examples

Switch is S3. S3 is set-up for a 6 bit binary address code.

	S3 Switch					
Addresses	A7	A6	A5	A4	A3	A2
*0 thru 3	on	on	on	on	on	on
4 thru 7	on	on	on	on	on	off
8 thru B	on	on	on	on	off	on
→ C thru F	on	on	on	on	off	off
-						
-						
20 thru 23	on	on	off	on	on	on
-						
E0 thru E3	off	off	off	on	off	off
F0 thru F3	off	off	off	off	on	on
F4 thru F7	off	off	off	off	on	off
F8 thru FB	off	off	off	off	off	on
FC thru FF	off	off	off	off	off	off

*(0,1 = Serial A); (2,3 = Serial B)

3.1.5 20mA/60mA Current Loop Strap-up

The IO-4 board is equipped with optical isolators for both the sending and receiving of serial data for a 20 or 60mA current loop interface. The optical isolators will respond to baud rates up to 12ØØ.

Serial Input Card

Make the following connections to J1 or J2:

20mA Loop

1. Connect pin 3 to pin 6 (for using internal -12V)
2. Remove R6 for serial B, or R12 for serial A.
3. Pins 2 & 7 are input signal pins to be connected to the current loop device. Pin 7 is ground.

60mA Loop

1. Connect an external 180ohm, 1 watt resistor between pins 3 and 4.
2. Insert resistor R6 for Serial B, or R12 for Serial A.

3.1.5 20mA/60mA Current Loop Strap-up (continued)

3. Pins 2 & 7 are input signal pins to be connected to the current loop device. Pin 7 is ground.

Serial Output from the card

Make the following connections to J1 or J2:

20mA Loop

1. Connect pin 5 to pin 12 (for using internal +12V).
2. Pins 10 & 8 are the output signal pins to be connected to the current loop device. Pin 8 is ground.

60mA Loop

1. Connect pin 5 through an external 180 ohm, 1 watt resistor to pin 9.
2. Pins 10 & 8 are the output signal pins to be connected to the current loop device. Pin 8 is ground.

3.1.6 EIA Interface Strap-up

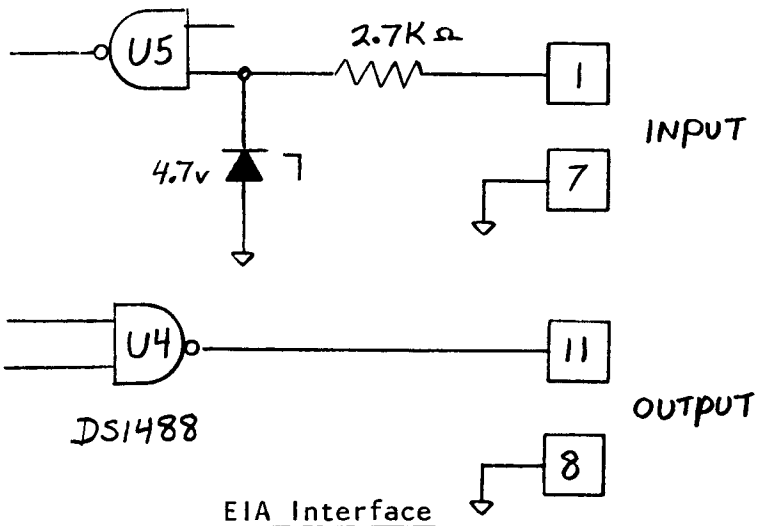
The 10-4 is equipped with an EIA interface for providing RS-232 compatible signals. The input impedance is about 2.7k ohms, and the output drive provided by U4 (DS1488) is about ±10 volts

Serial Input to Card

Pin 1 is the input pin for both J1 & J2. Pin 7 is the ground connection point for the input signal.

Serial Output From The Card

Pin 11 is the output pin for both J1 & J2. Pin 8 is the ground connection.



EIA Interface

3.2 Parallel Interfaces

3.2.1 Simple Parallel I/O

The parallel interface on the IO-4 uses an 8212 which is an 8-bit latch with a service request flip-flop.

Parallel Inputs

The parallel input ports J4 & J6 are loaded by using the strobe line (J4-1, J6-1). If the strobe line is high, data will pass into the 8212. When the strobe line goes low the previous data is latched into the 8212. The parallel input port can be used for sampling an 8-bit input signal by pulsing the strobe line positive (similar to data-available strobe).

The service request flip-flop is set so the $\overline{\text{INT}}$ signal line goes low (J4-2,J6-2) on the falling edge of the postive strobe pulse. When the CPU reads the parallel input port's data the service request flip-flop signal goes high (similar to an acknowledge signal).

Parallel Outputs

The parallel output ports J3 & J5 are like the input ports, except the input/output lines are switched. The service request flip-flop is still controlled by the strobe line and CPU, but the data is latched in under CPU control instead of strobe.

3.2.2 Status/Data Configuration

Parallel I/O-A can be set aside as a Status/Control port with parallel I/O-B the Data I/O port. This concept is used in most of the 8080 software written, but the selected status bits and polarity of status changes from company to company.

Example:

A. Parallel I/O-A will be the Status port.
B. Parallel I/O-B will be the Data port.
C. Data-available flag bit will be D0 going low.

Connections

1. Connect J4 pin 2 to J6 pin 9. ($\overline{\text{DAV}}$ bit)
2. Connect J6 pin 1 to J6 pin 14. (strobe=1)
3. Data must be strobed into J4 with a positive pulse on pin 1.

3.2.3 Addressing

The IO-4 Serial and Parallel sections are addressable independently and exclusively. If an overlay does occur between sections, NOTHING will be active in the area of contention.

The parallel section is addressable to any consecutive two port block increment beginning on any two port block boundary. A typical two port block would be addressing ports 0 thru 1 by setting all positions of S4 closed (on).

Parallel Addressing Examples

Switch is S4. S4 is set-up for a 7 bit binary address code.

	S4 Switch						
Addresses	A7	A6	A5	A4	A3	A2	A1
*0 & 1	on	on	on	on	on	on	on
2 & 3	on	on	on	on	on	on	off
4 & 5	on	on	on	on	on	off	on
6 & 7	on	on	on	on	on	off	off
8 & 9	on	on	on	on	off	on	on
-							
-							
FC & FD	off	off	off	off	off	off	on
FE & FF	off	off	off	off	off	off	off

*(0 = parallel A); (1= parallel B)

Port J5/J6 is the first port addressed at the setting of S4 and J3/J4 is the second port addressed (S4's setting plus one).

3.3 Interrupt Set-Up

Multiple interrupts can be generated by either the serial or parallel ports. The conditions for this are as follows:

Parallel Input Interrupt

Parallel input port A or B can generate a $\overline{INT}$ when data, comming in from an external circuit, strobes the 8212 (pin 1). The port which was strobed does not have to be selected by the system to generate an interrupt. The $\overline{INT}$ signals are sent to the interrupt header W4.

Serial Input Interrupt

Serial Input Interrupt is generated when Serial A or Serial B port receives a new character from the outside. DAV goes high (logic one) at this time, and by so doing generates an interrupt signal. The interrupt signal is inverted to the correct polarity by U28 and sent to header W4.

Serial Control Lines

Multiple port interrupts can be connected to either an 8 level priorty system card or brought out in parallel using a polling system through one of the IO-4's parallel input ports.

3.3 Interrupt Set-Up (continued)

Interrupt Examples:

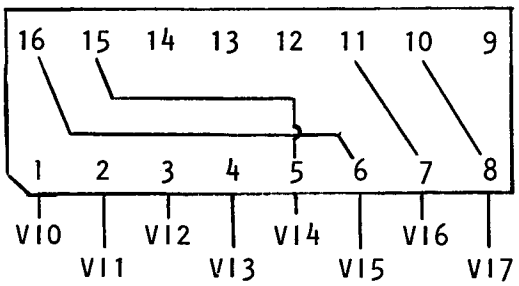
A. To an 8 level priority through the W4 header:

1. Ports A & B will interrupt the system with B having the highest priority.

2. Priority stack:

1st	Parallel input port B
2nd	Parallel input port A
3rd	Serial input port B
4th	Serial input port A

INTERRUPT HEADER

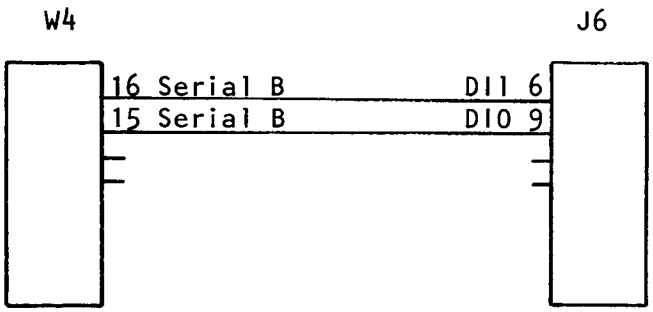


B. To a polling system through Parallel port A:

1. Connect J6 pin 1 to J6 pin 14 (strobe = 1)

2. Only Serial ports A & B will be polled:

3. DAV signals from W4 connected to inputs of J6.



4.0 Applications

4.1 8251 Emulation of Status

The serial interfaces A & B can be set up to emulate status bits in the same order as an 8251 (Asynchronous mode only) by strapping up header W2 or W1 as follows:

UART Status	Pin	Connect to	Data Bit	Pin
TBMT	5		D0	9
DAV	4		D1	10
TEOC	6		D2	11
RPE	2		D3	12
ROR	3		D4	13
RFE	7		D5	14

4.2 Altair Rev. 1

Serial Interface

Serial interfaces A & B can be set up to give the same data-available and data-acknowledge status bits as the Altair Rev. 1 I/O configuration.

1. Change U18 for Serial A, or U16 for Serial B to a 74 (LS)368 to invert the status signals.

2. Make the following connections on W2 for Serial A or W1 for Serial B:

UART Status	Pin	Connect to	Data Bit	Pin
DAV	4		D0	9
TBMT	5		D7	16

3. If the serial port is to be the main console port, then set the address switch S3-Serial to all closed (on) in order to address the serial data ports plus status at 0 thru 3. The main console port will be at ports 0 & 1.

Parallel Interface

The two parallel ports can be arranged into Status/Data configuration to simulate an Altair Rev. 1 I/O configuration.

1. Connect J4 pin 2 to J6 pin 9. ($\overline{\text{DAV}}$ bit)
2. Connect J6 pin 1 to J6 pin 14. (Strobe = 1)
3. Data must be strobed into J4 (connected to U11) with a positive pulse on pin 1 with a width of about 0.5 to 10 microseconds.
4. Data-acknowledge signal from the printing device should be a low-going signal ($\overline{\text{DAK}}$) connected to J6 pin 3.
5. If the Parallel port is to be the main console port, then set the address switch S4-Parallel to all closed (on) in order to address the parallel ports at 0 & 1.

4.3 Altair Rev. 0 Interface

Serial Interface

To simulate the status bits of an Altair Rev. 0 interface on the serial interfaces, make the following connections:

1. Strap-up header W2 for Serial A or W1 for Serial B.

UART Status	Pin	Connect to	Data Bit	Pin
DAV	4		D5	14
TBMT	5		D1	10

2. If the serial port is to be the main console port, then set the address switch S3-Serial to all closed (on) in order to address the serial data ports plus status at 0 thru 3. The main console port will be Serial A at ports 0 & 1.

4.4 Process or Technology Interface

Serial Interface

To simulate the status bits of a Processor Technology interface on the serial interfaces, make the following connections:

1. Strap-up header W2 for Serial A or W1 for Serial B.

UART Status	Pin	Connect to	Data Bit	Pin
DAV	4		D6	15
TBMT	5		D7	16

2. If the serial port is to be the main console port, then set the address switch S3-Serial to ALL closed (on) in order to address the serial data ports plus status at 0 thru 3. The main console port will be Serial A at ports 0 & 3.

4.5 IMSAI Interface

Serial Interface

To simulate the status bits of an IMSAI interface on the serial interfaces, make the following connections:

1. Strap-up header W2 for Serial A or W1 for Serial B.

UART Status	Pin	Connect to	Data Bit	Pin
DAV	4		D1	10
TBMT	5		D0	9

2. Set switch S2 for Serial A or S1-PR for Serial B to the closed (on) position. This switch will reverse the status and data port addresses to match IMSAI's.

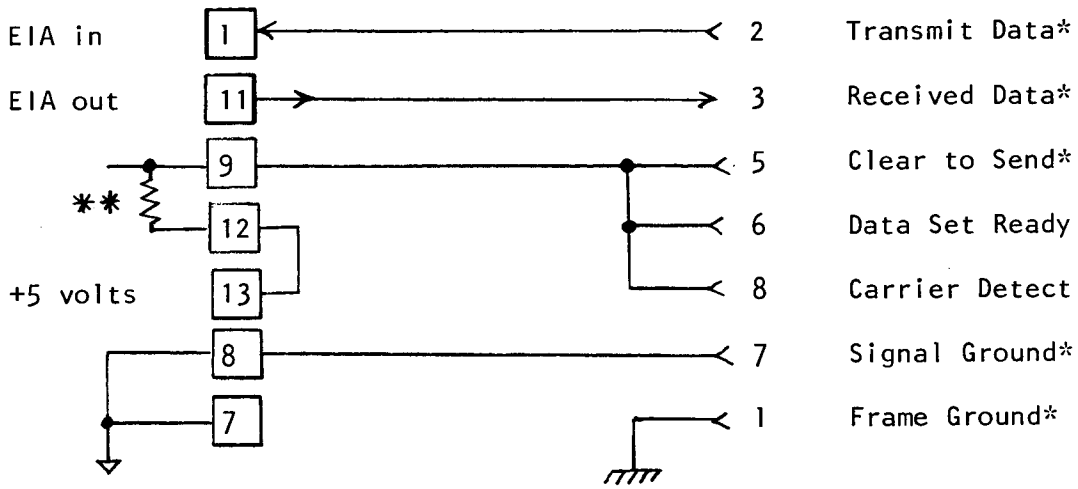
4.5 IMSAI Interface (Continued)

3. If the serial port is to be the main console port, then set the address switches S3-Serial to ALL closed (on) in order to address the serial ports plus status at 0 thru 3. The main console port will be Serial B at ports 2 & 3.

4.6 EIA RS232 Interconnection

The IO-4 is equipped with EIA interface circuitry. To set up board to drive a RS232 interface, the most common interconnection would be as follows:

(Interconnection submitted by Lynn E. Cochran)



* Signals used by Dura, Artec, Itel

** Using part of the current loop circuitry to act as a pull-up resistor on EIA pins 5, 6 & 8. The current loop interface cannot be used, if pin 9 is used as a pull-up. An alternate method is to drive pins 5, 6 & 8 of the EIA socket with three 1K ohm resistors off of pin 12 (+5v), then the current loop interface can be used at the same time.

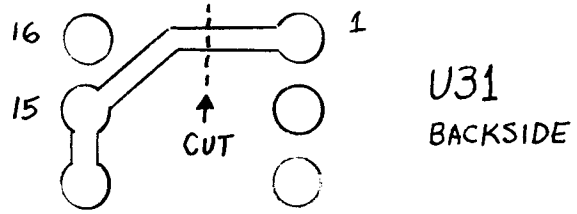
4.7 Selectric Baud Rate

The IO-4 was designed to generate ten different Baud rates to meet most serial interface applications, but the Selectric uses 134.5 which is not generated on this card. If you will not be using 100 & 55 Baud, then 110 can be increased to 133.5 Baud. (only 1% error)

For 133.5 Baud on W3, pin 8:

4.7 Selectric Baud Rate (continued)

1. Cut the trace between U31, pin 1 and pin 15.



2. Measure continuity between U31, pin 1 and pin 15 and verify that resistance is greater 100K ohm (greater than 500ohm with part inserted). Clean or scribe between pin 15 & pin 1, if necessary.

3. Connect U31, pin 1 to U31 pin 4.

4.8 Serial-TTL Input/EIA Output

If you are dealing with a Serial Terminal which cannot generate an EIA drive signal to the 104, but can receive a EIA signal from 104, then the serial input can be modified for TTL levels. This modification is needed, if you are driving a Xitex Video Card.

(Serial input modification submitted by J. Schrabal, 12-1-78.)

(1) Add a jumper-wire across R13, if you are using Serial-A for this application.

(2) Add a jumper-wire across R7, if you are using Serial-B for this application.

Make sure these jumpers are removed whenever a standard RS-232 interfacing device is connected, or you will damage U5, pins 5 & 9.

4.9 RS232 Interconnection--Busy, pin 4.
(Current-loop interface is disabled)

A "buffer-full" or "Printer-busy" detector can be added to the 104 for high speed printers. The following modification was used to interface the heath kit WH14 printer which has a "Busy" signal on pin 4. This busy signal goes high (>+3 volts) if the printer's buffer is almost full.

The interconnection that will be described is for Serial-A on the 104, but can be duplicated for Serial B in a similar manner.

(Circuitry tested by C. Aldridge of Tennessee, March, 1979)

4.9 RS232 Interconnection--Busy, pin 4. (continued)

Add a SN74LS00 IC (UX) to one of the two spare socket patterns at the bottom of the 104. Use an IC scoket.

A. Connect UX, pin 14 to +5 volts(U30,pin 14 orU31, pin 16).

B. Connect UX, pin 7 to ground (U30, pin 7 or U31, pin 8).

C. Connect UX, pin 3 to UX, pin 4.

D. Connect UX, pin 4 to UX, pin 5.

E. Cut one trace that runs on the front of the board horizontally between U18 & U9. This trace runs accross between pins 18 & 19 of U9. (This should be the trace that connects the UART (U9, pin 22) to a tri-state driver (U18, pin 6)).

F. Connect UX, pin 6 to U18 pin 6.

G. Connect UX, pin 1 to U9, pin 22.

Now a resistor-zener network will be added to the 104 for a EIA to TTL level shifter as follows:

H. Remove the input optical-isolator (U7).

I. Make R12 a 2.7K ohm, $\frac{1}{4}$w resistor.

J. Place a 3.3 volt up to a 4.7 volt zener diode (IN748, IN749, IN750, IN5228, IN5229 or IN5230 can be used.) into the U7 socket. The banded end (cathode) should be in U7, pin 1 the other end will go to U7, pin 4.

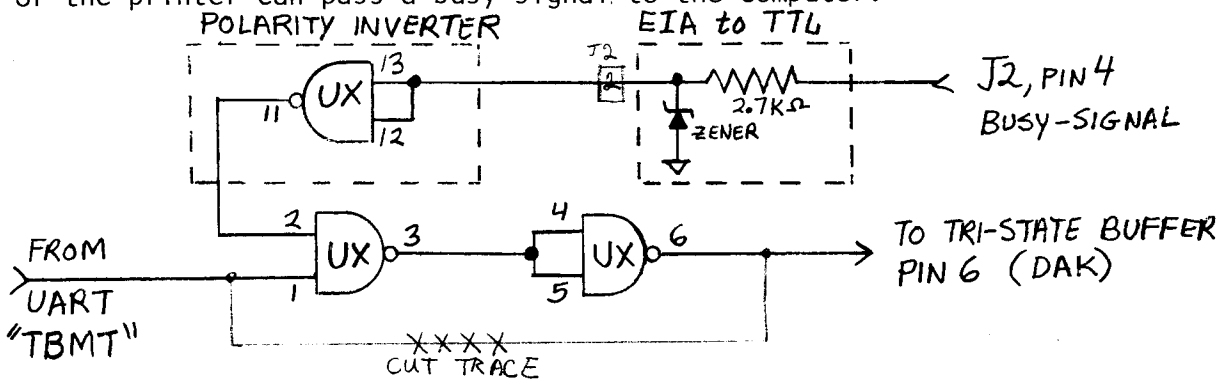
Now J2, pin 4 is the input signal pin to receive the busy signal from the printer. J2, pin 2 is a TTL level of the busy signal to be passed on to our busy detector (UX).

K. Connect J2, pin 2 to UX, pin 13.

L. Connect UX, pin 13 to UX, pin 12.

M. Connect UX, pin 11 to UX, pin 2.

This circuit is now complete! Now the busy signal from the UART or the printer can pass a busy signal to the computer.



4.10 RS232 Interconnection--Clear-to-Send, pin 5.
(Current-loop interface is disabled)

Some high speed printers use the clear-to-send signal in the RS232 interface as a buffer-full signal back to the computer. This type of hand-shaking configuration is used with the Integral Data Systems' printer. To incorporate this signal into the serial interface of the 104, follow the instructions for section 4.9 with the following exceptions:

A. Delete steps 4.9, k, l, & M.

B. Replace the deleted steps with:

K. Connect J2, pin 2 to UX, pin 2.

L. Clear-to-Send, pin 5 will go to J2, pin 4.

4.11 Baud-rate for PolyMorphic System

The PolyMorphic System doesn't use 2MHz for the main system clock (Bus pin 49), but instead it uses 1.8MHZ. This difference in clock frequence will throw the 104's baud-rate off by -10 percent, which is greater than the allowed 3 percent for 10 or 11 bit serial communication. If the system clock is 1.8MHz, then a change can be made to the 104 to reduce the baud-rate error to 2 percent.

A. Cut the trace between U32, pin 14 & 15. (backside of board)

B. Cut the trace from U32, pin 15 up to a feedthru. (0.3 inches up).

C. Connect a jumper wire from the feedthru to U32, pin 14.

D. Verify that there is no short, with an ohmmeter, between U32, pin 15 and ground (U32, pin 8). Now connect U32, pin 15 to U32, pin 16.

E. U32 now divides by 12, instead of 13 to set the baud-rates.

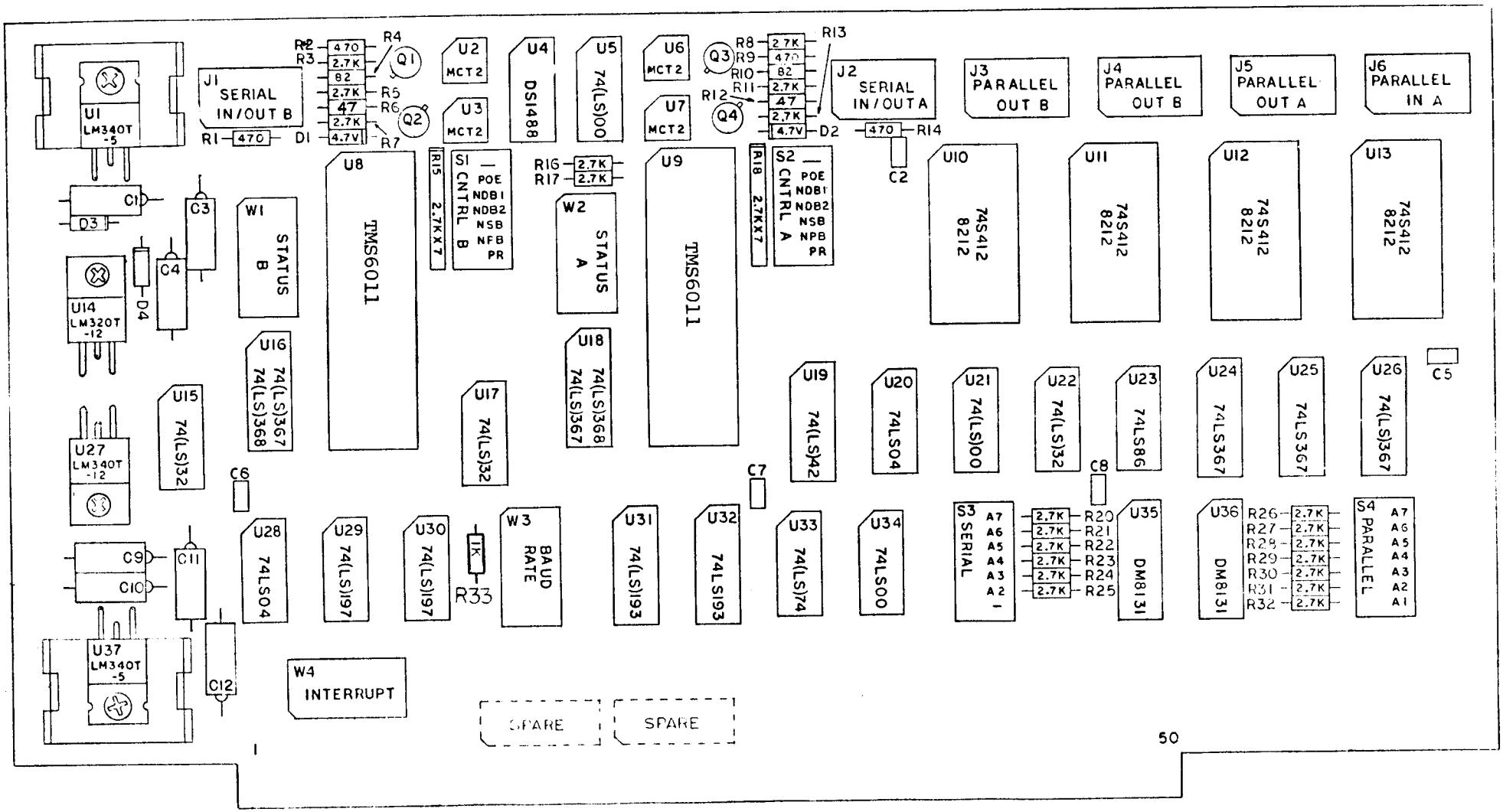
5.0 Warranty

SSM warrants its products to be free from defects in materials and/or workmanship for a period of ninety (90) days for kits and bare boards, and one (1) year for factory assembled boards. In the event of malfunction or other indication of failure attributable directly to faulty workmanship and/or material, then, upon return of the product (postage paid) to SSM at 2190 Paragon Drive, San Jose, CA 95131, "Attention: Warranty Claims Department", SSM will, at its option, repair or replace the defective part or parts to restore said product to proper operating condition. All such repairs and/or replacements shall be rendered by SSM without charge for parts or labor when the product is returned within the specified period of the date of purchase. This warranty applies only to the original purchaser.

This warranty will not cover the failure of SSM products which at the discretion of SSM shall have resulted from accident, abuse, negligence, alteration, or misapplication of the product. While every effort has been made to provide clear and accurate technical information on the application of SSM products, SSM assumes no liability in any events which may arise from the use of said technical information.

This warranty is in lieu of all other warranties, expressed or implied, including warranties of mercantability and fitness for use. In no event will SSM be liable for incidental and consequential damages arising from or in any way connected with the use of its products. Some states do not allow the exclusion or limitation of incidental or consequential damages, so the above limitation or exclusion may not apply to you.

IMPORTANT: Proof of purchase necessary for products returned for repair under warranty. Before returning any product, please call our Customer Service Department for a return authorization number.



104 2P+2S I/O

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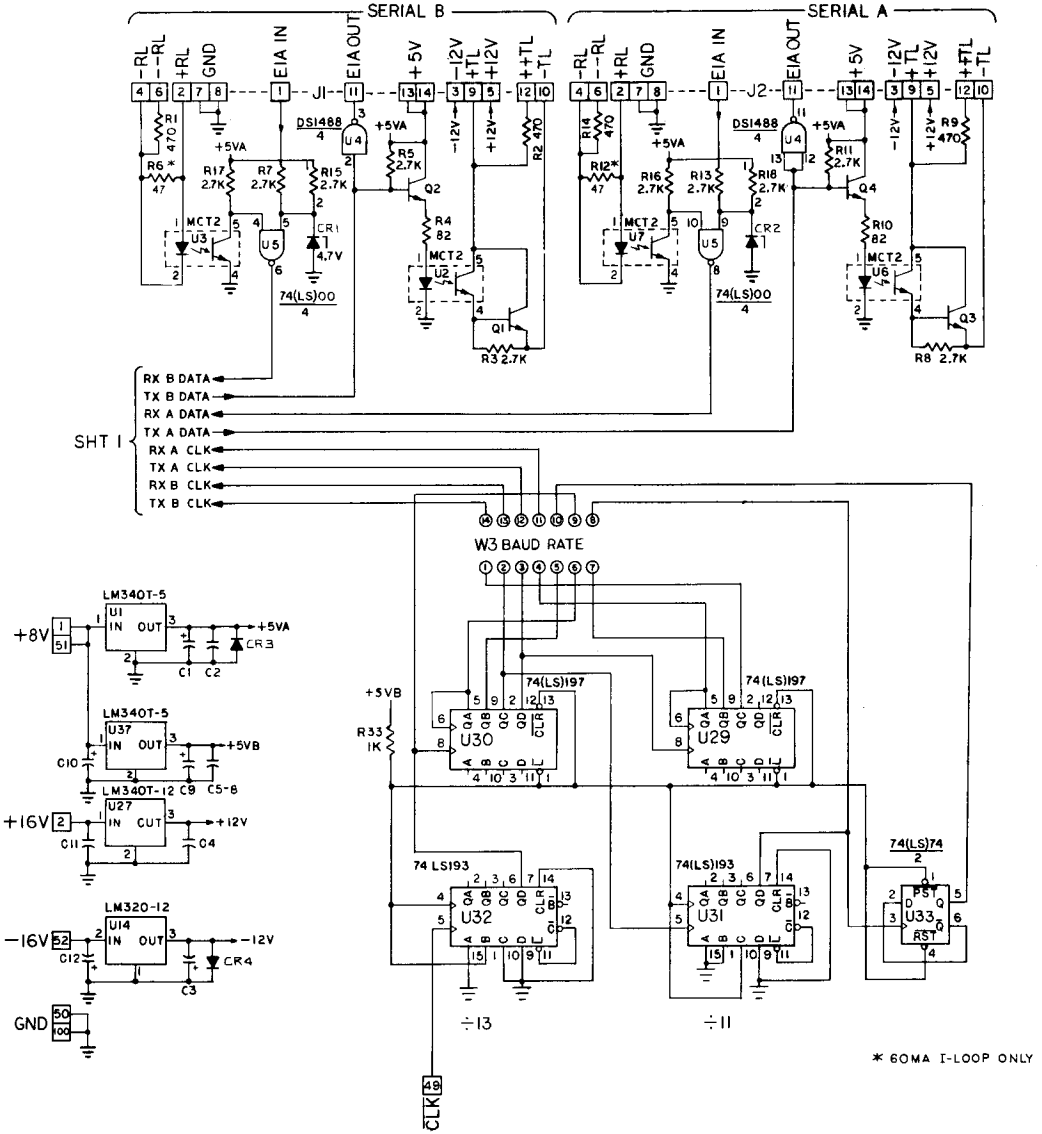
IO4 PARTS LIST

		CHIP PACK
1	U4	1488
4	U2-3,6-7	MCT2
3	U5,21,34	74L$00
2	U20,28	74L$04
3	U15,17,22	74L$32
1	U19	74L$42
1	U33	74L$74
1	U23	74L$86
2	U31-32	74L$193
2	U29-30	74L$197
5	U16,18,24-26	74367
2	U16,18	74368
2	U35-36	8131
4	U10-13	8212
4	S1-4	7 position dip switches
		UART PACK
2	U8-9	8017
		RESISTOR PACK
2	R6,12	47 ohm, 1/4 W (yellow, violet, black)
2	R4,R10	82 ohm, 1/4 W (gray, red, black)
4	R1-2,9,14	470 ohm, 1/4 W (yellow, violet, brown)
1	R33	1 K ohm, 1/4 W (brown, black, red)
21	R3,5,7-8,11,13 16-17,20-32	2.7 K ohm, 1/4 W (red, violet, red)
2	R15,18	2.7 K X 7 SIP resistors
		CAPACITOR PACK
5	C2,5-8	.1 uf monolithic radial, .1" spacing
7	C1,3-4,9-12	10 uf, 25v electrolytic axial
		DIODE PACK
2	D3-4	1N4003
2	D1-2	1N749
4	Q1-4	2N3904
		SOCKET PACK
2	U2-3,6-7 **	14 pin sockets ** SPECIAL 14 PIN SOCKETS
4	U10-13	24 pin sockets
2	U8-9	40 pin sockets
1		14 pin IC header
3		16 pin IC headers

IO4 PARTS LIST

		HARDWARE PACK
2	U1,37	7805
1	U27	7812
1	U14	7912
2	U1,37	regular heatsinks
4	U1,14,27,37	sets of #6 hardware (nut, washer and bolt)
		MISCELLANEOUS PACK
20	U4-5,15,17 20-23,28-30 33,34,J1-6,W3	14 pin sockets
13	U16,18,19 24-26,31,32 35,36,W1,2,4	16 pin sockets
3		spectra cables with 14 pin DIP plugs
1		IO4 PC Board
1		IO4 Instruction Manual
1		Warranty card

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
	SEE SHEET 1		



J1, J2 — SERIAL

EIA IN	1	14	+5V
+RL	2	13	+5V
-12V	3	12	++TL
-RL	4	11	EIA OUT
+12V	5	10	-TL
--RL	6	9	+TL
GND	7	8	GND

J3, J5 — OUTPUT

STROBE	1	14	+5V
ACK	2	13	-12V
D07	3	12	D06
D05	4	11	D04
D03	5	10	D02
D01	6	9	D00
GND	7	8	GND

W1, W2 — STATUS

—	1	16	D7
RPE	2	15	D6
ROR	3	14	D5
ODA	4	13	D4
TBMT	5	12	D3
TEOC	6	11	D2
RFE	7	10	D1
—	8	9	D0

J4, J6 — INPUT

STROBE	1	14	+5V
ACK	2	13	-12V
DI7	3	12	DI6
DI5	4	11	DI4
DI3	5	10	DI2
DI1	6	9	DI0
GND	7	8	GND

W3 — BAUD RATE

75	1	14	TX B
1.2K	2	13	RX B
600	3	12	TX A
300	4	11	RX A
2.4K	5	10	55
4.8K	6	9	9.6K
150	7	8	110

W4 — INTERRUPT

VI0	1	16	SERIAL B RX
VI1	2	15	SERIAL A RX
VI2	3	14	SERIAL A TX
VI3	4	13	SERIAL B TX
VI4	5	12	—
VI5	6	11	PARALLEL INB
VI6	7	10	PARALLEL INA
VI7	8	9	PINT

SSM MICROCOMPUTER PRODUCTS, INC.			
TITLE: I04 SCHEMATIC	P/N: 1005-002		REV A
DRAWN BY:	APPROVED:		
SCALE: —	DATE: 10-22-77	SHEET: 2	

IO4 MANUAL REGISTRATION FORM

In our effort to continually upgrade our documentation, we would appreciate any feedback that you can give concerning this manual. Please mail your comments and suggestions to SSM Customer Service at the address below.

COMMENTS AND CORRECTIONS ON THE SSM IO4 MANUAL

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