CHAPTER 4

SYM-1 SYSTEM OVERVIEW

This chapter will describe your SYM-1 microcomputer system's hardware and software in sufficient detail to allow you to understand its theory of operation. Each integrated circuit (IC) component on the SYM-1 board is discussed and related to a functional block diagram. Each functional module is then discussed schematically and the I/O connectors are described. The system memory is then covered and the software is discussed briefly. Detailed data on the software itself is found in Chapter 5 of this manual.

4.1 HARDWARE DESCRIPTION

The SYM-1 microcomputer consists primarily of a 6502 CPU, one or more 6522 Versatile Interface Adapters (VIA), a 6532 Memory and I/O Controller and two types of memory involving any combination of several different components. Because of the flexibility of the memory structure, it is discussed in a separate section (4.2, below).

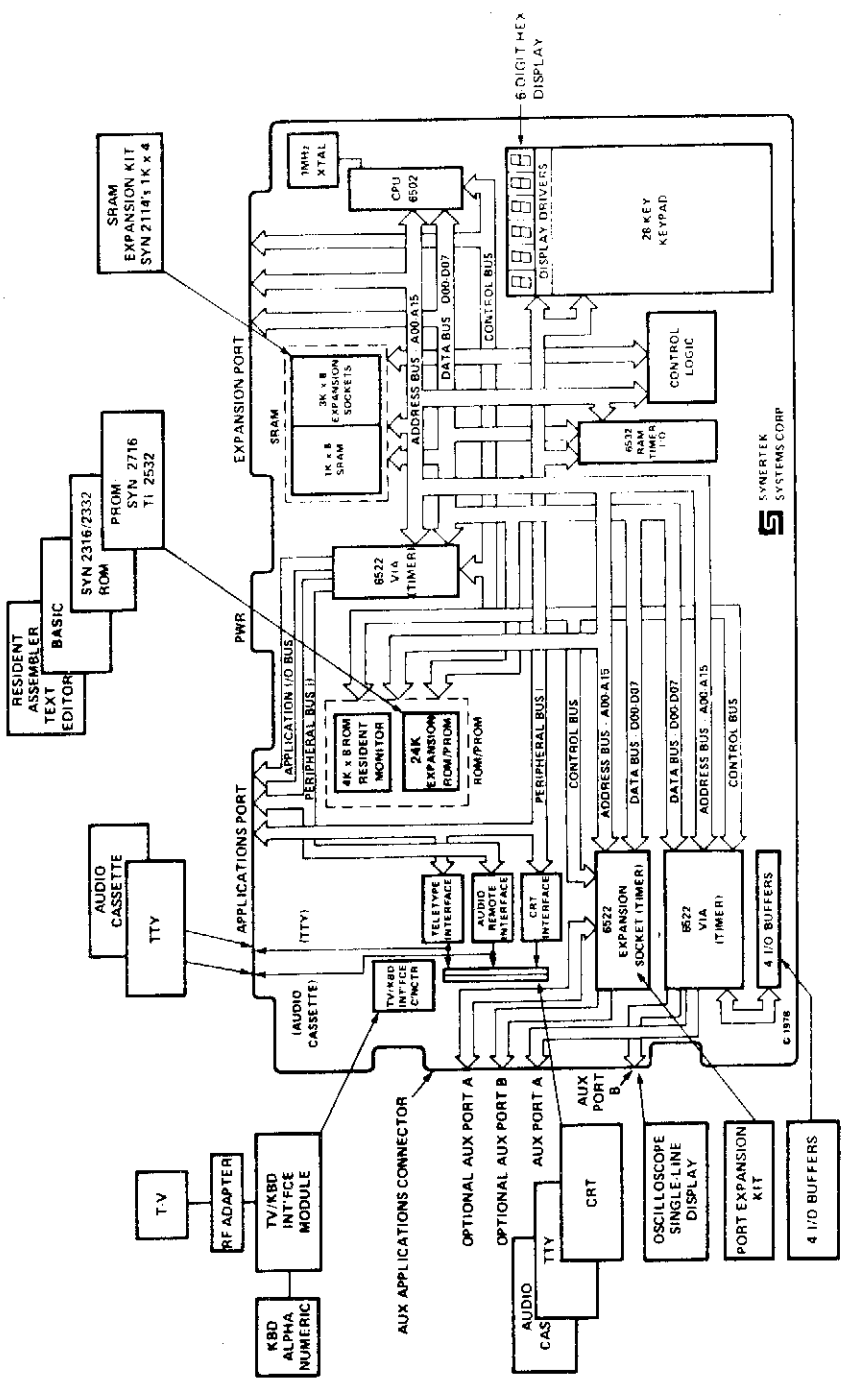
In any microcomputer system, all the components work together functionally as well as being physically interconnected. These connections are illustrated in Figure 4-1, a block diagram of the SYM-1 microcomputer system.

4.1.1 6502 CPU Description

The Central Processing Unit (CPU) of the SYM-1 microcomputer system is the 6502 microprocessor which is designed around a basic two-bus architecture--one full 16-bit address bus and an eight-bit data bus. Two types of interrupts are also available on the processor. Packaged in a 40-pin dual-in-line package, the 6502 offers a built-in oscillator and clock drivers. Additionally, the 6502 provides a synchronization signal which indicates when the processor is fetching an instruction (operation code) from program memory.

During the following discussion of the 6502, you should refer to the Data Sheets in this manual, which describe the pin connections for all three of the major types of devices present on the SYM-1 microprocessor system.

4.1.1.1 Bus Structure. The 6502 CPU is organized around two main busses, each of which consists of a separate set of parallel paths which can be used to transfer binary information between the components and devices in the SYM-1 system. The address bus transfers the address generated by the processor to the address inputs of the peripheral interface and memory devices (i.e., the 6522 and 6532 components). Note that in the Data Sheet for the 6502, the address lines originate at pins 9-20 and 22-25 of the 6502 CPU. These address lines go to pins 2-17 on the 6522 and/or to pins 2, 5-8, 10-15 and 34-40 on the 6532. Since the processor is almost always the only source of address generation in a system, an address bus is generally referred to as "unidirectional." That is the case with the SYM-1 microcomputer system. Since the address bus consists of 16 lines, the processor may read and write to a total of 65,536 bytes of storage (i.e., program memory words, RAM words, stack, I/O devices and other information), a condition which is normally referred to as a "64K memory capacity."



4-1. FUNCTIONAL BLOCK DIAGRAM

The other bus in the 6502 processor is called the data bus. It is an eight-bit bidirectional data path between the processor and the memory and interface devices. When data is moved from the processor to a memory location, the system performs a write; when the data is traveling from memory to the CPU, a read is being performed. Pins 26-33 on the 6502, 6522 and 6532 devices are all data lines connected to the data bus. The direction of the transfer of data between these pin connectors is determined by the output of the Read/Write (R/W, Pin 34) of the 6502. This line enables a write memory when it is "low" (when its voltage is below 0.4 VDC). Write is disabled and all data transfers will take place from memory to the CPU if the level is high (greater than 2.4 VDC).

One of the important aspects of the 6502 CPU is that it has two interrupt input lines available, Interrupt Request (labeled $\overline{IRQ}$ in the Data Sheet) and a Non-Maskable Interrupt (labelled $\overline{NMI}$).

Interrupt handling is one of the key aspects of microprocessor system design. Although the idea of interrupt handling is fairly simple, a complicating factor is the necessity for the processor to be able to handle multiple interrupts in order of priority (usually determined by the programmer) and not "losing track" of any of them in the process. These are concepts which you as a programmer-user of the SYM-1 will be concerned with only in advanced applications. The handling of user-generated interrupts is discussed elsewhere in this manual. If you do have occasion to alter pre-determined interrupt handling, it will be helpful for you to understand how the process works for the two types of interrupts in the 6502.

There are two main differences between the $\overline{IRQ}$ and $\overline{NMI}$ signals and their handling. First, $\overline{IRQ}$ will interrupt the CPU only if a specific flag--the Interrupt Disable Flag (I)--in the system's Processor Status Register is cleared, i.e., zero. If this flag is "set"—i.e., one--the $\overline{IRQ}$ is disabled until the flag is cleared. But an $\overline{NMI}$ request (as its name implies) always causes an interrupt, regardless of the status of the I-flag. The other main difference between the two types of interrupts is that the $\overline{IRQ}$ interrupt is "level sensitive." Any time the signal is less than 0.4 VDC and the Interrupt Disable flag is cleared, an interrupt will take place. In the case of $\overline{NMI}$, the interrupt is said to be "edge-sensitive" because it is dependent on a sequence of timing events. This interrupt will occur only if the signal goes "high" (i.e., exceeds 2.4 VDC) and then goes back to ground (less than 0.4 VDC). The interrupt occurs on the negative-going transition past 0.4 V.

The Data Sheet contains a summary of the 40 pins on the 6502 CPU and their function. Note that three of the pins--5, 35 and 36--are not connected on the 6502.

4.1.1.2 Summary. The 6502 CPU is a versatile processor. It was selected for your SYM-1 microprocessor system because of its overall functional characteristics, which facilitate its use in a wide variety of applications. Its role in the SYM-1 system will become clearer when we discuss programming and software in Section 4.3 and in Chapters 5 and 6.

4.1.2 6522 Description

The SY6522 Versatile Interface Adapter (VIA) is a highly flexible component used on the SYM-1 module to handle peripheral interfaces. Two of these devices are standard components on your SYM-1; a third may be added merely by plugging it into the socket (U28) provided. Control of the peripheral devices is handled primarily through the two eight-bit bi-directional ports. Each line of these ports can be programmed to act as

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either an input or an output. Also, several of the peripheral I/O lines can be controlled directly from the two very powerful interval timers integrated into the chip. This results in the capability to 1) generate programmable frequencies, 2) count externally generated pulses, and 3) to time and monitor real time events.

A description of the pin designations on the SY6522 is contained in the Data Sheet enclosed with your SYM-1. It should be used in following the discussion of the operation of the component in the SYM-1 module which follows. The Memory Map of the SYM-1 module (Figure 4-10) will also be helpful during this discussion.

4.1.2.1 Processor Interface. Data transfers between the SY6522 and the CPU (6502) take place over the eight-bit data bus (DB0-DB7) only while the Phase Two Clock (Ø2) is high and the chip is selected (i.e., when CS1 is high and $\overline{CS2}$ is low). The direction of these data transfers is controlled by the Read/Write line (R/W). When this line is low, data will be transferred out of the processor into the selected 6522 register; when R/W is high and the chip is selected, data will be transferred out of the SY6522. The former operation is described as the write operation, the latter the read operation.

Four Register Select lines (RS0-RS3) are connected to the processor's address bus to allow the processor to select the internal SY6522 register which is to be accessed. There are 16 possible combinations of these four bits and each combination accesses a specific register. Because of the fact that the SY6522 is a programmable-addressable device, these RS line settings, in combination with the basic device address, form the specific register address shown in the 6522 Data Sheet.

Two other lines are used in the SY6522 interface to the 6502 processor. The Reset line ($\overline{RES}$) clears all internal registers to a logical zero state (except T1, T2 and SR), placing all peripheral lines in the input state. It also disables the timers, shift register and other on-chip functions and disables interrupting from the chip. The Interrupt Request line ($\overline{IRQ}$) generates a potential interrupt to the CPU when an internal interrupt flag is set and a corresponding interrupt enable bit is set to a logical "1." The resulting output signal is then "wire or'ed" with other similar signals in the system to determine when and whether to interrupt the processor.

4.1.2.2 Peripheral Interface. As we mentioned earlier, peripheral interface is handled largely over two eight-bit ports, with each of the 16 lines individually programmable to act as an input or output line. Port A consists of lines PA0-PA7 and Port B of lines PB0-PB7.

Three registers are used to access each of the eight-bit peripheral ports. Each port has a Data Direction Register (DDRA and DDRB), which is used in specifying whether the pins are to act as inputs or outputs. If a particular bit in the Data Direction Register is set to zero, the corresponding peripheral pin is acting as an input; if it is set to "1," the pin acts as an output point.

Each of the 16 peripheral pins is also controlled by a bit in the output register (ORA and ORB) and a similar bit in the Input Register (IRA and IRB). When the pin is programmed to act as an output, the voltage on the pin is controlled by the corresponding bit in the Output Register. A "1" in the appropriate Output Register causes the pin to go "high" (2.4 VDC or higher), and a zero causes it to go "low (0.4 VDC or lower).

Functionally, reading a peripheral port causes the contents of the appropriate Input Register to be transferred to the Data Bus.

The SY6522 has a number of sophisticated features which allow very positive control of data transfers between the processor and peripheral devices through the operation of "handshake" lines which involve the use of Peripheral Control Lines (CA1-CA2 and CB1-CB2). These operations are beyond the scope of this manual; if you are interested in further information, you should consult the data sheet enclosed.

4.1.3 6532 Description

Like the SY6522 described above, the SY6532 is used on the SYM-1 module to control peripheral interface. Only one SY6532 is furnished with your SYM-1 and no others are provided for.

From an operational standpoint, the SY6532 is quite similar to the SY6522. One key difference, particularly on your SYM-1 module, is the presence of a 128-byte x 8-bit RAM within the SY6532. This is the location referred to as "System RAM" in discussions of the software operation and in the Memory Map (Figure 4-10).

A description of the pin designations on the SY6532 is included in the enclosed Data Sheet. You will notice that, like the SY6522, the SY6532 contains 16 peripheral I/O pins divided into two eight-bit ports (lines PA0-PA7 and PB0-PB7). Each of these pins can be individually programmed to function in input or output mode. $\overline{IRQ}$ on the SYM-1 SY6532 is not connected.

The Address lines (A0-A6) are used with the RAM Select ($\overline{RS}$) line and the Chip Select lines (CS1 and $\overline{CS2}$) to address the SY6532. It is in this addressing that the SY6532 differs somewhat from the SY6522's on your SYM-1 module. To address the 128-byte RAM on the SY6532, CS1 must be high and $\overline{CS2}$ and $\overline{RS}$ must both be low. To address the I/O lines and the self-contained interval timer, CS1 and $\overline{RS}$ must be high and $\overline{CS2}$ must be low. In other words, CS1 is high and $\overline{CS2}$ is low to address the chip; $\overline{RS}$ is used to differentiate between addressing RAM and the I/O Interval Timer functions. Distinguishing between I/O lines and the Interval Timer is the function of Address Line 2 (A2), which is high to address the timer and low to address the I/O section. Again, the Memory Map in Figure 4-10 clarifies these operations since they are largely software-directed and address-dependent.

4.1.4 Functional Schematics

Understanding the electrical interfaces among the various components may be of some interest to you as you use and expand your SYM-1 microcomputer. The figures on the following pages include segmented schematics, where each figure provides an electronic overview of the interface between the CPU and its related component devices and peripherals.

Table 4-1 describes the contents of each figure in this group of schematic segments.

Table 4-1. INDEX OF SCHEMATIC SEGMENTS FIGURES 4-2 TO 4-9

Figure	Function/Segment Diagrammed
4-2	TTY and CRT Interface
4-3	Audio Cassette Interface
4-4	Audio Cassette Remote Control
4-5	I/O Buffer
4-6	Keyboard/Display
4-7	Control Section
4-8	Memory Section
4-9	Oscilloscope Output Driver

Table 4-2 provides, in summary form, a list of the connector points on the four SYM-1 connectors. This allows you to determine pin and connector configurations for various application options.

Table 4-2. CONNECTOR POINTS AND THEIR FUNCTIONS IN SYM-1

Key: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 Component Side
A B C D E F H J K L M N P R S T U V W X Y Z Solder Side

EXPANSION (E)

1	SYNC	A	AB0
2	RDY	B	AB1
3	Ø1	C	AB2
4	IRQ	D	AB3
5	RO	E	AB4
6	NMI	F	AB5
7	RES	H	AB6
8	DB7	J	AB7
9	DB6	K	AB8
10	DB5	L	AB9
11	DB4	M	AB10
12	DB3	N	AB11
13	DB2	P	AB12
14	DB1	R	AB13
15	DB0	S	AB14
16	18	T	AB15
17	DBOUT (1)	U	Ø2
18	$\overline{POR}$	V	R/W
19	Unused	W	$\overline{R/W}$
20	Unused	X	AUD TEST
21	+5V	Y	Ø2
22	GND	Z	Ram-R/W

APPLICATION (A)

1	GND	A	+5V
2	APA3	B	$\overline{00}$
3	APA2	C	$\overline{04}$
4	APA1	D	$\overline{08}$
5	APA4	E	$\overline{0C}$
6	APA5	F	$\overline{10}$
7	APA6	H	$\overline{14}$
8	APA7	J	$\overline{1C}$
9	APB0	K	$\overline{18}$
10	APB1	L	Audio In
11	APB2	M	Audio Out (LO)
12	APB3	N	RCN-1 (1)
13	APB4	P	Audio Out (H1)
14	APA0	R	TTY KB RTN (+)
15	APB7	S	TTY PTR (+)
16	APB5	T	TTY KB RTN (-)
17	KB ROW O	U	TTY PTR (-)
18	KB COL F	V	KB ROW 3
19	KB COL B	W	KB COL G
20	KB COL E	X	KB ROW 2
21	KB COL A	Y	KB COL C
22	KB COL D	Z	KB ROW 1

AUXILIARY APPLICATION (AA)

1	GND	A	+5V
2	-VN	B	+VP
3	2 PA 1	C	2 PA 2
4	2 CA 2	D	2 PA 0
5	2 CB 2	E	2 CA 1
6	2 PB 7	F	2 CB 1
7	2 PB 5	H	2 PB 6
8	2 PB 3	J	2 PB 4
9	2 PB 1	K	2 PB 2
10	2 PA 7	L	2 PB 0
11	2 PA 5	M	2 PA 6
12	2 PA 3	N	2 PA 4
13	RES	P	3 CA 1
14	3 CB 1	R	SCOPE
15	3 PB 2	S	3 PB 3
16	3 PB 0	T	3 PB 1
17	3 PA 6	U	3 PA 7
18	3 PA 3	V	3 PA 0
19	3 PA 4	W	3 PA 1
20	3 PA 5	X	3 PA 2
21	3 PB 5 (B)	Y	3 PB 4 (B)
22	3 PB 7 (B)	Z	3 PB 6 (B)

(1) Jumper option
(B) Buffered

TABLE 4-2. CONNECTOR POINTS AND THEIR FUNCTIONS IN SYM-1 (Continued)

POWER (P)

1	+5V	A	+VP (optional)
2	GND	B	GND
3	+5V	C	+5V
4	GND	D	GND
5	+5V	E	-VN (optional)
6	GND	F	GND

TERMINAL (T)

1	GND
2	RS-232 IN
3	RS-232 OUT
4	N.C.
5	+5V
6	+5V
7	GND
8	+5V
9	TTY Keyboard IN +
10	TTY Keyboard IN -
11	TTY Printer OUT -
12	TTY Printer OUT +
13	N.C.
14	Audio Remote NPN HI
15	Audio Remote NPN LO
16	Audio Remote PNP LO
17	Audio Remote PNP HI
18	Audio IN
19	Audio GND
20	N.C.
21	Audio Out (HI)
22	N.C.
23	Audio Out (LO)
24	N.C.
25	Audio GND

KEYBOARD (K)

1	+5V
2	+5V
3	+5V
4	+5V
5	+VP
6	+VP
7	-VN
8	-VN
9	GND
10	GND
11	GND
12	GND
13	RS-232 IN
14	RS-232 OUT

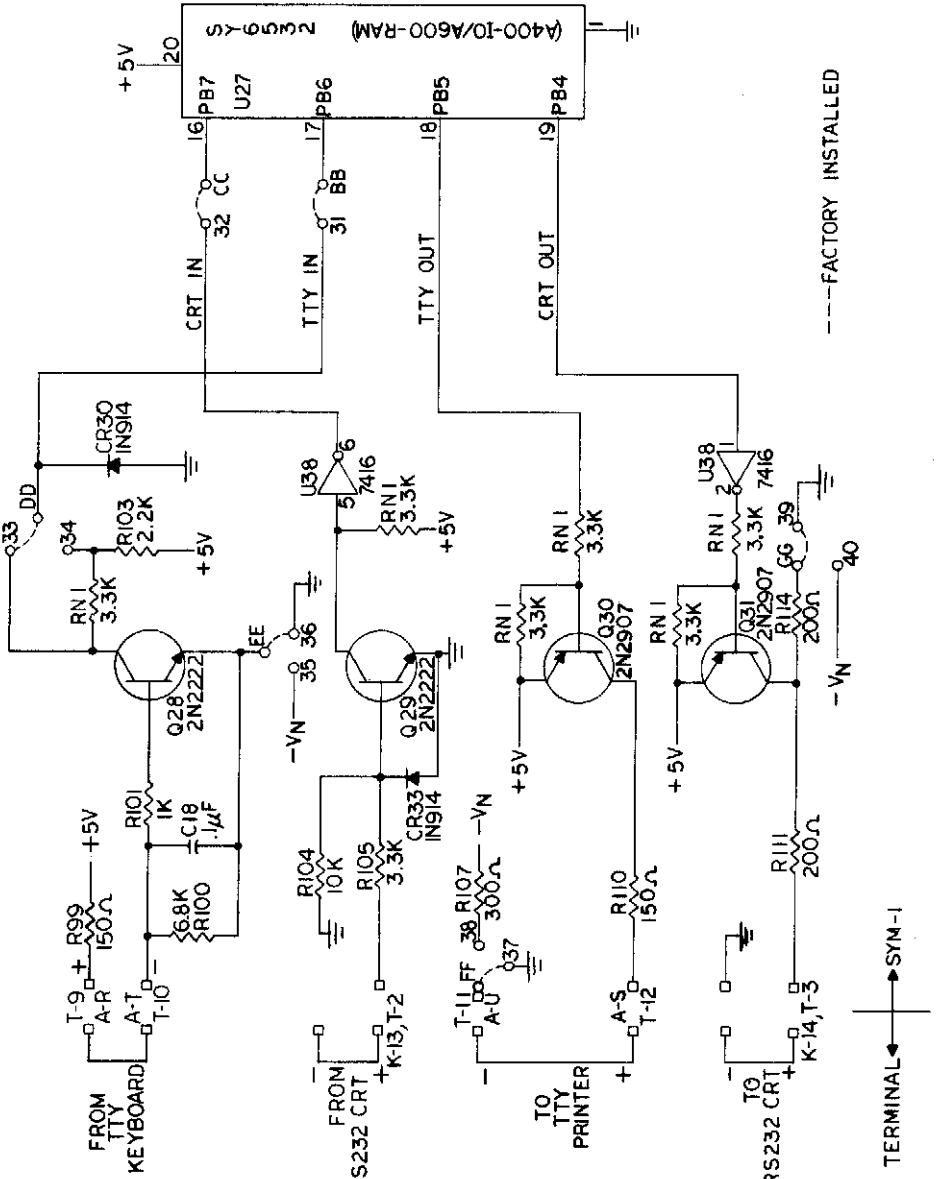


Figure 4-2. TTY/CRT INTERFACE SCHEMATIC

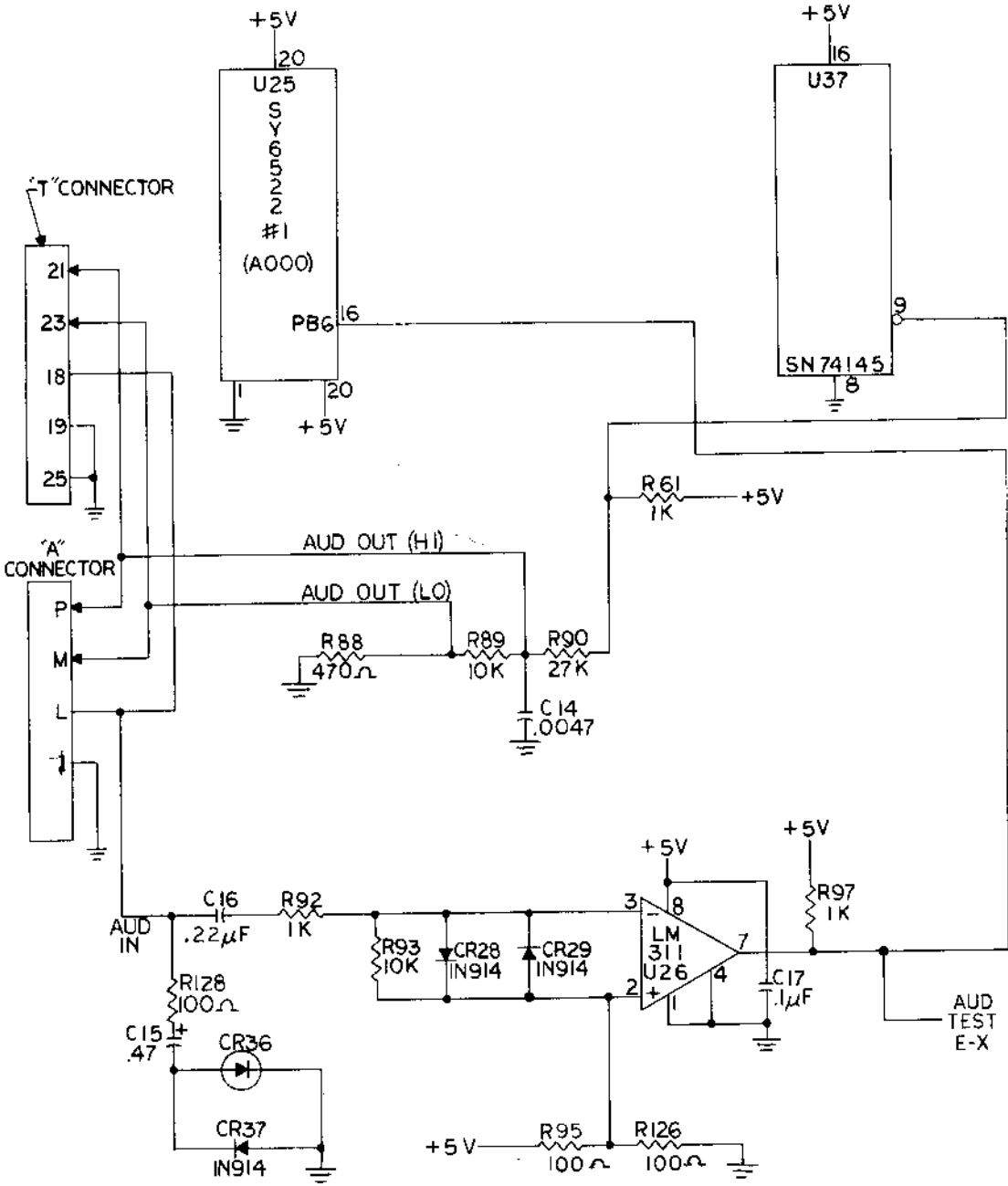


Figure 4-3. AUDIO CASSETTE INTERFACE SCHEMATIC

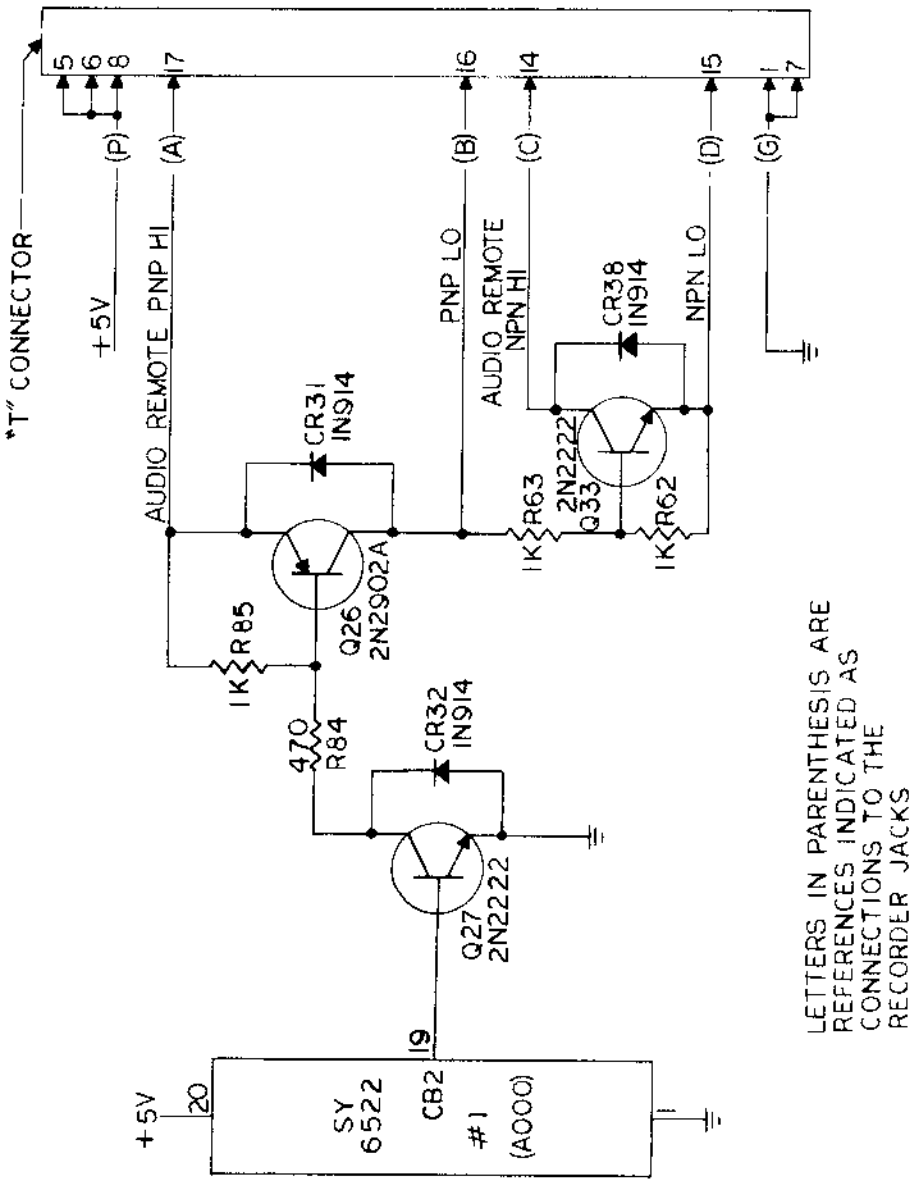
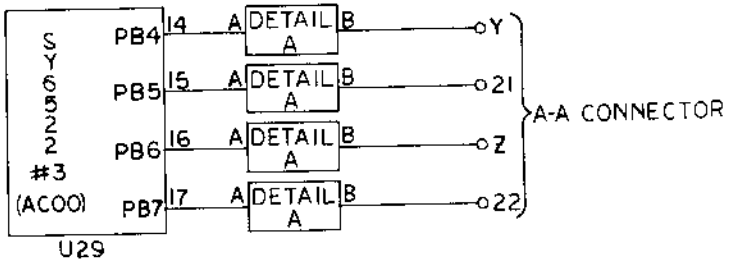


Figure 4-4. AUDIO CASSETTE REMOTE CONTROL



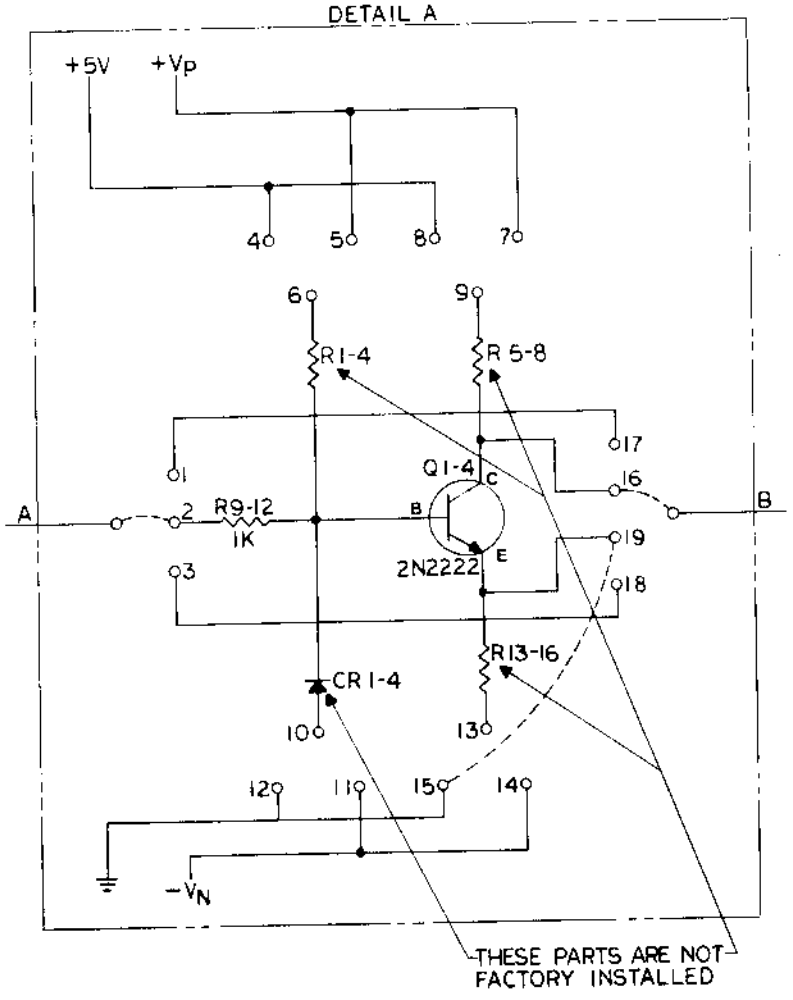


Figure 4-5. I/O BUFFERS SCHEMATIC

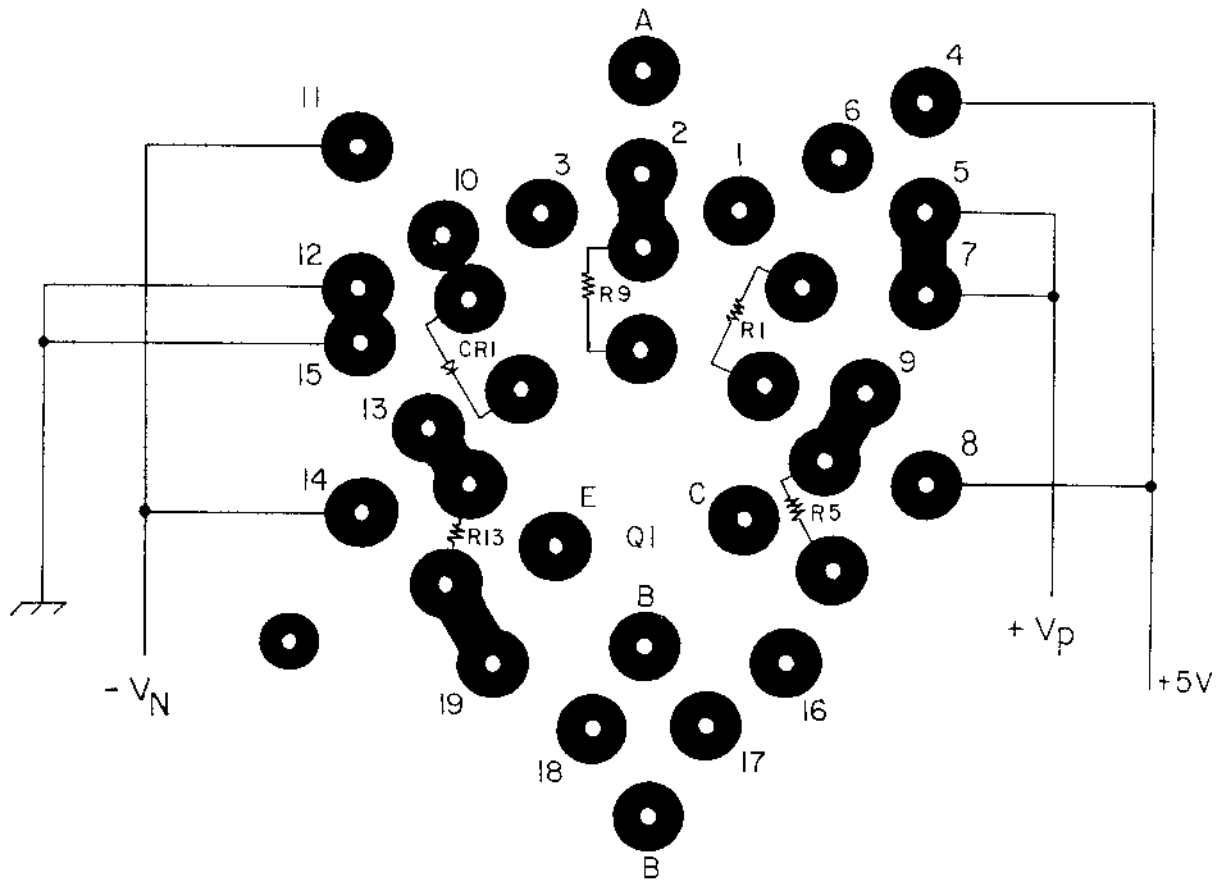


Figure 4-5a. I/O BUFFERS, PC LAYOUT BLOW-UP

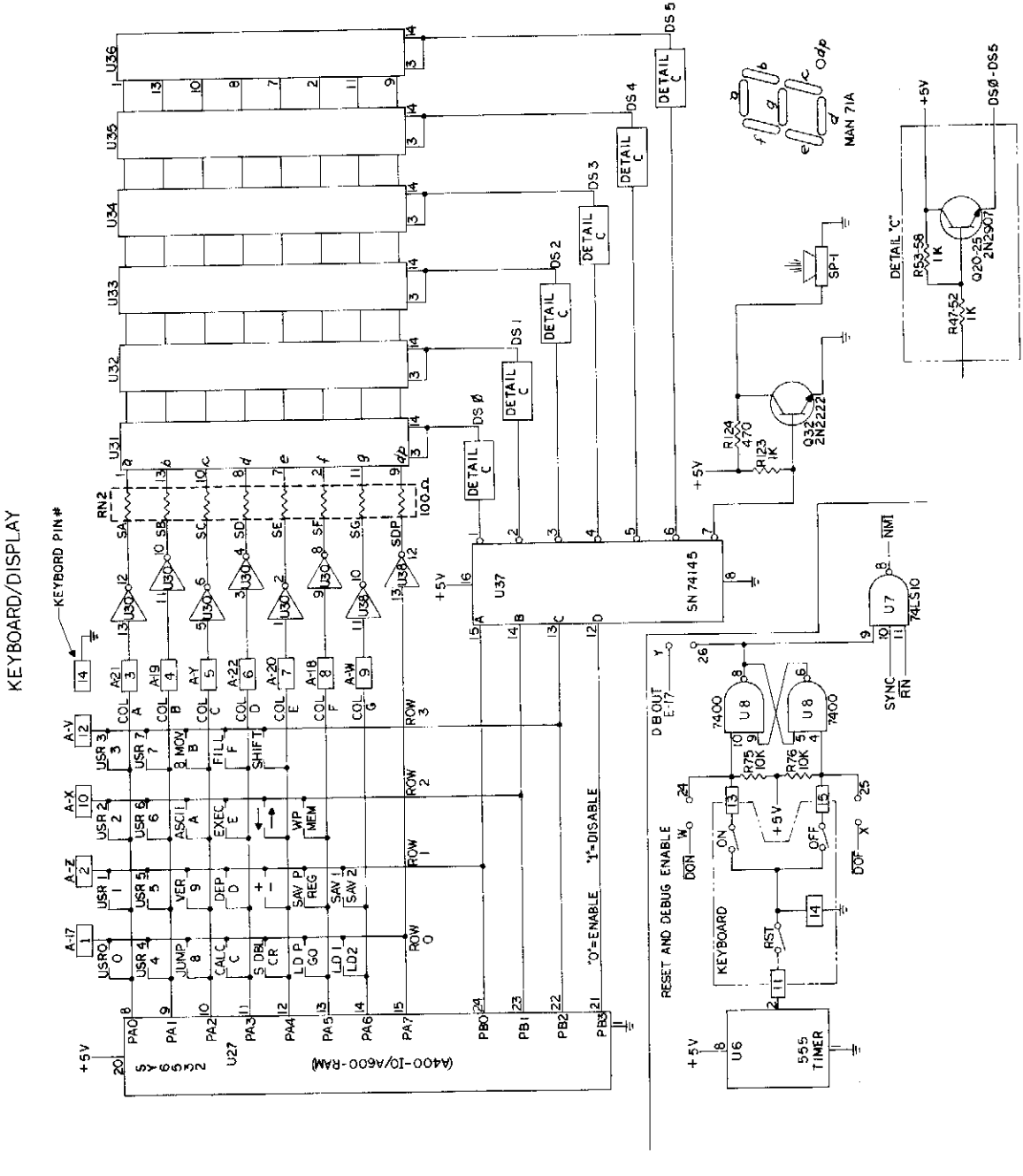


Figure 4-6. KEYBOARD/DISPLAY SCHEMATIC

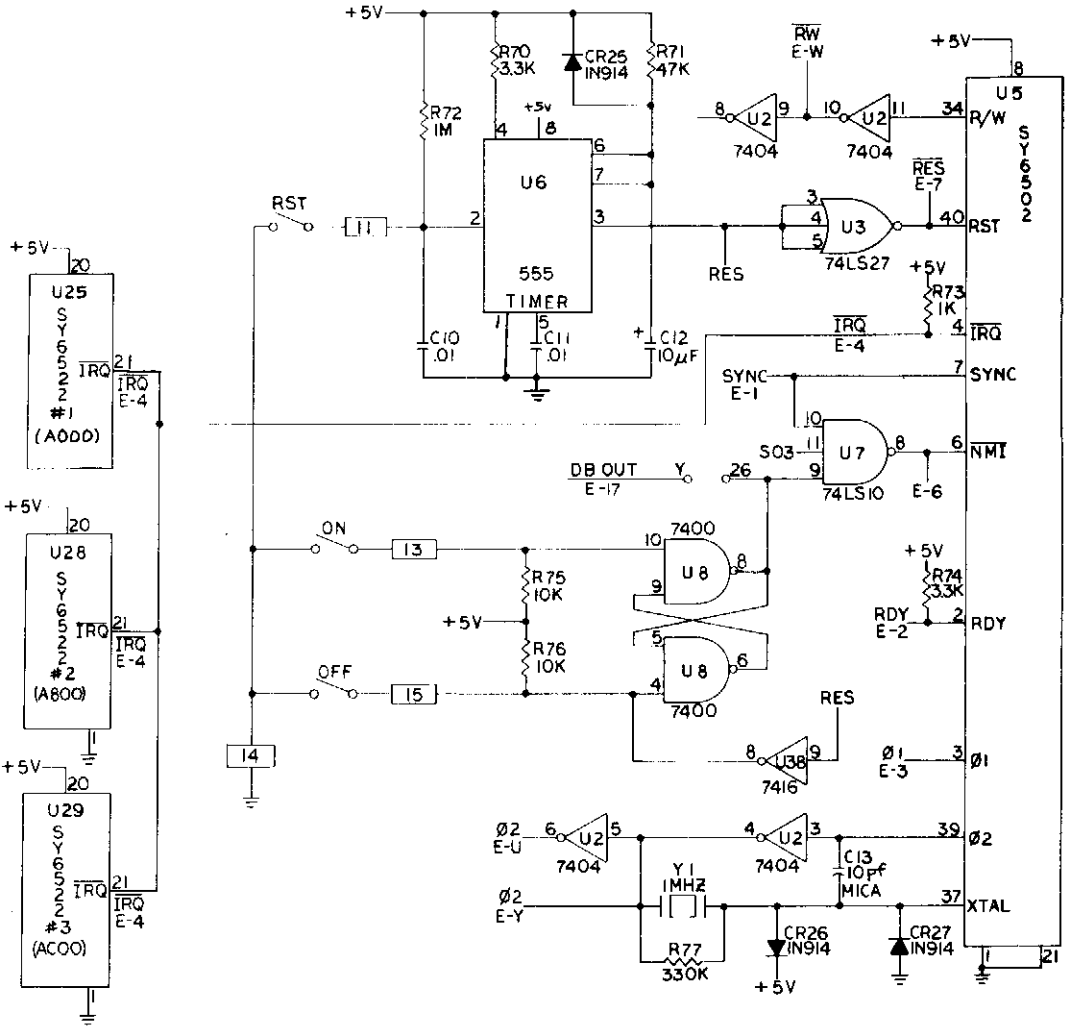


Figure 4-7. CONTROL SECTION SCHEMATIC

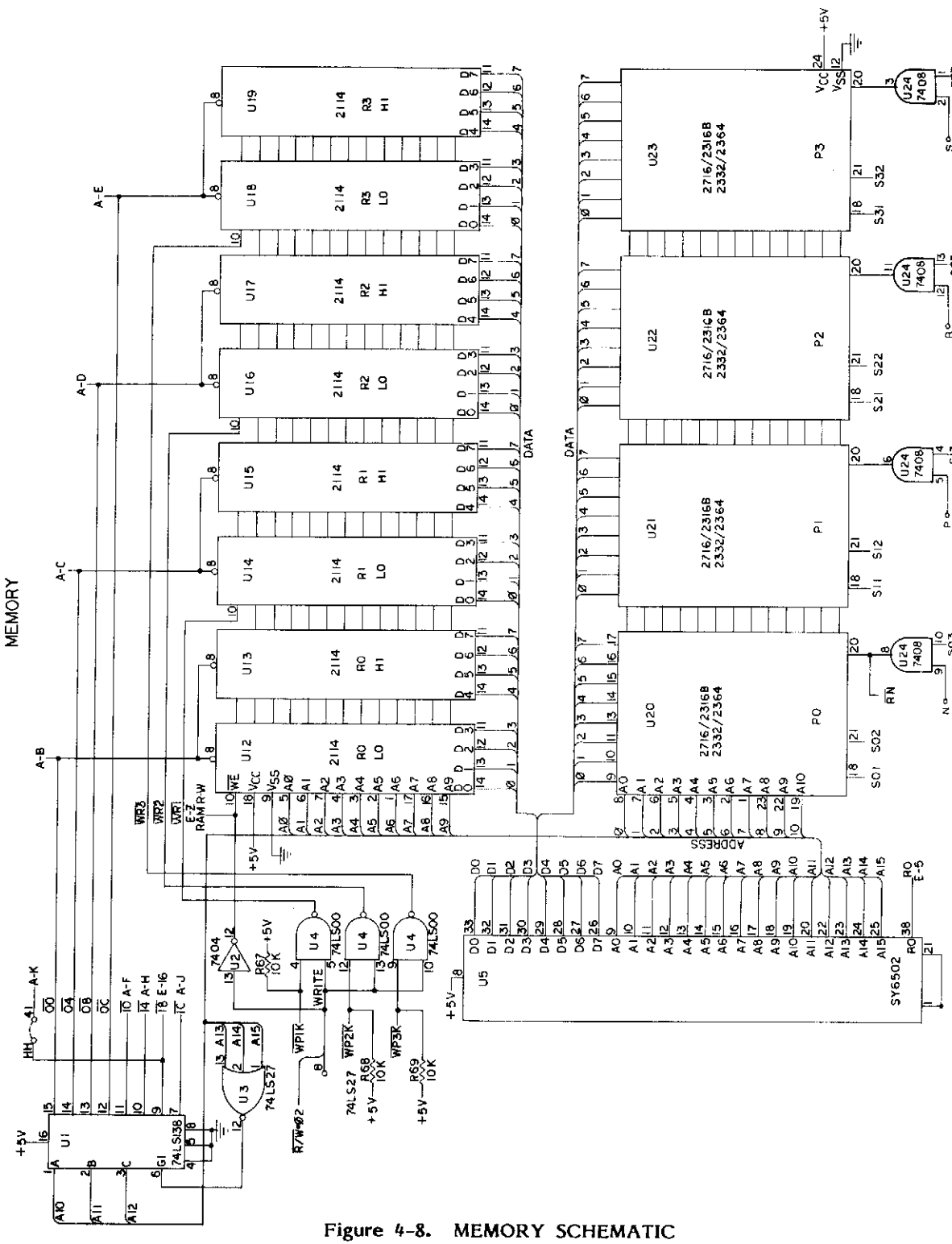


Figure 4-8. MEMORY SCHEMATIC

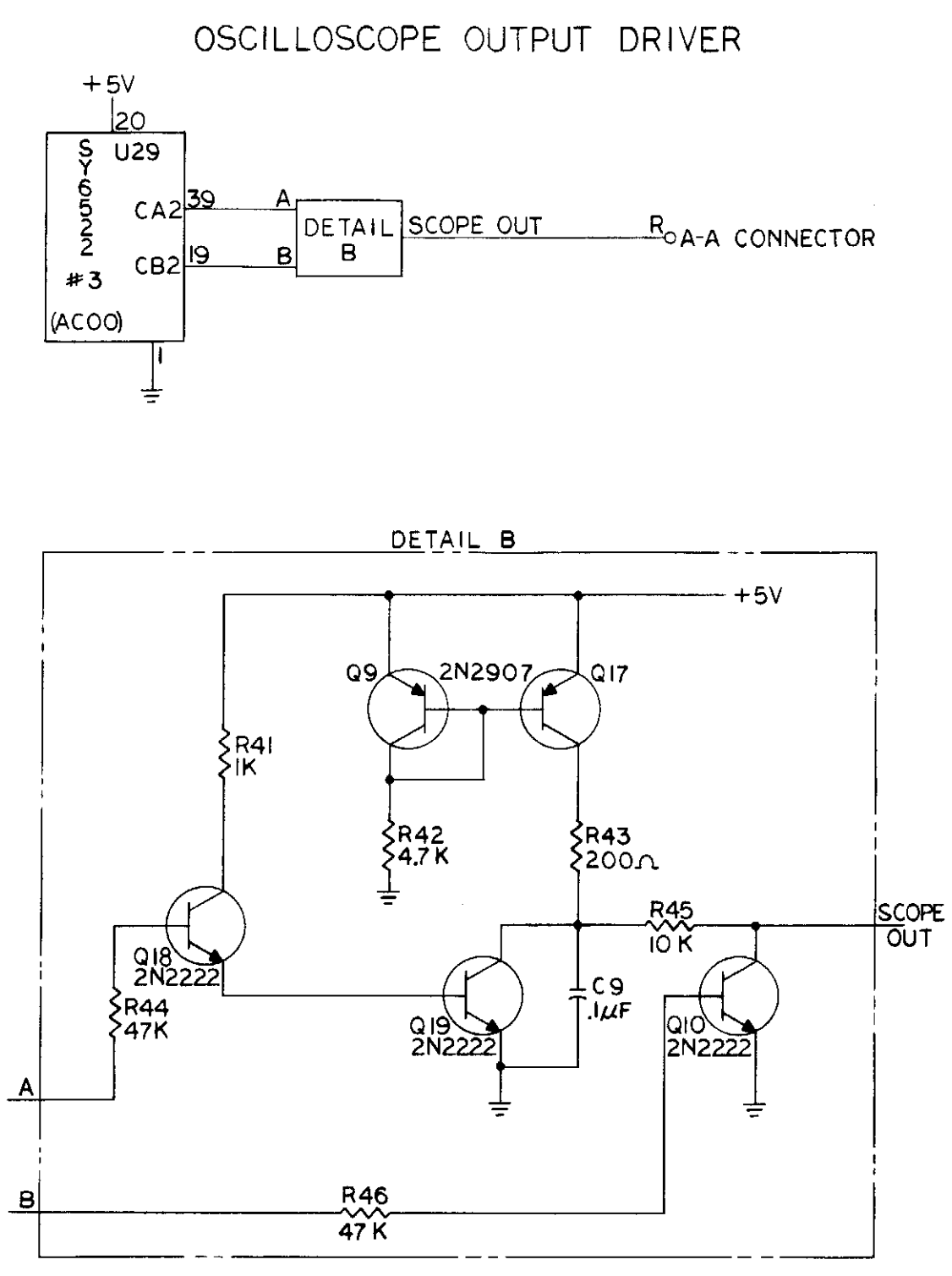


Figure 4-9. OSCILLOSCOPE OUTPUT DRIVER SCHEMATIC

4.2 MEMORY ALLOCATION

This section describes the standard memory allocation in your SYM-1 microcomputer system. It makes extensive use of the detailed Memory Map contained in Figure 4-10. Also described in this section is the technique by which ROM and RAM addressing and usage may be altered by using an array of on-board jumpers which allow you to modify and expand your SYM-1 memory. Expanding RAM memory using off-board components is taken up briefly in Section 4.2.3, although a detailed discussion of this is reserved for Chapter 8, "System Expansion".

4.2.1 Standard Memory Allocation

Figure 4-10 is a map of the standard memory allocation in your SYM-1 microcomputer. Provided with your system are 1K of on-board RAM, extending from location 0000 to 03FF in the Memory Map. Note that the top-most eight bytes (locations 00F8 to 00FF) in Page Zero of this 1K block are reserved for use by the system and should not be used by your programs. The remainder of Page Zero is largely similar to the rest of the RAM provided, but it also has some special significance for addressing which will become clearer in Section 4.3. Locations 0100-01FF in the 1K memory block furnished with your system are reserved for stack usage. Your programs may use this area, but you should use it for normal stack operations incidental to operating your programs. Locations 0200-03FF are general-use RAM for your program and data storage.

In addition to the 1K of on-board RAM furnished with your system, sockets are provided for 3K of plug-in RAM, allowing you to have 4K of on-board RAM memory. These sockets occupy memory locations 0400-0FFF.

The SUPERMON monitor resides in ROM at memory locations 8000-8FFF. (As you know, the SY6502 CPU addresses all memory and I/O identically, so that it is immaterial whether a specific address location is occupied by RAM, ROM or I/O devices.) The next 4K block, from 9000-9FFF, is reserved for future expasion of SUPERMON, although you may use those locations if you wish to do so, provided you remember that if you should obtain an expanded SUPERMON system in the future these addresses may be used.

Extending from A000-AFFF are the I/O devices on your SYM-1 module. As we have previously said, each port on the SY6522/SY6532 devices in SYM-1 is an addressable location. Sheets 2-6 of Figure 4-10 provide you with a detailed Memory Map breakdown of how these devices are addressed. Note that within the SY6532 is a 128 byte segment (locations A600-A7FF). This is the RAM which is resident on the SY6532 used by SYM-1 as System RAM. Sheet 4 of Figure 4-10 describes each memory location within System RAM in detail; you will need this data if you wish to make use of the capability of the system for modifications to SUPERMON. These modifications may include creating your own commands (as described in Chapter 5) which may be entered as if they were Monitor commands. Other such modifications making use of System RAM locations are described in Chapter 9 of this manual.

Memory locations B000-FB80 may be used by your programs, provided of course you have expanded memory to fill those address locations (see Chapter 8). Note, however, that if you plan to obtain the Synertek Systems 8K BASIC module at some later date, that module will occupy locations C000-DFFF. You should plan your applications programs accordingly. Locations FB80-FFFF are reserved for special use by the system, and should not be used in any of your applications code.

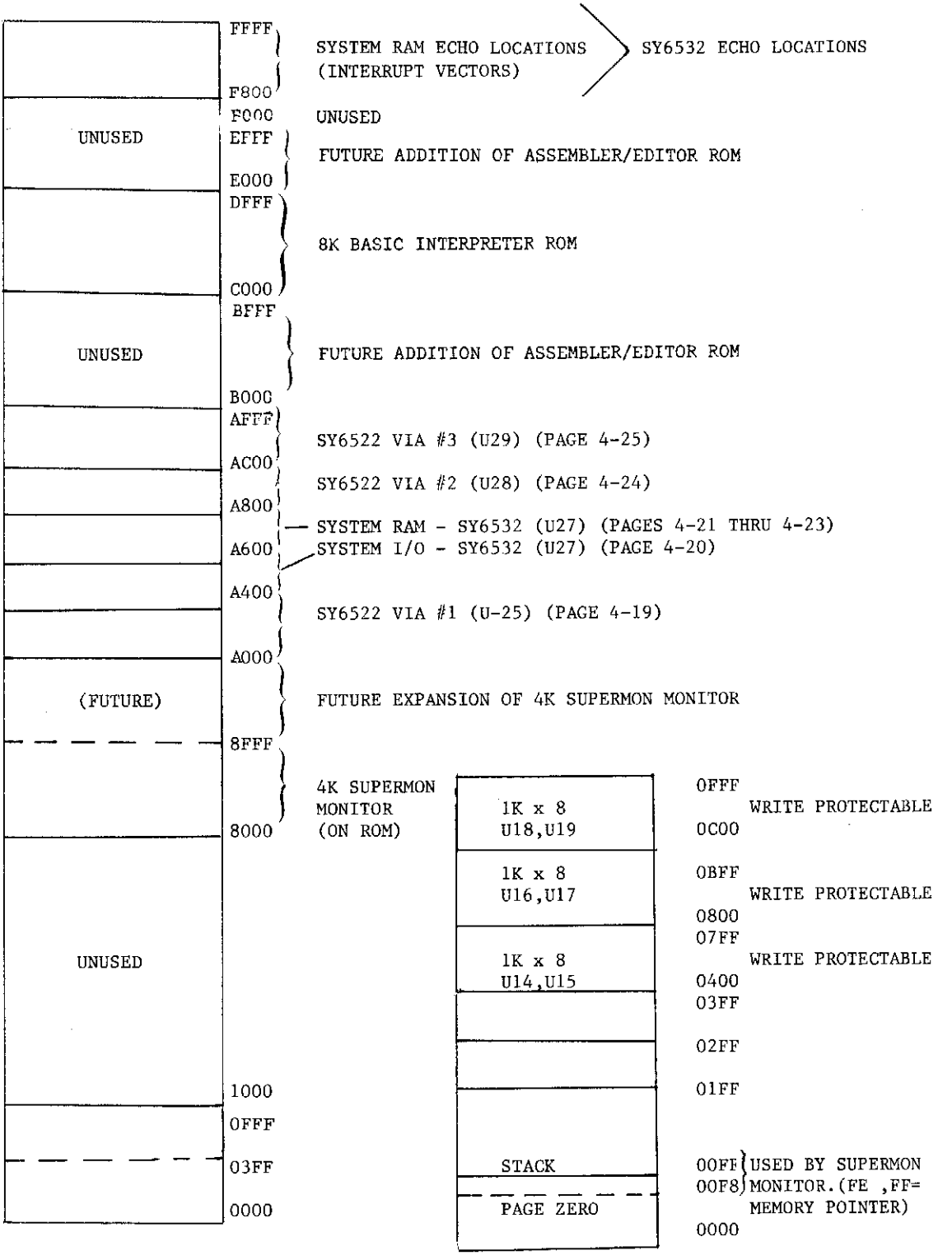


Figure 4-10. STANDARD MEMORY MAP, SYM-1

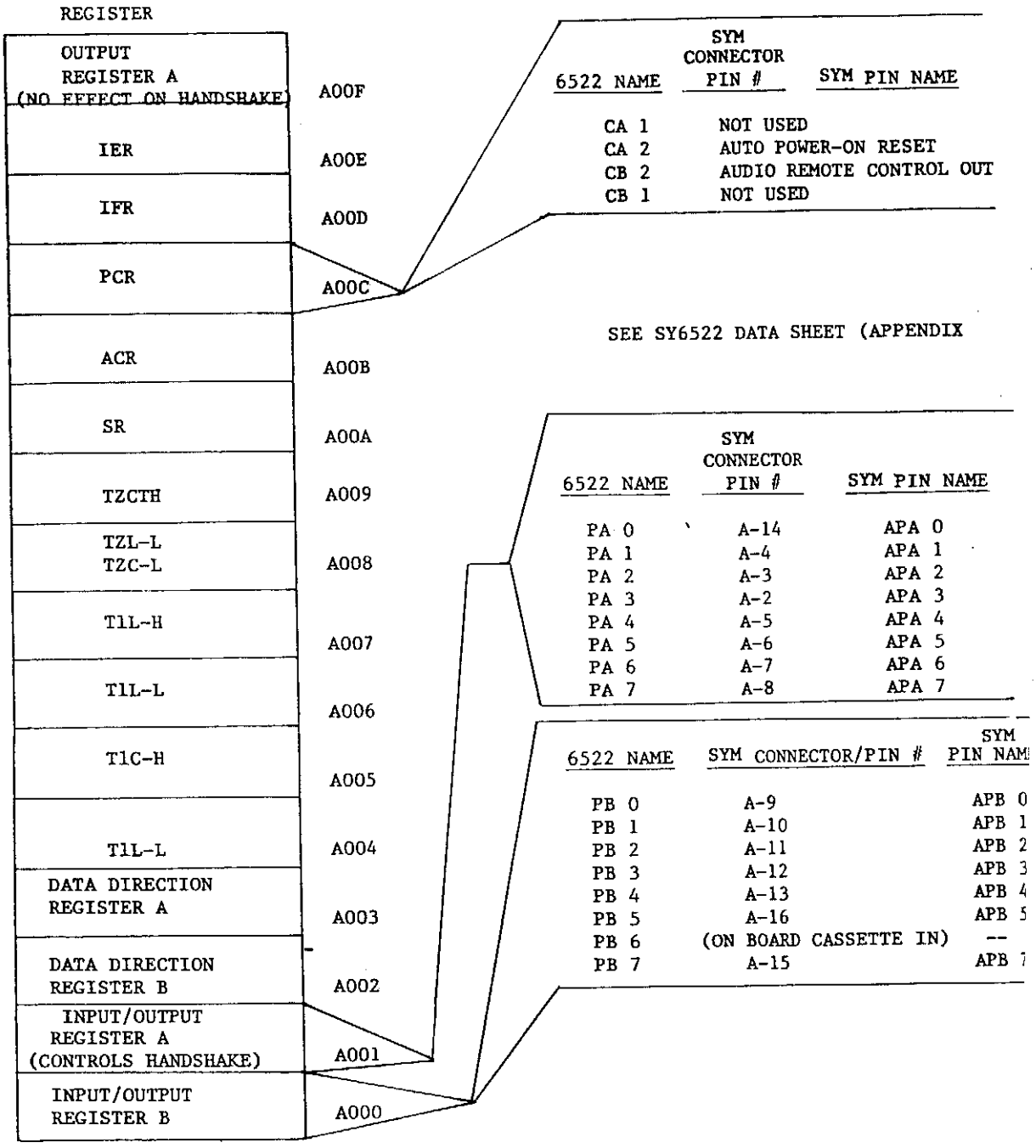


Figure 4-10 (Cont'd). MEMORY MAP FOR SY6522 VIA #1 (DEVICE U25)

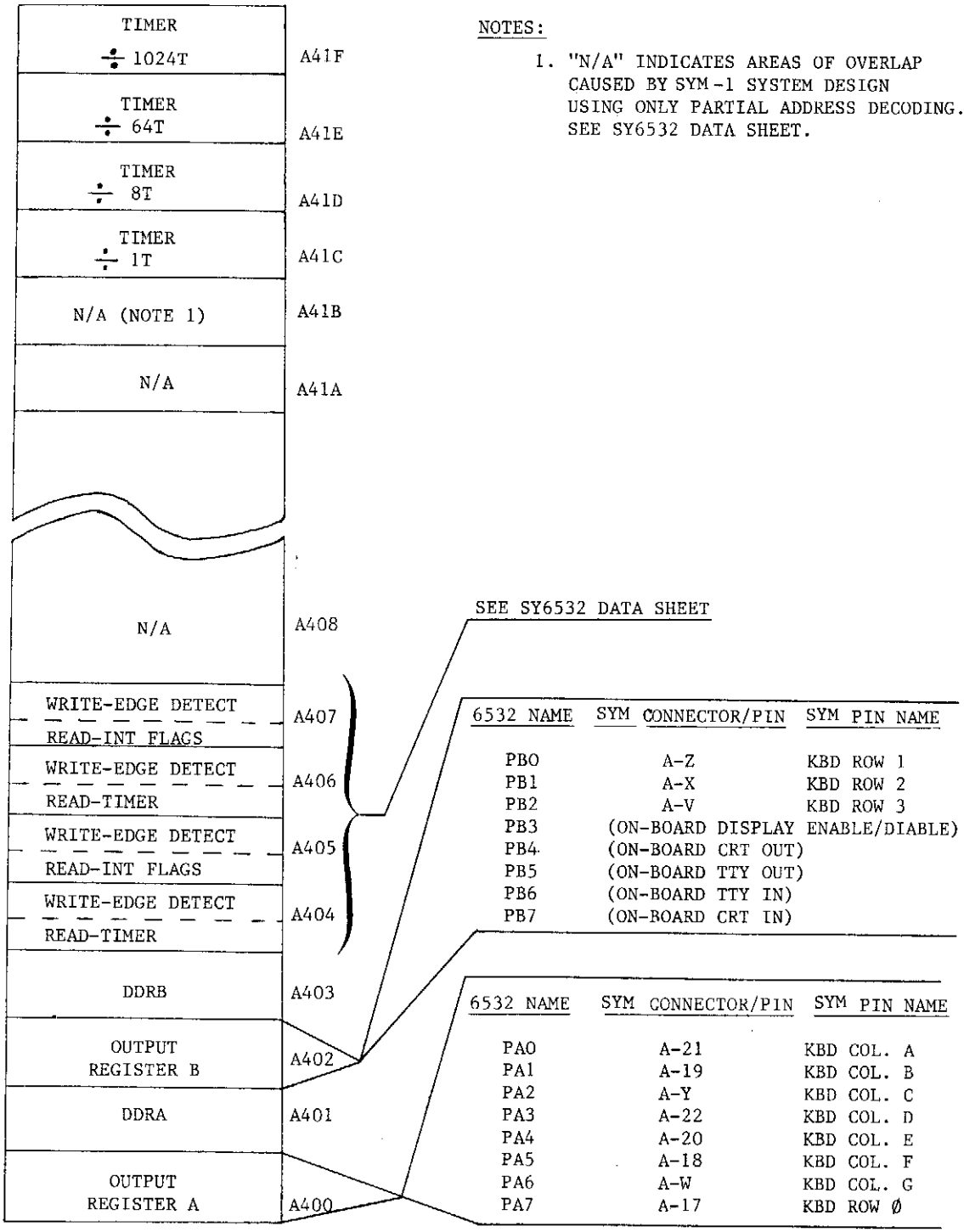


Figure 4-10 (Cont'd). MEMORY MAP FOR SY6532 (DEVICE U27)

SYMBOL	ADDRESS	DEFAULT VALUE	COMMENTS
IRQVEC	A67F	80	IRQ Vector
	A67E	0F	
RSTVEC	A67D	8B	RESET Vector
	A67C	4A	
NMIVEC	A67B	80	NMI Vector
	A67A	9B	
UIRQVC	A679	80	User IRQ Vector
	A678	29	
UBRKVC	A677	80	User Break Vector
	A676	4A	
TRCVEC	A675	80	Trace Vector
	A674	C0	
EXEVEC	A673	88	'Execute' Vector
	A672	7E	
SCNVEC	A671	89	
	A670	06	Display Scan Vector
	A66F	4C	
URCVEC	A66E	81	
	A66D	D1	Unrecognized Command Vector
	A66C	4C	
URSVEC	A66B	D1	
	A66A	81	Unrecognized Syntax Vector
	A669	4C	
INSVEC	A668	89	
	A667	6A	In Status Vector
	A666	4C	
OUTVEC	A665	89	
	A664	00	Output Vector
	A663	4C	
INVEC	A662	89	
	A661	BE	Input Vector
	A660	4C	
YR	A65F	00	
XR	A65E	00	
AR	A65D	00	
FR	A65C	00	User Registers
SR	A65B	FF	
PCHR	A65A	8B	
PCLR	A659	4A	
MAXRC	A658	10	Max. No. Bytes/Record, Paper Tape (Note 6)
LSTCOM	A657	00	Last Monitor Command
TV	A656	00	Trace Velocity (Note 5)
KSHFL	A655	00	Hex Keyboard Shift Flag
TOUTFL	A654	B0	In/Out Enable Flags (Note 4)
TECHO	A653	80	Terminal Echo (Note 3)
ERCNT	A652	00	Error Count (Note 2)
SDBYT	A651	4C	Baud Rate (Note 1)
PADBIT	A650	01	Number of Padbits on Carriage Return

Figure 4-10. SYSTEM RAM MEMORY MAP, SY6532

SYMBOL	ADDRESS	DEFAULT VALUE	COMMENTS
P1H	A64F	00	16-Bit Parameters
P1L	A64E	00	
P2H	A64D	00	
P2L	A64C	00	
P3H	A64B	00	
P3L	A64A	00	
PARNR	A649	00	No. of Parameters Entered
	A648	00	
	A647	00	Not Used
	A646	00	
RDIG	A645	06	Right-most Digit of Display Buffer
DISBUF	A644	86	Display Buffer
	A643	6E	
	A642	6D	
	A641	00	
	A640	00	
SCRF	A63F	00	Monitor Scratch Locations
SCRE	A63E	00	
SCRD	A63D	00	
TAPET2	A63C	5A	High Speed Tape Waveform
SCRB	A63B	00	Monitor Scratch Locations
SCR6	A636	00	
TAPET1	A635	33	High Speed Tape Waveform
SCR4	A634	00	Monitor Scratch Locations
SCR3	A633	00	
HSBDRY	A632	46	High Speed Tape Boundary
KMBDRY	A631	2C	KIM Tape Boundary
TAPDEL	A630	04	High Speed Tape Leader
JTABLE	A62F	D0	User Socket P3 (Jump Entry No. 7)
	A62E	00	
	A62D	C8	User Socket P2 (Jump Entry No. 6)
	A62C	00	
	A62B	03	0300 (Jump Entry 5)
	A62A	00	
	A629	02	0200 (Jump Entry 4)
	A628	00	
	A627	00	0000 (Jump Entry 3)
	A626	00	
	A625	8B	NEWDEV (Jump Entry 2) (Note 7)
	A624	64	
	A623	8B	TTY (Jump Entry 1)
	A622	A7	
	A621	C0	BASIC (Jump Entry 0)
	A620	00	
SCPBUF	A61F	--	Scope Buffer, No Defaults (32 locations)
	A600	--	

Figure 4-10. SYSTEM RAM MEMORY MAP, SY6532 (Continued)

NOTES - SYSTEM RAM

1. BAUD RATE -

BAUD	SDBYT
110	D5
300	4C
600	24
1200	10
2400	06
4800	01

2. ERCNT - Used by LD P, FILL, B MOV

   Count of bytes which failed to write correctly
   And invalid checksums up to $FF

3. TECHO - bit 7 - ECHO/NO ECHO

   bit 6 - OUTPUT/NO OUTPUT This bit is toggled everytime a control O (ASCII 0F) is encountered in the input stream.

4. TOUTFL - bit 7 = enable CRT IN
   bit 6 = enable TTY IN
   bit 5 = enable TTY OUT
   bit 4 = enable CRT OUT

5. TV - TRACE VELOCITY
   00 = SINGLE STEP

   non-zero - PRINT PROGRAM COUNTER AND ACCUMULATOR
   THEN PAUSE AND RESUME

   PAUSE DEPENDS ON TV
   (TRY TV = 09)

6. USER PC - DEFAULT = 8B4A = RESET

7. NEW DEV TO CHANGE BAUD RATE ON RS-232 INTERFACE.

Figure 4-10. SYSTEM RAM MEMORY MAP, SY6532 (Continued)

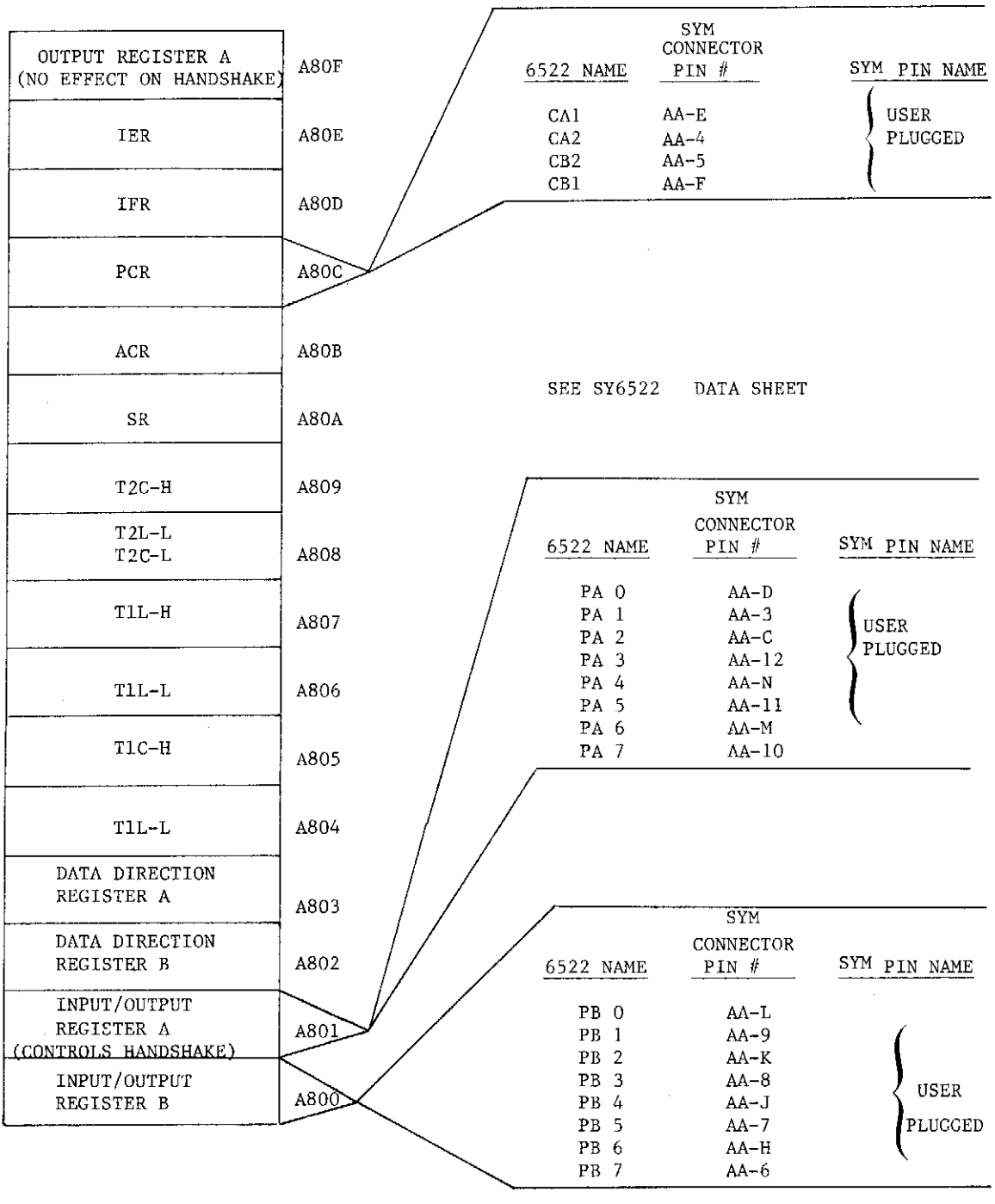


Figure 4-10. MEMORY MAP FOR SY6522 VIA #2 (DEVICE U28-USER SUPPLIED)
(Continued)

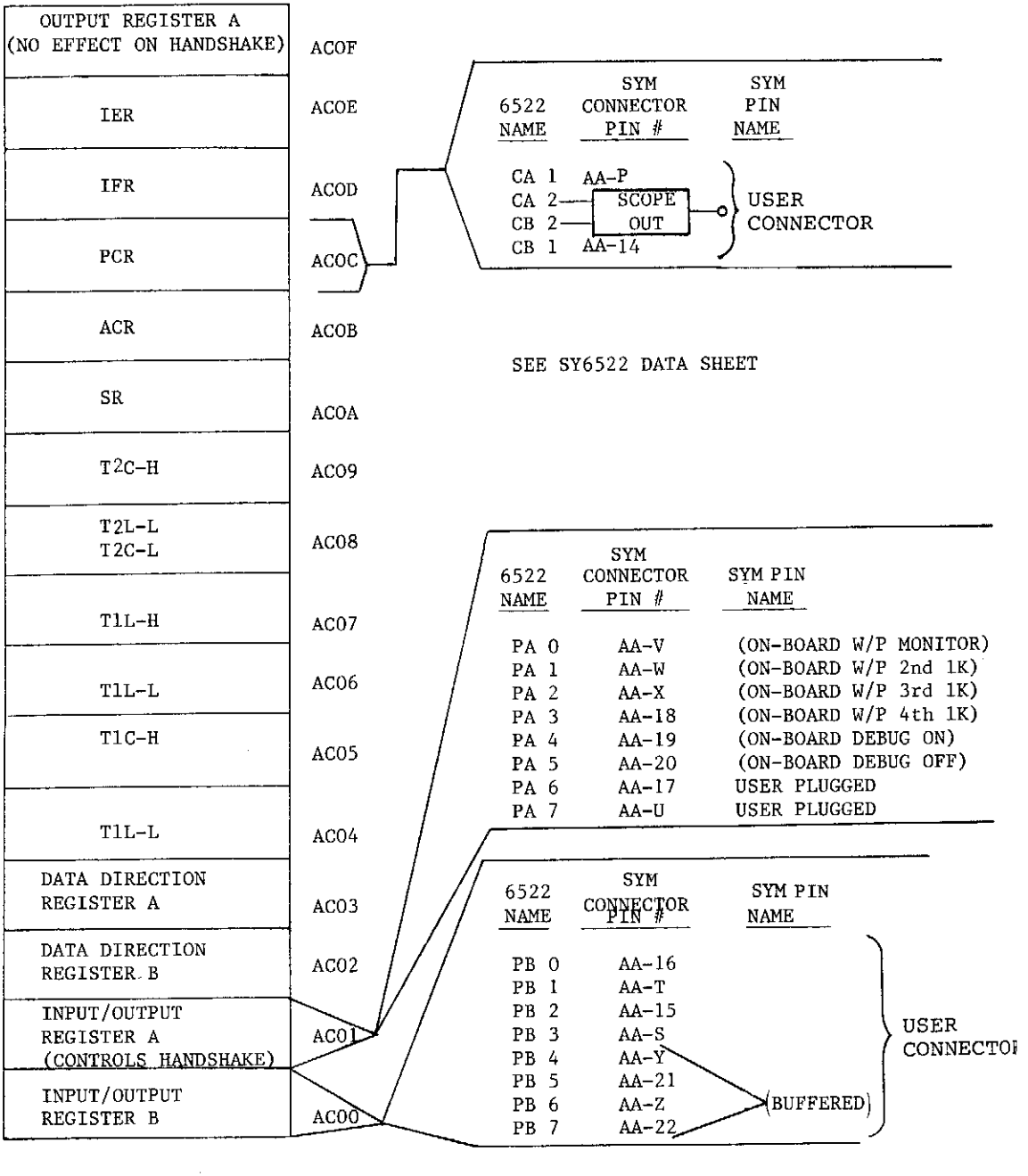


Figure 4-10. MEMORY MAP FOR SY6522 VIA #3 (DEVICE U29) (Continued)

4.2.2 Address Decoding Jumper Options

Four sockets (labeled P0-P3 on the board) for ROM, PROM or EPROM are provided with your SYM-1. Each socket may contain any of four different types of Read-Only Memory devices, up to a total of 28K. The four acceptable devices are the SY2716, the SY2316B, the SY2332 and the SY2364. Each device is slightly different, but they are all read-only memories. They may appear in any combination on a SYM-1 microcomputer system, provided their total capacity does not exceed 24K. But since the devices have different memory capacities, it is necessary to alter normal addressing to accomodate the specific devices selected.

To serve this purpose, we have provided a set of jumpers, located just to the left of the center of the board and directly under the two 74LS145's. The schematic in Figure 4-11 illustrates each useful jumper combination and Table 4-3 outlines them in greater detail. (Note that Table 4-3 contains other jumpers available on the SYM-1, not all of which pertain to memory use.) The broken lines in Figure 4-11 indicate the jumpers installed at the factory. Note, for example, that the first PROM socket, labeled PO (device U20) is associated with the address group beginning with 8000. It it were necessary to change this configuration, you would remove the connection from Pin 1 of the lower address decoder (74LS145) to jumper connection 7-J so that it becomes associated with a jumper combination which addresses the device you wish to address. Table 4-3a will assist you in configuring your selection of ROM correctly.

Near the bottom of the board below the speaker unit are four jumpers labeled JJ, KK, LL and MM. These enable Write Protection on the RAM in the four 1K blocks available on the board. Jumper 45-MM is factory-installed, enabling Write Protection on System RAM (the 128-byte block in the SY6532). As you add RAM later, or to Write Protect any of the on-board RAM aside from System RAM, you must connect the appropriate jumpers to enable the Write Protect function on the desired memory locations. RAM may be enabled for Write Protect in 1K blocks.

These jumpers offer you flexibility to adapt the SYM-1 board to your particular application. The jumpers will give you the ability to do the following:

- Use 2K, 4K, or 8K byte ROM or PROM in each 24 pin socket.
- Complete flexibility in selecting user PROM addressing.
- Ability to auto power-on to any of the ROM/PROM sockets.
- Write protect expansion RAM.

4.2.3 Off-Board Expandability

SYM-1 is expandable, on-board, up to 28K bytes of EPROM/ROM memory and 4K bytes of RAM, with 4K bytes of address space allocated to the on-board I/O devices. Further expansion of any combination of ROM, PROM, RAM or I/O can be implemented by using SYM's "E" (Expansion) connector to attach an auxiliary board containing the additional devices. Total expandability is limited only by the amount of addressing capability of the SY6502 CPU, i.e., 64K bytes.

Detailed instructions for implementing off-board expansion are contained in Chapter 8, "System Expansion."

4.2.4 I/O Buffers

Your SYM-1 board comes to you equipped with four specially configured I/O buffer circuits. (See Figure 4-5.) The circuit configuration and PC Board layout allow the user to configure these buffers in many ways.

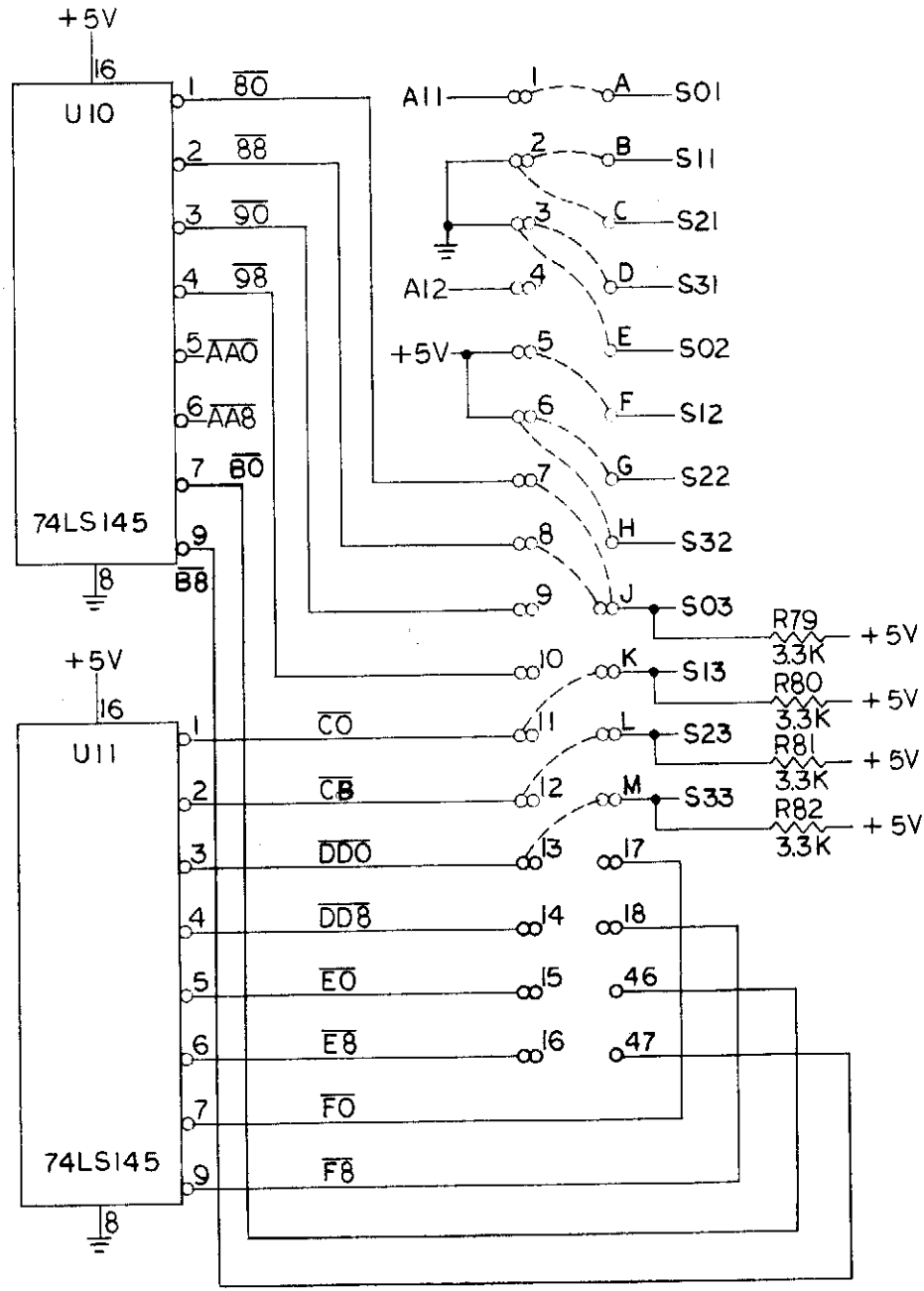


Figure 4-11. MEMORY ADDRESS DECODING JUMPER OPTIONS

Table 4-3. SYM-1 JUMPERS

JUMPER LETTER	POSITION NUMBER	DESCRIPTION
A,B,C,D E,F,G,H	1,2,3 4,5,6	PROM/ROM Device Select (See Table 4-3a)
J,K,L,M	7,8,9,10,11,12 13,14,15,16,17,18	ADDRESS SELECT (See Table 4-3b)
N	19 (1) 20	Auto Power-On to U20 (2) Disable Auto Power-On to U20
P	19 (1) 20	Auto Power-On to U21 (2) Disable Auto Power-On to U21
R	19 (1) 20	Auto Power-On to U22 (2) Disable Auto Power-On to U22
S	19 (1) 20	Auto Power-On to U23 (2) Disable Auto Power-On to U23
T U	21 22	Enables Monitor RAM at A0xx (3) Enables Monitor RAM at F8xx (3)
V	23	RCN-1 to connector A-N
W X	24 25	Enables Software Debug ON Enables Software Debug OFF
Y	26	DBOUT to connector E-17
BB CC	31 32	Connects TTY IN to PB6 @A402 Connects CRT IN to PB7 @A402
DD	33 34	To run TTY @ +5V and GND To run TTY @ +5V and -Vn (4)
EE	35 36	To run TTY @ +5V and -Vn (4) To run TTY @ +5V and GND
FF	37 38	To run TTY @ +5V and GND To run TTY @ +5V and -Vn (4)
GG	39 40	To run RS232 @+5V and GND To run RS232 @+5V and -Vn (5)
HH	41	Decode line $\overline{I8}$ to connector A-K
JJ KK LL MM	42 43 44 45	Enable software write protect 3K block Enable software write protect 2K block Enable software write protect 1K block Enable software write protect monitor RAM

Table 4-3. SYM-1 JUMPERS (Continued)

NOTES

1 Only one socket (U20, U21, U22, U23) should be jumpered to position 19 at one time. The remaining three sockets should be jumpered to position 20.

2 See software consideration of auto power-on in Chapter 9.

3 One or both can be connected at the same time.

4 These positions require a recommended -9V to -15V supply applied to the power connector pin E. R107 should be adjusted (removed and replaced) for your proper current loop requirements.

Example: (for 60ma current loops and Vn = -10V)

a. Connect DD to 33
EE to 35
FF to 38

b. $R107 = \frac{Vn - 5V}{I} = \frac{(10 - 5)}{60\ ma} = 100$

R107 = 300Ω (as installed) for 20 ma current loop and Vn=-10V

5 For RS232 devices using other than LM1489 or equivalent input receivers (i.e., probably terminals older than ten years) then GG should be strapped to 40 and a -9V to -15V supply applied to the power connector pin E.

Table 4-3a. SYM-1 PROM/ROM DEVICE SELECT

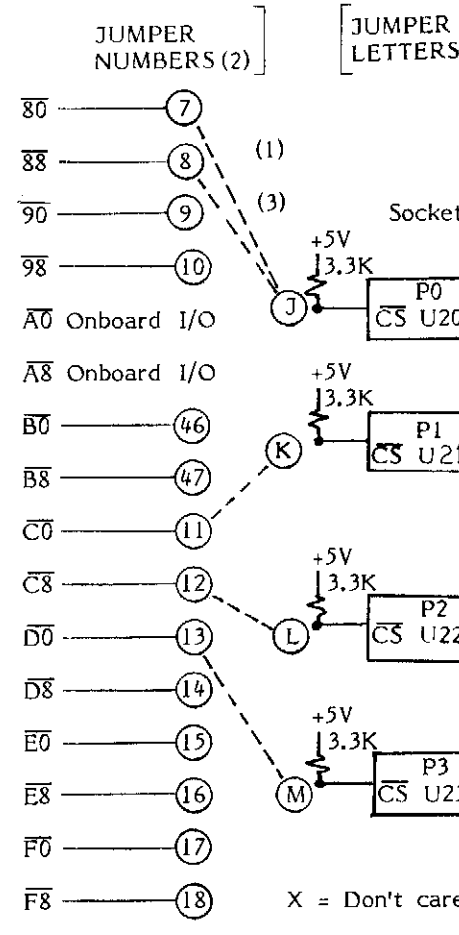
SOCKET LOCATION	SOCKET NAME	MEMORY DEVICE	JUMPER LETTER	POSITION NUMBER
U20	P0	2716	A E	2 or 3 5 or 6
U20	PO	2316	A E	2 or 3 2 or 3
U20	PO	2332	A E	1 2 or 3
U20	PO	2364	A E	1 4
U21	P1	2716	B F	2 or 3 5 or 6
U21	P1	2316	B F	2 or 3 2 or 3
U21	P1	2332	B F	1 2 or 3
U21	P1	2364	B F	1 4
U22	P2	2716	C G	2 or 3 5 or 6
U22	P2	2316	C G	2 or 3 5 or 6
U22	P2	2332	C G	1 2 or 3
U22	P2	2364	C G	1 4
U23	P3	2716	D H	2 or 3 5 or 6
U23	P3	2316	D H	2 or 3 2 or 3
U23	P3	2332	D H	1 2 or 3
U23	P3	2364	D H	1 4

NOTE: 2716 devices assumes Synertek, Intel or equivalent pin outs.

Table 4-3b. SYM-1 ADDRESS SELECT

High Order SYM-1 Address lines

2K Blocks	A 15	A 14	A 13	A 12	A 11	A 10	A 9	A 8
	1	0	0	0	0	X	X	X
	1	0	0	0	1	X	X	X
	1	0	0	1	0	X	X	X
	1	0	0	1	1	X	X	X
	1	0	1	0	0	X	X	X
	1	0	1	0	1	X	X	X
	1	0	1	1	0	X	X	X
	1	0	1	1	1	X	X	X
	1	1	0	0	0	X	X	X
	1	1	0	0	1	X	X	X
	1	1	0	1	0	X	X	X
	1	1	0	1	1	X	X	X
	1	1	1	0	0	X	X	X
	1	1	1	0	1	X	X	X
	1	1	1	1	0	X	X	X
	1	1	1	1	1	X	X	X



NOTES:

(1) Broken lines indicate delivered version of jumpers.
(2) Each jumper number represents a 2K address space decode.
(3) Jumper numbers can be wire or'ed to increase the address space of the $\overline{CS}$ on any socket (i.e., decoder is open collector.)

The single-stage circuit consists of a transistor and "circuit positions" for the user to add resistors, capacitors and dioders in any of many positions. This flexibility allows inverting and noninverting stages, input-resistive or capacitive coupling and much more. The user should refer to the schematic and P.C. layout in Figure 4-5a in order to completely understand this circuit.

4.3 SOFTWARE DESCRIPTION

Software on your SYM-1 microcomputer must be discussed from two perspectives. First, the SYM SUPERMON Monitor software which handles keyboard display, interrupts and other requirements for system operation must be understood. We will discuss this subject in succeeding sections. The second aspect of software is the microprocessor assembly language with which you will write your applications programs. A brief introduction to the 6502 instruction set is included later in this chapter.

In this chapter, we discuss the SYM-1 command language syntax only briefly; Chapter 5 contains a detailed discussion of each of the instructions in the set. Chapter 6 will help you through the process of using these and the 6502 language in applications programming by describing three selected sample programs.

4.3.1 Monitor Description - General

Figure 9-1 illustrates the general system flow of the SYM-1 SUPERMON Monitor software. As you can tell, the main program is simple and straightforward. Its purpose is to direct processing to the appropriate I/O or command routine, and for this reason it is thought of as a "driver"--it "drives" or directs the software.

The means by which the Monitor handles the direction of software flow is one of the unique features of the SYM-1 system and is worth a brief explanation at this point. We will discuss the subject in greater detail in Chapters 5 and 8.

When the SUPERMON Monitor receives a one- or two-character command from the on-board keyboard, TTY or CRT terminal, it then accepts 0-3 parameters associated with the command. The string of command and parameters (if any) is terminated by a carriage return. It is noteworthy that each instruction which may be entered by use of a single key on the on-board keyboard may also be entered with a similar command from a terminal.

Upon receiving a command and up to three parameters, SUPERMON checks to determine whether the command and its associated number of parameters is a defined combination. If so, the command is executed. Otherwise, an error message is printed or displayed showing the ASCII representation of the command which was not recognized.

For example, a "GO" with one parameter causes the program to pass control to the program stored at the memory location indicated by the parameter. Thus, a "GO" followed by "0200" instructs the system to begin executing the instructions stored starting at memory location 0200. A "GO" with no parameters (i.e., "GO" followed by a Carriage Return) will cause program execution to resume at the address stored in the "pseudo Program Counter" (memory locations A659 and A65A).

However, a "GO" command with two or three parameters is not a defined command in SUPERMON, and will result in a display or message of "Er 47". The "47" is the ASCII representation for a "G" and is designed to help you define the instruction or command which was not recognized.

The monitor is designed so that you can extend the range of defined command-parameter combinations by "intercepting" the error routine before it executes and designing your own series of pointers to memory locations to be associated with specific commands. Thus, you might wish to define a "GET" routine which could be entered at the keyboard with a "GO" and two parameters. You will learn how to do this in Chapter 9.

4.3.2 Software Interfacing

The SYM-1 Monitor is structured to be device-independent. Special requirements for device handling are "outside" the Monitor's central control routines, which isolate them from the Monitor's standard functions. Also, as we have indicated, SYM-1 commands may be entered from any device. It is not necessary to use the on-board keyboard to do so. This means you need not concern yourself with the details of I/O; they are handled internally.

4.3.3 6502 Microprocessor Assembly Language Syntax

The SY6502 microprocessor used on your SYM-1 is an eight-bit CPU, which means that eight bits of data are transferred or operated upon at a time. It has a usable set of 56 instructions used with 13 addressing modes. Instructions are divided into three groups.

Group One instructions, of which there are eight, are those which have the greatest addressing flexibility and are therefore the most general-purpose. These include Add With Carry (ADC), the logical AND (AND), Compare (CMP), the logical Exclusive OR (EOR), Load A (LDA), logical OR with Accumulator (ORA), Subtract With Carry (SBC) and Store Accumulator (STA).

Group Two instructions include those which are used to read and write data or to modify the contents of registers and memory locations.

The remaining 39 instructions in the SY6502 instruction set are Group Three instructions which operate with the X and Y registers and control branching within the program. You'll learn more about these instructions in the next section. More detailed information can be found in the Synertek Programming Manual for the SY6500 family.

An assembly language instruction consists of the following possible parts:

Label - Optional. Used to allow branching to the line containing the label and for certain addressing situations.

Mnemonic - Required. The mnemonic is a three-character abbreviation which represents the instruction to be carried out. Thus the mnemonic to store the contents of the accumulator in a specific memory location is "STA" (STore Accumulator).

Operand(s) - Some may be required, or none may be allowed. This depends entirely upon the instruction itself and may be determined from the later discussion.

Comment - Optional. Separated from last operand (or from the command mnemonic where no operand is used) by at least one blank. These words are ignored by the assembler program but are included only to allow the programmer and others to understand the program.

The SY6502 allows 13 modes of addressing, which makes it one of the most flexible CPUs on the market. Table 4-4 describes these addressing modes briefly. Details may be found in the Synertek Programming Manual for the SY6500 family.

You will note that some of the addressing modes make use of Page Zero, a concept introduced briefly earlier in this chapter. Page Zero addressing modes are designed to reduce memory requirements and provide faster execution. When the SY6502 processor encounters an instruction using Page Zero addressing, it assumes the high-order byte of the address to be 00, which means you need not define that byte in your program. This technique is particularly useful in dealing with working registers and intermediate values. As the Memory Map (Figure 4-10, Sheet 1) shows, memory locations 0000-00FF make up Page Zero.

4.3.4 SY6502 Instruction Set

Table 4-5 provides you with a summary of the SY6502 instruction set. Each instruction is shown with its mnemonic, a brief description of the function(s) it carries out, and the corresponding "op code" for each of its valid addressing modes. The "op code" is the hexadecimal representation of the instruction and is what will appear when the instruction byte is displayed by SUPERMON.

When creating applications programs for your SYM-1, you will typically write them in the SY6502 assembly language mnemonic structure shown in Table 4-5, then perform a "hand assembly" to generate the "op codes" and operands. The process of hand assembling code is explained in greater detail in Section 6.2.2. You will be referring to this table--or to your SYM Reference Card--quite frequently during programming.

To understand some of the instructions, you should be aware of six "status register" flags which are set and reset by the results of program execution. Generally, these flags and their functions are:

N - Set to "1" by CPU when the result of the previous instruction is negative
Z - Set to "1" by CPU when the result of the previous instruction is zero
C - Set to "1" by CPU when the previous instruction results in an arithmetic "carry"
Set to "0" by CPU when the previous instruction results in "borrow" (subtract)
Also modified by shift, rotate and compare instructions.
I - When "1," IRQ to the CPU is held pending
D - When "1," CPU arithmetic is operates in decimal mode
V - Set to "1" by CPU when the result of the previous instruction causes an arithmetic overflow

The Synertek Programming Manual (MNA-2) discusses this subject in greater detail.

Table 4-4. SUMMARY OF SY6502 CPU ADDRESSING MODES

SY6502 INSTRUCTION SET SUMMARY

Addressing Modes

Mode	Description	# Bytes	Example		
IMPLIED	The operation performed is implied by the instruction.	1*	TAX	AA	Code for transfer A to X
ACCUMULATOR	The operation is performed upon the A register.	1	ROL A	2A	Code for rotate left A
IMMEDIATE	The data accessed is in the second byte of the instruction.	2	LDA #3	A9 03	Code for load A immediate Constant to use
ZERO PAGE	The address within page zero of the data accessed is in the second byte of the instruction.	2	LDA Z	A5 75	Code for load A zero page Low part of address on page zero
ZERO PAGE INDEXED BY X	The second byte of the instruction plus the contents of the X register (without carry) is the address on page zero of the data accessed.	2	LDA Z,X	B5 75	Code for zero page indexed by X Base address on page zero
ZERO PAGE INDEXED BY Y	The second byte of the instruction plus the contents of the Y register (without carry) is the address on page zero of the data accessed.	2	LDX Z,Y	B6 75	Code for zero page indexed by Y Base address on page zero
ABSOLUTE	The address of the data accessed is in the second and third bytes of the instruction.	3	LDA L	AD 47 02	Code for load A absolute Low part of address High part of address

*Except BRK which is two bytes when not using SUPERMON or when in DEBUG mode.

Table 4-4. SUMMARY OF SY6502 CPU ADDRESSING MODES (Continued)

Mode	Description	# Bytes	Example		
INDEXED BY X	The address in the second and third bytes of the instruction, plus the contents of the X register is the address of the data accessed.	3	LDA L,X	BD 47 02	Code for load A indexed by X Low part of base address High part of base address
INDEXED BY Y	The address in the second and third bytes of the instruction, plus the contents of the Y register is the address of the data accessed.	3	LDA L,Y	B9 47 02	Code for load A indexed by Y Low part of base address High part of base address
INDIRECT PRE-INDEXED BY X	The second byte of the instruction plus the contents of the X register (without carry) is the address on page zero of the two-byte address of the data accessed.	2	LDA (Z,X)	A1 75	Code for load A, indirect pre-indexed by X Base address on page zero
INDIRECT POST-INDEXED BY Y	The contents of the page zero two-byte address specified by the second byte in the instruction, plus the contents of the Y register is the address of the data accessed.	2	LDA (Z),Y	B1 75	Code for load A, indirect post-indexed by Y Base address of page zero
RELATIVE BRANCH	The second byte of the instruction contains the offset (in bytes) to branch address.	2	BEQ LOC	F0 07	Code for branch if equal Seven bytes ahead
INDIRECT JUMP	The address in the second and third bytes of the instruction is the address of the address to which the jump is made.	3	JMP (LOC)	6C 47 02	Code for jump indirect Low part of indirect address High part of indirect address

Table 4-5. SY6502 CPU Instruction Set Summary

6502 INSTRUCTION SET SUMMARY

Instr	Description	Mode													Condition Codes						
		IMP	ACC	IMM	Z	Z,X	Z,Y	ABS	L,X	L,Y	(Z,X)	(Z),Y	REL	IND	N	Z	C	I	D	V	B
ADC	A + M + C → A, C Add memory to accumulator with carry			69	65	75		6D	7D	79	61	71			*	*	*	-	-	*	-
AND	A ∧ M → A "AND" memory with accumulator			29	25	35		2D	3D	39	21	31			*	*	-	-	-	-	-
ASL	C ← 7 6 5 4 3 2 1 0 ← 0 Shift left one bit (memory or accumulator		0A		06	16		0E	1E						*	*	*	-	-	-	-
BCC	Branch on C = 0 Branch on carry clear												90		-	-	-	-	-	-	-
BCS	Branch on C = 1 Branch on carry set												B0		-	-	-	-	-	-	-
BEQ	Branch on Z = 1 Branch on result zero												F0		-	-	-	-	-	-	-
BIT	A ∧ M, M_7 → N, M_6 → V Test bits in memory with accumulator				24			2C							M_7	*	-	-	-	M_6	-
BMI	Branch on N = 1 Branch on result minus												30		-	-	-	-	-	-	-
BNE	Branch on Z = 0 Branch on result not zero												D0		-	-	-	-	-	-	-
BPL	Branch on N = 0 Branch on result plus												10		-	-	-	-	-	-	-
BRK	Forced interrupt PC↓ P↓ Force break	00													-	-	-	1	-	-	1

Table 4-5. SY6502 CPU Instruction Set Summary (Continued)

6502 INSTRUCTION SET SUMMARY

Instr	Description	Mode													Condition Codes						
		IMP	ACC	IMM	Z	Z,X	Z,Y	ABS	L,X	L,Y	(Z,X)	(Z),Y	REL	IND	N	Z	C	I	D	V	B
BVC	Branch on V = 0 Branch on overflow clear												50		-	-	-	-	-	-	-
BVS	Branch on V = 1 Branch on overflow set												70		-	-	-	-	-	-	-
CLC	0 → C Clear carry flag	18													-	-	0	-	-	-	-
CLD	0 → D Clear decimal mode flag	D8													-	-	-	-	0	-	-
CLI	0 → I Clear interrupt disable flag	58													-	-	-	0	-	-	-
CLV	0 → V Clear overflow flag	B8													-	-	-	-	-	0	-
CMP	A - M Compare memory and accumulator			C9	C5	D5		CD	DD	D9	C1	D1			*	*	*	-	-	-	-
CPX	X - M Compare memory and index X			E0	E4			EC							*	*	*	-	-	-	-
CPY	Y - M Compare memory and index Y			C0	C4			CC							*	*	*	-	-	-	-
DEC	M - 1 → M Decrement memory by one				C6	D6		CE	DE						*	*	-	-	-	-	-
DEX	X - 1 → X Decrement index X by one	CA													*	*	-	-	-	-	-

Table 4-5. SY6502 CPU Instruction Set Summary(Continued)

6502 INSTRUCTION SET SUMMARY

Instr	Description	Mode													Condition Codes						
		IMP	ACC	IMM	Z	Z,X	Z,Y	ABS	L,X	L,Y	(Z,X)	(Z),Y	REL	IND	N	Z	C	I	D	V	B
DEY	Y - 1 → Y Decrement index Y by one	88													*	*	-	-	-	-	-
EOR	A ⊻ M → A "Exclusive-Or" memory with accumulator			49	45	55		4D	5D	59	41	51			*	*	-	-	-	-	-
INC	M + 1 → M Increment memory by one				E6	F6		EE	FE						*	*	-	-	-	-	-
INX	X + 1 → X Increment Index X by one	E8													*	*	-	-	-	-	-
INY	Y + 1 → Y Increment index Y by one	C8													*	*	-	-	-	-	-
JMP	(PC + 1) → PCL (PC + 2) → PCH Jump to new location							4C						6C	-	-	-	-	-	-	-
JSR	PC + 2 ↓, (PC + 1) → PCL (PC + 2) → PCH Jump to new location saving return address							20							-	-	-	-	-	-	-
LDA	M → A Load accumulator with memory			A9	A5	B5		AD	BD	B9	A1	B1			*	*	-	-	-	-	-
LDX	M → X Load index X with memory			A2	A6		B6	AE		BE					*	*	-	-	-	-	-
LDY	M → Y Load index Y with memory			A0	A4	B4		AC	BC						*	*	-	-	-	-	-

6502 INSTRUCTION SET SUMMARY

Instr	Description	Mode													Condition Codes						
		IMP	ACC	INM	Z	Z,X	Z,Y	ABS	L,X	L,Y	(Z,X)	(Z),Y	REL	IND	N	Z	C	I	D	V	B
LSR	0 → [7 6 5 4 3 2 1 0] → [C] Shift right one bit (memory or accumulator)		4A		46	56		4E	5E						0	*	*	-	-	-	-
NOP	No Operation	EA													-	-	-	-	-	-	-
ORA	A V M → A "OR" memory with accumulator			09	05	15		0D	1D	19	01	11			*	*	-	-	-	-	-
PHA	A ↓ Push accumulator on stack	48													-	-	-	-	-	-	-
PHP	P ↓ Push processor status on stack	08													-	-	-	-	-	-	1
PLA	A ↑ Pull accumulator from stack	68													*	*	-	-	-	-	-
PLP	P ↑ Pull processor status from stack	28													From Stack						
ROL	M or A [7 6 5 4 3 2 1 0] ← [C] Rotate one bit left (memory or accumulator)		2A		26	36		2E	3E						*	*	*	-	-	-	-
ROR	Rotate One Bit Right (Memory or Accumulator)		6A		66	76		6E	7E						*	*	*	-	-	-	-
RTI	P ↑ PC ↑ Return from interrupt	40													From Stack						
RTS	PC ↑, PC + 1 → PC Return from subroutine	60													-	-	-	-	-	-	-

Table 4-5. SY6502 CPU Instruction Set Summary (Continued)

6502 INSTRUCTION SET SUMMARY

Instr	Description	Mode													Condition Codes						
		IMP	ACC	IMM	Z	Z,X	Z,Y	ABS	L,X	L,Y	(Z,X)	(Z),Y	REL	IND	N	Z	C	I	D	V	B
SBC	A - M - $\overline{C}$ → A Note: $\overline{C}$ = Borrow Subtract memory from accumulator with borrow			E9	E5	F5		ED	FD	F9	E1	F1			*	*	*	-	-	*	-
SEC	1 → C Set carry flag	38													-	-	1	-	-	-	-
SED	1 → D Set decimal mode flag	F8													-	-	-	-	1	-	-
SEI	1 → I Set interrupt disable flag	78													-	-	-	1	-	-	-
STA	A → M Store accumulator in memory				85	95		8D	9D	99	81	91			-	-	-	-	-	-	-
STX	X → M Store index X in memory				86		96	8E							-	-	-	-	-	-	-
STY	Y → M Store index Y in memory				84	94		8C							-	-	-	-	-	-	-
TAX	A → X Transfer accumulator to index X	AA													*	*	-	-	-	-	-
TAY	A → Y Transfer accumulator to index Y	A8													*	*	-	-	-	-	-
TSX	S → X Transfer stack pointer to index X	BA													*	*	-	-	-	-	-

Table 4-5. SY6502 CPU Instruction Set Summary (Continued)

6502 INSTRUCTION SET SUMMARY

Instr	Description	Mode													Condition Codes						
		IMP	ACC	IMM	Z	Z,X	Z,Y	ABS	L,X	L,Y	(Z,X)	(Z),Y	REL	IND	N	Z	C	I	D	V	B
TXA	X → A Transfer index X to accumulator	8A													*	*	-	-	-	-	-
TXS	X → S Transfer index X to stack pointer	9A													-	-	-	-	-	-	-
TYA	Y → A Transfer index Y to accumulator	98													*	*	-	-	-	-	-