Radio Shack®

Service Manual

26-3806/3807

TRS-80®

DISK/VIDEO INTERFACE

(AND EXPANSION FLOPPY DISK DRIVE UNIT)

Catalog Numbers: 26-3806/3807

CUSTOM MANUFACTURED FOR RADIO SHACK, A DIVISION OF TANDY CORPORATION

Contents

Note: The expansion drive unit (Radio Shack Catalog Number 26-3807) is exactly the same as the built-in drive unit of the Disk/Video Interface. When servicing the 26-3807, refer to the drive unit portion of this service manual.

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1/Introduction

This manual is prepared for the TRS-80 Disk/Video Interface technicians working in the field or repair centers. The user of this manual should be acquainted with Z-80 CPU, 8255 PPI (Programmable Peripheral Interface), HD6845S CRTC (CRT Controller) and M5W1793-02P FDC (Floppy Disk Controller).

This manual consists of seven sections and three appendices:

- The Introduction gives general information on the TRS-80 Disk/Video Interface such as specifications, switch functions, etc.
- Section 1 describes disassembly procedures.
- Section 2 describes preventive maintenance and adjustment.
- Section 3 describes general theory of the TRS-80 Disk/Video Interface operation.
- Section 4 describes how to troubleshoot the TRS-80 Disk/Video Interface.
- Section 5 provides a parts list and an exploded view of the TRS-80 Disk/Video Interface.
- Section 6 provides schematics, P.C. board diagrams and silk screen view of the P.C. boards of the TRS-80 Disk/Video Interface.
- Appendix A provides instructions for installing an additional disk drive unit.
- Appendix B provides technical information for connector signals.
- Appendix C provides service information on the built-in FDD unit.

General

By utilizing the TRS-80 Disk/Video Interface with the TRS-80 Portable Computer, the user can fully realize the capabilities of the TRS-80 Portable Computer.

The TRS-80 Disk/Video Interface consists of:

- **Interface circuit:** Transfers data and commands to the TRS-80 Portable Computer.
- **Floppy disk drive unit:** Drives 5-1/4 inch single-sided, double density floppy disk.
- **Floppy disk controller (FDC):** Controls driving of the floppy disk drive unit.
- **Central processing unit (CPU) and memory:** Controls interface circuit, floppy disk controller and CRT controller.

To connect the TRS-80 Disk/Video Interface to the Portable Computer, use the connector cable supplied as an accessory. Install the adapter socket provided with the Disk/Video Interface on the System Bus Connector located on the bottom side of the TRS-80 Portable Computer. Connect one side of the cable to the adapter socket and the other side to the same connector located on the bottom side of the Disk/Video Interface.

System Overview

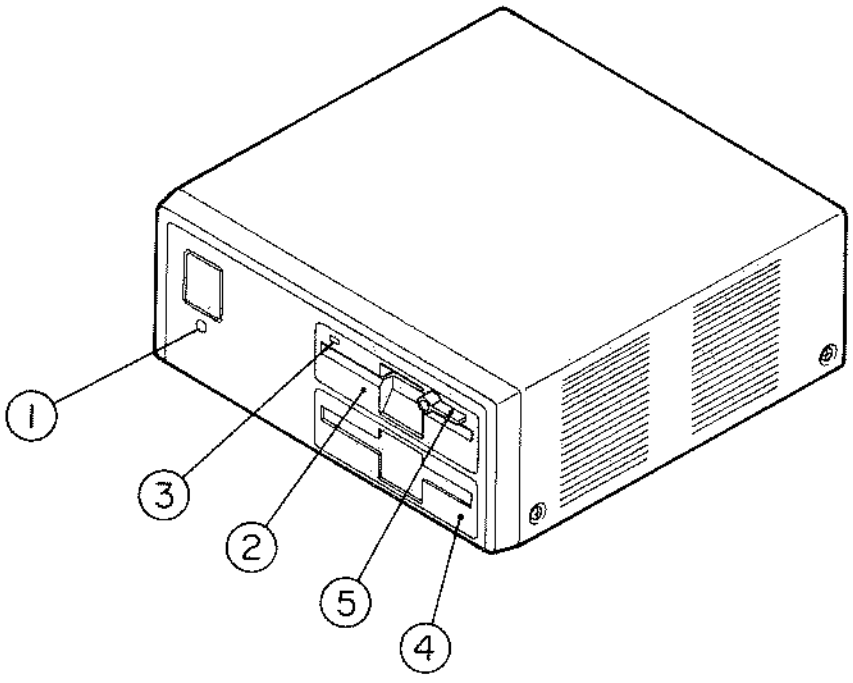


Figure 1-1. Disk/Video Interface (Front view)

(1) **LED Power Indicator:** Lights up when the Power Switch is on.

(2) **Drive 0:** This is the disk drive unit used for the BASIC SYSTEM diskette.

(3) **Drive Select LED:** LED lights during access of the diskette.

(4) **Optional Disk Cover:** Remove this cover to install the expansion drive unit. See Appendix A.

(5) **Clamp Lever:** Turning this lever downward locks the disk drive unit into the operating position.

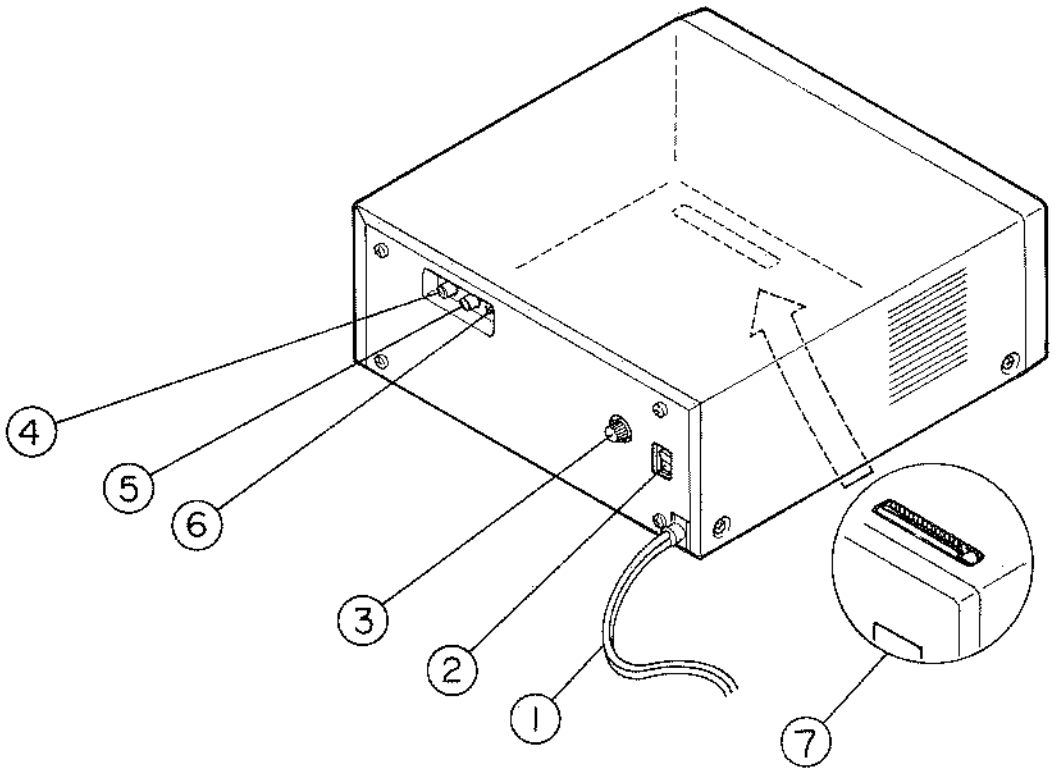


Figure 1-2. Disk/Video Interface (Rear view)

(1) **AC Power Cord:** Supplies AC power source to the Disk/Video Interface.

(2) **Power Switch:** Turn this switch on to supply AC power to the Disk/Video Interface.

(3) **Fuse Holder:** Contains a fuse. Remove the AC cord from the AC receptacle while inspecting/replacing the fuse.

(4) **Video Monitor Terminal:** Connect your video monitor for a 80 x 25 or 40 x 25 line display.

(5) **Home TV Terminal:** Provides RF output modulated to Channel 3 or Channel 4* of the TV frequency. Connect your home TV set to this terminal using the TV cable and switch box supplied.

(6) **Channel 3/Channel 4 Exchange Switch**:** Select either Channel 3 or Channel 4 RF output (Channel 1 or Channel 2 for Australia), whichever is not used in your area.

(7) **System Bus Connector:** Connect the system bus connector of the Portable Computer using the attached cable.

* Channel 1 or Channel 2 for Australia version.
Channel 36 UHF signal for UK/Belgium version.

** Deleted for UK/Belgium version.

Specifications

Operating Voltage:	120 Volts AC for USA and Canada 220 Volts AC for Belgium 240 Volts AC for UK and Australia
Power Consumption:	66 Watts
Operating Temperature Range:	5°C ~ 40°C
Operating Humidity Range:	20 to 80%
Dimensions (W x H x D):	430 x 125 x 300 mm (16-15/16" x 4-15/16" x 11-10/12")
Weight:	8 kg (17.7 lbs)
Disk Drive:	Single-sided, double density
Spindle Rotation Speed	300 R.P.M.
Seek Time	6 msec.
Average Access Time	88 msec.
Motor Starting Time	500 msec.
Data Density	5536 B.P.I.
Track Density	48 T.P.I.
Number of Tracks	40
Number of Sectors	18
Bytes/Sector	256 Bytes
CRT Interface:	
Display Mode	40 columns x 25 lines or 80 column x 25 lines
Display attribution	Normal, Blink, Reverse or Reverse and Blink
RF Output Channel	VHF 3 or 4 channel for USA/Canada VHF 1 or 2 channel for Australia UHF 36 channel for UK/Belgium
Modulation Ratio	75% Typ.
Output Impedance	75 ohms
RF Output Level	62.5 dBμ (67.3 dBf) Typ.
Horizontal Scanning Frequency	15.625 kHz
Vertical Scanning Frequency	60.1 Hz

2/Disassembly Instructions

Top Case

1. Disconnect the cables from the unit.
2. Remove the four screws (A) on the left and right of the unit.
3. Remove the top case by sliding it toward the rear of the unit.

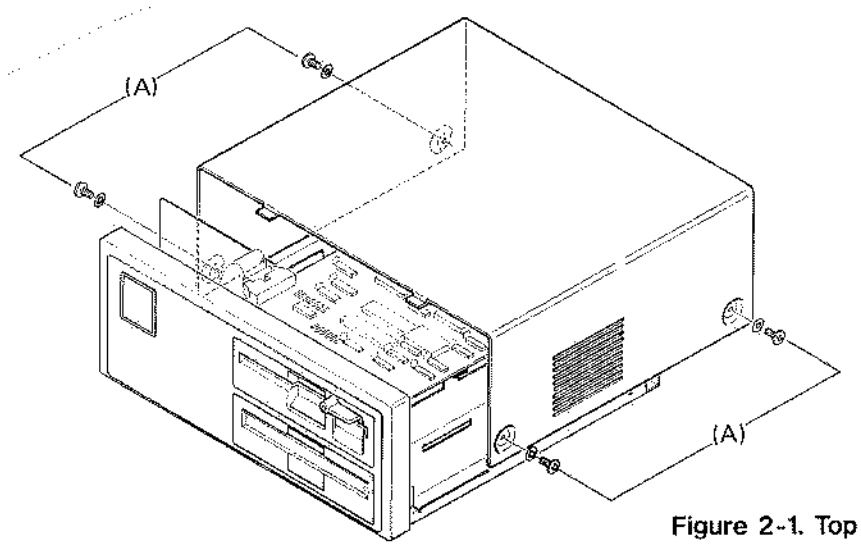


Figure 2-1. Top Case Removal

Main P.C. Board

1. Disconnect the two connectors marked CN1 and CN4 on the main P.C. Board.
2. Remove the four screws (B).
3. Take out the main P.C. Board. Be careful not to damage the connectors and switch inside on the rear panel.
4. Disconnect the connector marked CN2 and ground lead.

Power Supply P.C. Board

1. Disconnect all the connectors from the power supply P.C. Board.
2. Remove the two screws (C) and take out the power supply P.C. Board.

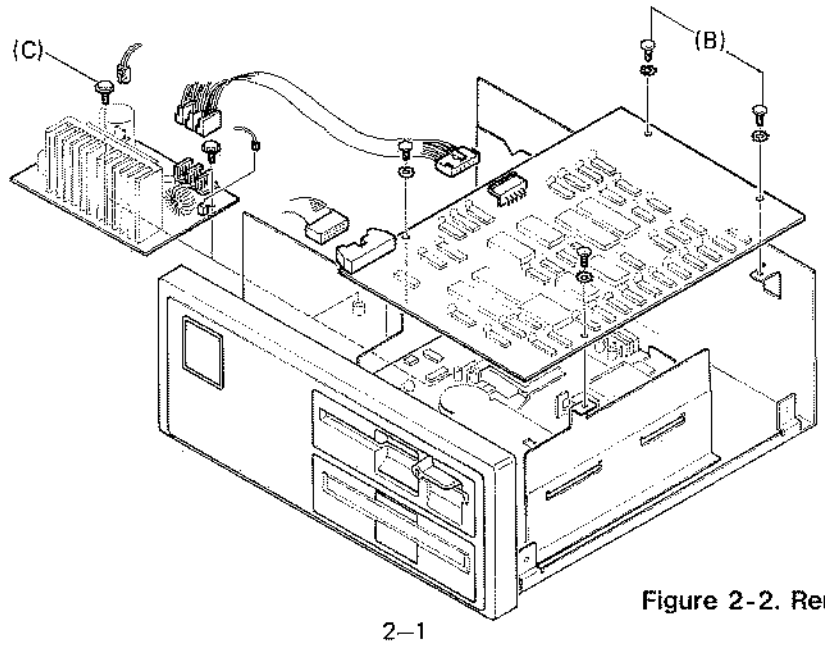


Figure 2-2. Removal of P.C. Boards

Disk Drive Unit

1. Disconnect the two connectors marked CN-2 and CN-4 on the floppy disk control P.C. Board.
2. Remove the four screws (D) tightening the floppy disk supporting bracket.
3. Remove the floppy disk drive unit together with the floppy disk supporting bracket by sliding them toward the rear of the unit.
4. Remove the screws (E), two each on the left and right supporting brackets securing the floppy disk drive unit.

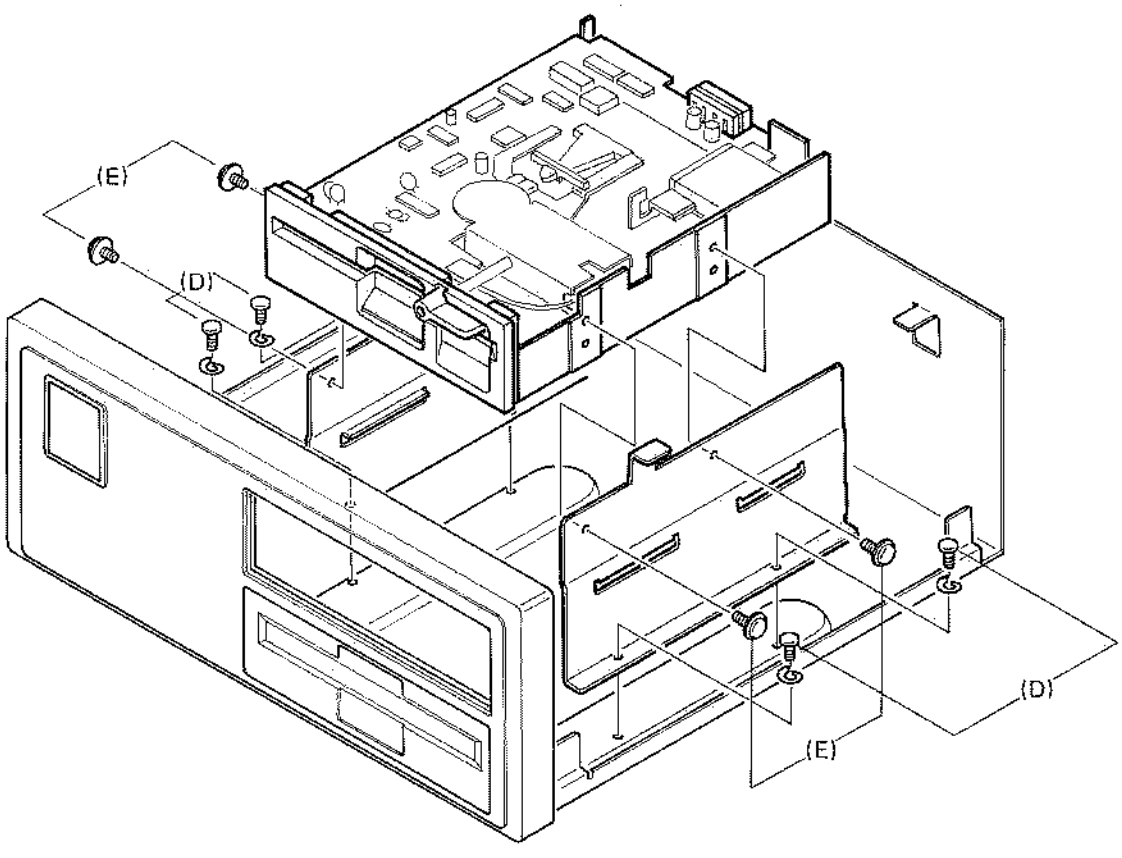


Figure 2-3. Disk Drive Removal

Front Panel Assembly

1. Remove the two screws securing the front panel assembly to the chassis.
2. Take out the front panel assembly by moving it toward the front of the unit. Be careful not to damage the three snaps securing the front panel assembly to the chassis.

3/Preventive Maintenance

To ensure the proper operation of the Disk/Video Interface, the only scheduled preventive maintenance required is periodic cleaning of the magnetic recording head.
Radio Shack's Universal Disk Drive head cleaning kit for 5-1/4-inch disks works well for this purpose. The kit includes two special cleaning disks and one bottle of cleaning solution.

Cleaning the Head

To clean the magnetic head, use a lint-free cloth or cotton swab moistened with 91% Isopropyl alcohol. Wipe the head carefully to remove all accumulated oxide and dirt.

CAUTION: Rough or abrasive cloth should not be used to clean the magnetic recording head. Use of cleaning solvents other than 91% Isopropyl alcohol may damage the head.

Extreme care must be exercised to prevent the head from being damaged (do not scratch or strike the head).

Adjustment

This section describes adjustment of the System Clock and Power Supply. When you are going to adjust the floppy disk drive, refer to Appendix C. Before adjustment, turn the power switch of the Disk/Video Interface on and load the DOS from the system diskette.

System Clock Adjustment

1. Connect the frequency counter to pin 3 of M11 on the Main PCB.
2. Adjust the C44 trimmer capacitor to read 16 MHz +0%, −0.3% (16 MHz to 15.952 MHz) on the frequency counter.

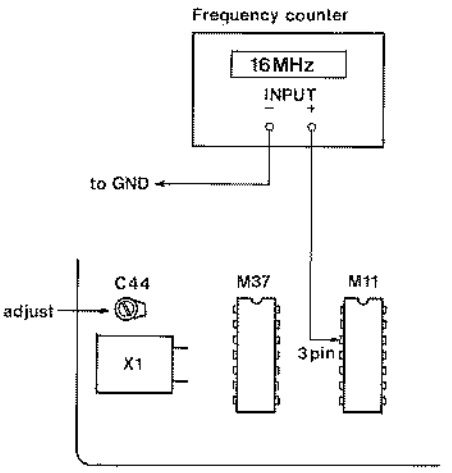


Figure 3-1. System Clock Adjustment

+5V Adjustment

1. Connect a DC voltmeter across pin 2 of CN4 (Ground) and pin 3 of CN4 (+5V) on the Main PCB.
2. Adjust VR101 on the Power Supply PCB to read +5V +0.1V, −0.1V on the DC voltmeter.

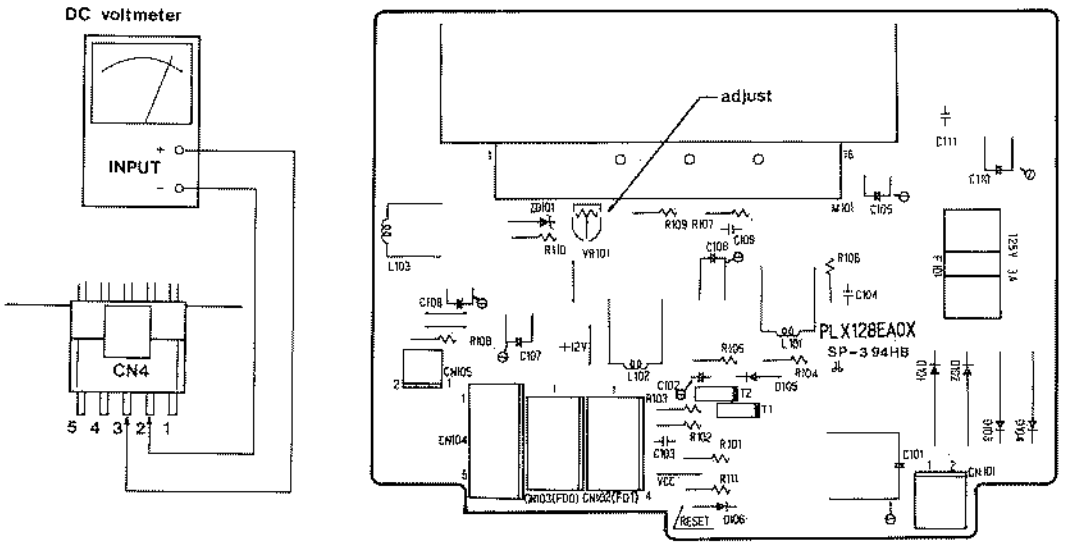


Figure 3-2. +5V Adjustment

4/Theory of Operation

The TRS-80 Disk/Video Interface uses a μPD780C (compatible with Z-80A) as the CPU.

The CPU controls the transaction of data or commands between the Portable Computer and the Disk/Video Interface by the PPI (8255), control of the CRT by the CRTC (HD46505) and control of the FDD by the FDC (M5W1793-02).

The memory consists of four sections:

- 4K bytes of P-ROM which store a program that reads the control program from track 1 of the system diskette (actual memory size used is 1K bytes).
- 4K bytes of RAM to store the control program read.
- 4K bytes of VRAM (Video RAM) to display characters on the CRT.
- 4K bytes of P-ROM to store the dot pattern of the characters (actual memory size used is 2 K bytes).

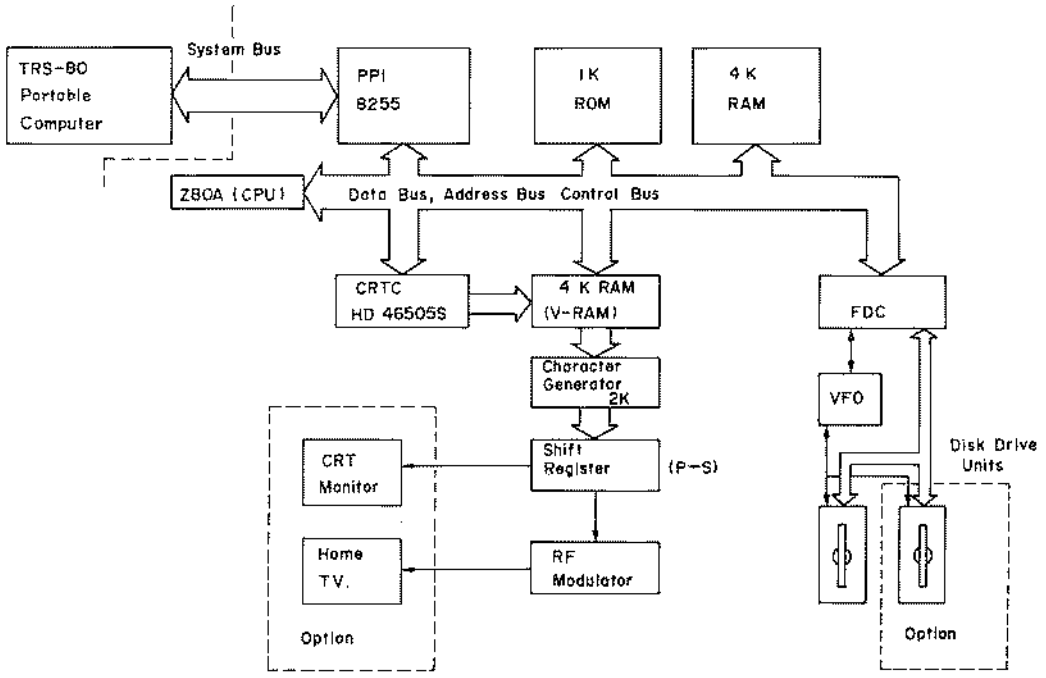


Figure 4-1. Block Diagram

This section provides circuit descriptions of the Disk/Video Interface, dividing it into the following eleven parts:

- CPU
- Address Decoding and Bank Selection Circuit
- Memory Map
- I/O Map
- Clock Generator Circuit
- System Bus Interface Circuit
- CRT Interface and Control Circuit
- Flicker Suppressing Circuit
- FDD Interface Signals
- FDD Control Circuit
- Power Supply and Reset Circuit

CPU

The CPU is a μPD780C compatible with the Z-80A.

System Clock: Uses 4-MHz clock. The clock generator circuit generates a 16-MHz clock and it is divided by four by M27 (SED9421C).

Data BUS and Address BUS: Connected to each memory and also used as the select signal and data BUS for the PPI, CRTC and FDC.

Interrupt: Two terminals, $\overline{INT}$ (Interrupt Request) and $\overline{NMI}$ (Non Maskable Interrupt), accept interrupts. By writing data into the PPI via the Portable Computer, $\overline{INT}$ is generated. The CPU receives the data from PPI by jumping to the Interrupt Handling Routine. $\overline{NMI}$ is used for accepting the completion of disk commands.

BUSRQ: $\overline{BUSRQ}$ is input from the Flicker Suppressing circuit. $\overline{BUSRQ}$ prohibits the CPU from accessing VRAM while the CRT is displaying characters and prevents flicker of the CRT.

RESET: RESET is generated in the power supply circuit and is used as a $\overline{RESET}$ signal for the CPU, ICs and LSIs.

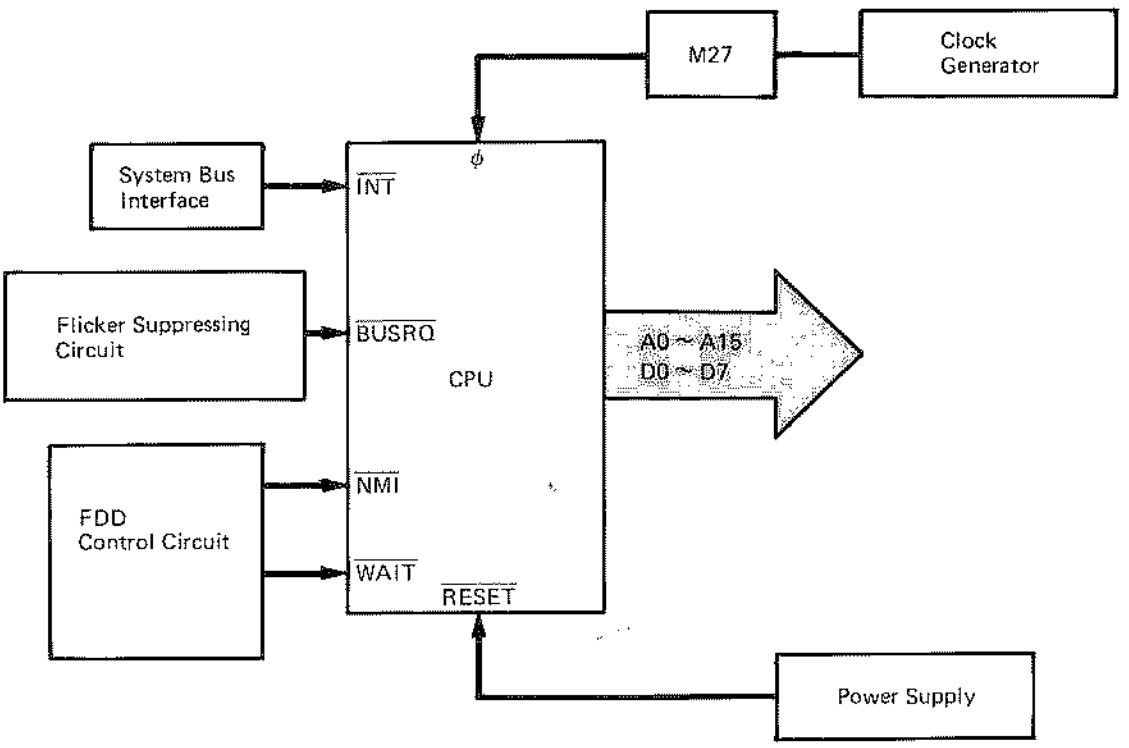


Figure 4-2. CPU Control Diagram

Address Decoding and Bank Selection Circuit

M31 and M38 determine memory address decoding. M31 decodes A15, A14 and A13, and selects ROM (M40), RAM (M28 and M36), ARAM (M23) and CRAM (M9).

The output of 2Q in M16 selects BANK switching. At power-on, M16 receives the $\overline{\text{RESET}}$ signal and BANK0 is assigned so that the program starts from address 0000H in the ROM. After that, the CPU assigns $\overline{\text{STS}}$ as the I/O Port and sets bit D1 of the data bus to "H", and the BANK1 is selected.

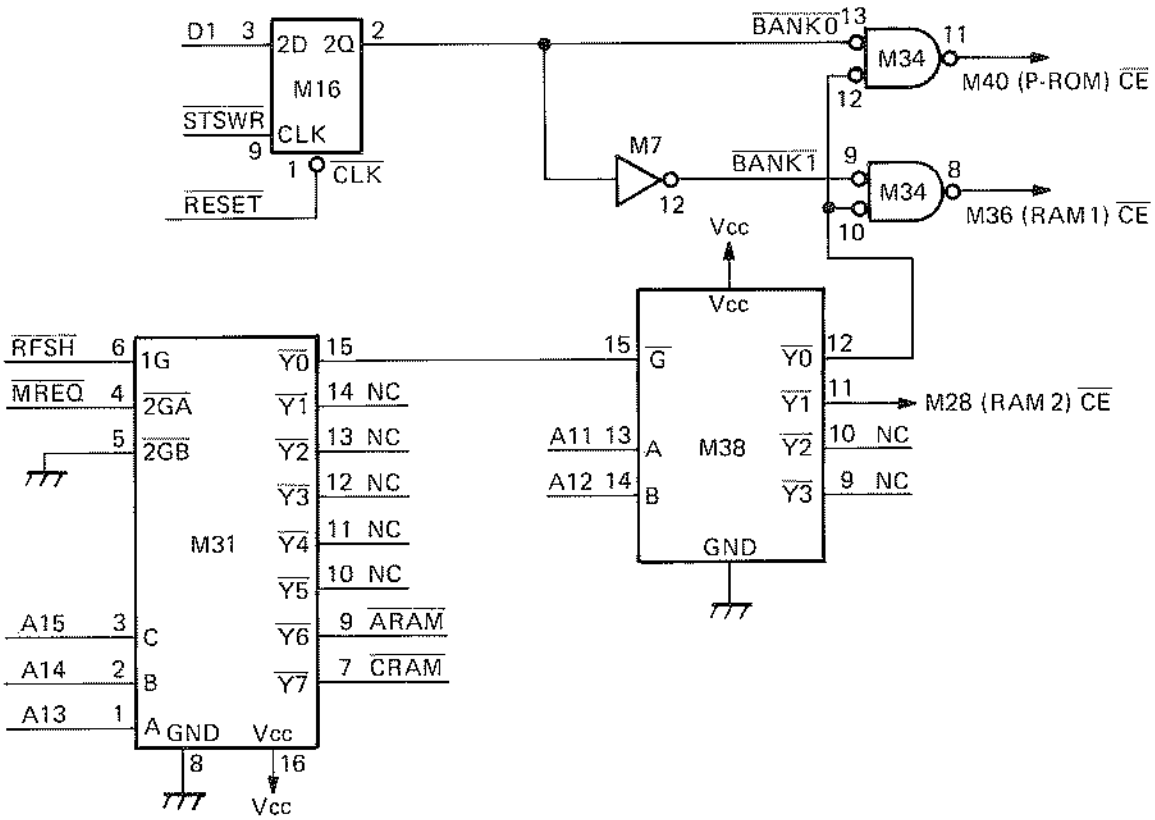


Figure 4-3. Address Decoding and BANK Selection Circuit

Memory Map

The Disk/Video Interface uses two 4K-byte P-ROMs and four 2K-byte Static RAMs.

At power-on, the P-ROM program is used to load the control program from the system diskette, but as the address codes A10 and A11 are connected to ground through R25 and R28, memory is 1024 bytes.

Another P-ROM is used as a character generator and accessed by the CRTC. Two 2K-byte RAMs, RAM1 and RAM2, are assigned for the control program.

Two other RAMs are CRAM (Character RAM), which stores data to display on the CRT, and ARAM (Attribute RAM), which stores data to reverse and blink characters.

A P-ROM for the program and RAM1 are switched by the BANK selection circuit. At power-on and while track 1 of the system diskette is being read, the combination of RAM2 and BANK0 P-ROM is selected. After the system has been read, the combination is switched to RAM2 and BANK1 RAM1.

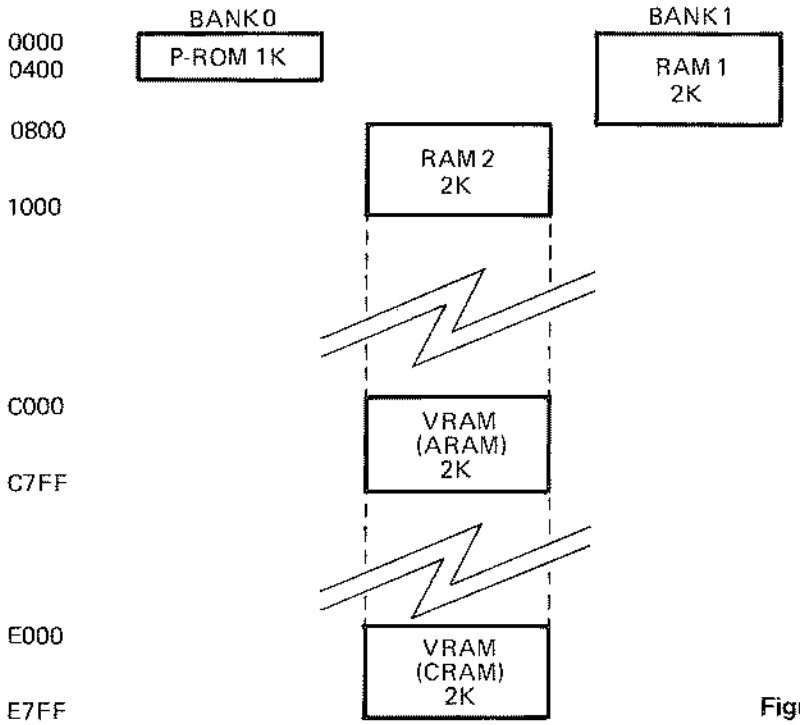


Figure 4-4. Memory Map

I/O Map

Selection of an I/O Port is determined by M38 by decoding the address of A5, A6 and A7. There are four I/O ports:

Address	Signal	Description
00H ↓ 1FH	$\overline{CRTC}$	00H: Address Register of CRTC 02H: Command Register of CRTC (for Write) 03H: Status Register of CRTC (for Read)
20H ↓ 3FH	$\overline{STS}$	20H Bit / Read / Write 0 — PPI PB0 — Select 80 characters mode 1 — PB1 — Select Bank 1 2 — PB2 — Not Used 3 — PB3 — Not Used 4 — PB4 — Select Drive 0 5 — VSRET — Select Drive 1 6 — IBF — Half CPU if VSRET is High 7 — MOTOR ON — Enable head
40H ↓ 5FH	$\overline{FDC}$	50H: Status Register of FDC (for Read) 50H: Command Register of FDC (for Write) 51H: Track Register of FDC 52H: Select Register of FDC 53H: Data Register of FDC
60H ↓ 7FH	$\overline{8255}$	60H: Input from 8255 70H: Output to 8255

Table 4-1. I/O Port Description

Clock Generator Circuit

The clock generator circuit generates a 16-MHz clock and is used as the fundamental element for the system clock in the CPU, the timing clock for the FDD to read/write data and the timing clock for the CRT.

The 16-MHz clock, generated by M37 (NAND gate) and the 16-MHz crystal oscillator, is transferred to the FDD interface circuit and also transferred to M27 (SED9421C). This 16-MHz clock is divided by four by M27 and, passing through M14, it is transferred to the CPU as a 4-MHz clock. The CPU uses this clock as the system clock.

Also in M27, the 16-MHz clock is used as the timing clock to read/write data between the FDD. This 16-MHz clock is divided by two by M47 and the divided 8-MHz clock is supplied to the pre-compensation circuit in the FDD interface. The timing clock of the CRT is also generated by this circuit.

The fundamental factor of character display is DCLK. DCLK is a timing signal which shows 1 dot on the CRT. Every eight DCLK outputs one LOAD signal. LOAD is a timing signal which displays one character on the CRT.

There are two modes of character display; one is 40 characters per one line and the other is 80 characters per one line.

For the 80 characters mode, 1Q in M16 is set by the CPU and 80C becomes "L". Then M11 becomes preset so that the 16-MHz clock passes through M34 and M37, and is input into the CLK terminal of M33 directly.

For the 40 characters mode, at the gate of M34, 80C becomes "H" so that the 16-MHz clock is inhibited and divided by two in M11, and input into the CLK terminal of M33.

Because of this logic, display time of one character in 80 characters mode becomes half of that in 40 characters mode.

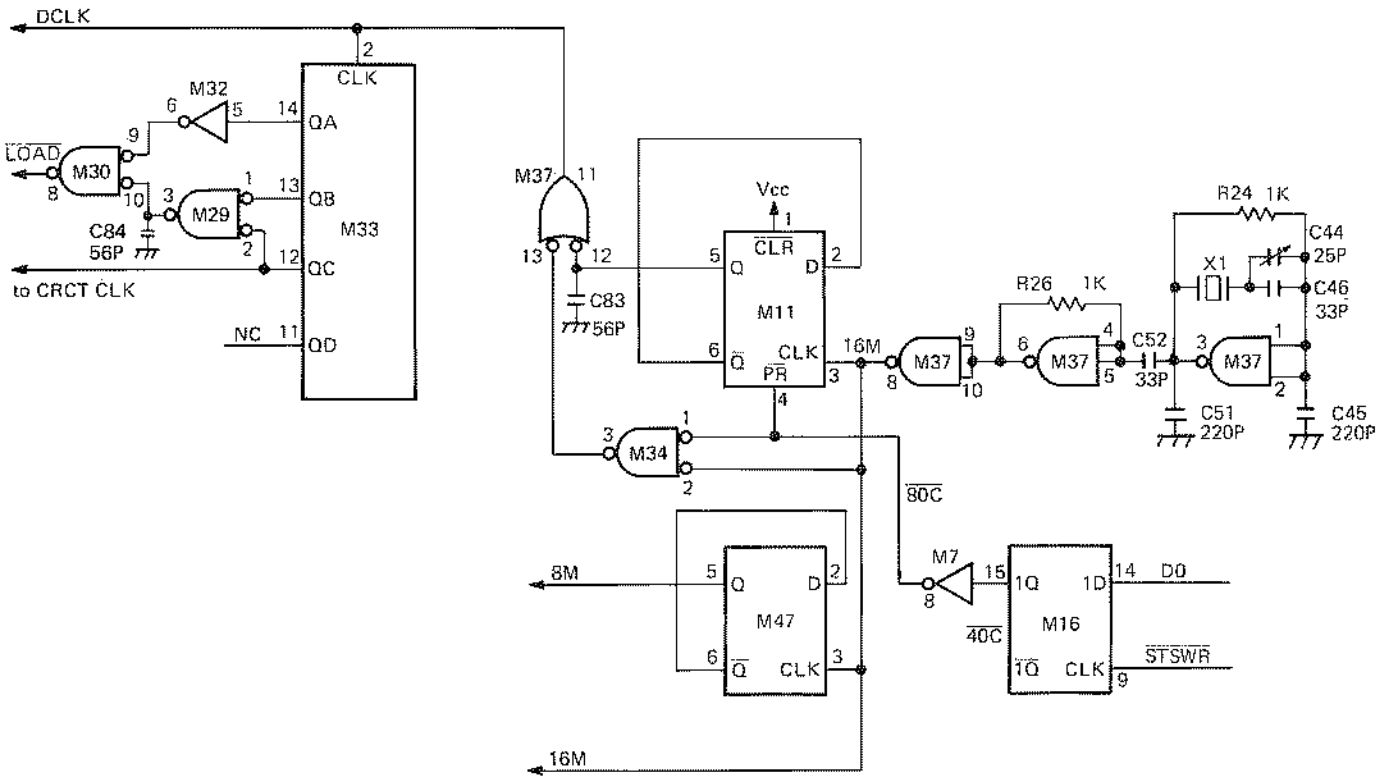


Figure 4-5. Clock Generator Circuit

System Bus Interface Circuit

Transaction of data or commands between the Portable Computer and the Disk/Video Interface is executed by M45, M41 and M44 under the control of the CPU.

The signals from the Portable Computer are as follows:

Signal name	Input or Output	Description
$\overline{Y0}$	Input	Chip select signal for PPI
A0	Input	Port select signal for PPI
A1	Input	Port select signal for PPI
$\overline{RD}$	Input	Allows the Portable Computer to read data from the PPI
$\overline{WR}$	Input	Allows the Portable Computer to write data and commands in the PPI ds in the PPI
D0 — D7	Input/Output	Data lines

Table 4-2. Signals from the Portable Computer

As soon as the DC voltage of the Disk/Video Interface reaches a proper level, RES signal becomes "L" and PC0, PC1 and PC2 terminals in the PPI also become low level. By checking the level of these 3 bits (whether they are "L" or not), the Portable Computer decides if the Disk/Video Interface is in an operable or inoperable mode.

1. Transmission of signals from the TRS-80 Portable Computer to the Disk/Video Interface

If you are going to transmit data from TRS-80 Portable Computer to the Disk/Video Interface, the Portable Computer checks $\overline{OBF}$ (Output Buffer Full) first. If this signal is "L", the Portable Computer waits until it becomes "H". As soon as the output buffer becomes empty ($\overline{OBF}$ = "H"), the Portable Computer writes data mode on the least significant 4 bits of Port B in the PPI.

This data mode is the data which define the going data whether they are commands or data, and to be transferred to the CRT or FDD and then, the data are written on the Port A in the PPI. Then, $\overline{OBF}$ becomes "L".

The $\overline{OBF}$ signal generates interruption in the CPU of the Disk/Video Interface. Through this interruption, the CPU acknowledges that the data is ready to be transmitted in the PPI, and then receives the data through PA0 — PA7 terminals in the PPI by switching the ACK (Acknowledge input) signal to "L".

Receiving the $\overline{ACK}$ signal from the CPU, the PPI switches $\overline{OBF}$ to "H", and reading $\overline{OBF}$ from Port C, the Portable Computer transfers the next data to Port A in the PPI.

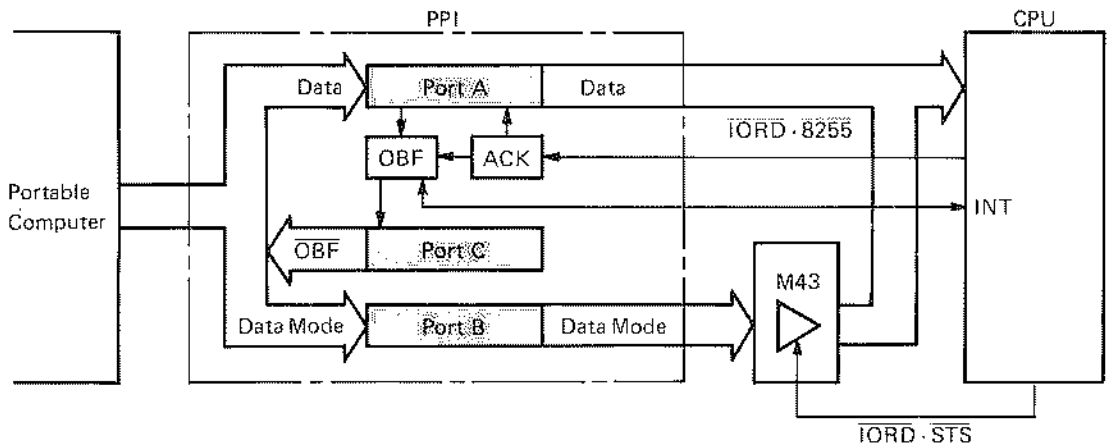


Figure 4-6. System BUS Interface Block Diagram (Receive Mode)

2. **Transaction from the Disk/Video Interface to the Portable Computer**

When the data is going to be transferred to the Portable Computer, the CPU waits until the IBF (Input buffer full) becomes empty (IBF = "L"). As soon as the IBF becomes "L", the CPU transfers the data to the Portable Computer to Port A and switches STB to "L".

Then, the IBF is switched to "H" and the data is latched in Port A in the PPI. The Portable Computer confirms IBF being "H" through Port C and accepts the data stored in Port A.

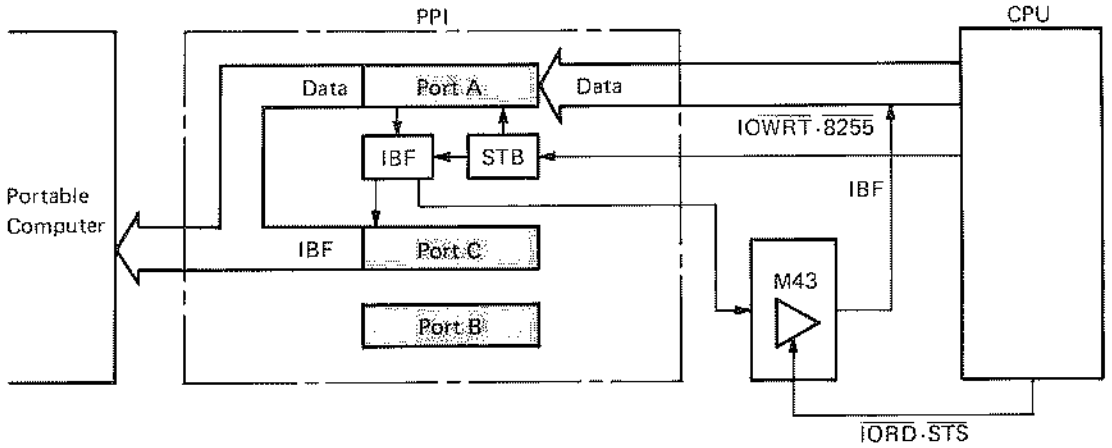


Figure 4-7. System BUS Interface Block Diagram (Transmit Mode)

3. **Data Modes**

There are four types of data transaction modes to transfer data between the Portable Computer and the Disk/Video Interface. The mode of data transaction is settled by the least significant four bits which the Portable Computer delivers to Port B in the PPI.

PB3	PB2	PB1	PB0	Data Mode	Remarks
0	0	0	0	CRT data	Data to be displayed on the CRT.
0	0	0	1	CRT screen copy	Transfers the contents of the VRAM to the Portable Computer.
0	0	1	0	Disk data	Read/write data to the disk.
0	0	1	1	Disk command	Commands or parameters to the disk.
1	1	0	0	I/O break	Stop of data transaction.

Table 4-3. PPI Function Table

CRT Interface and Control Circuit

The data to be displayed on the CRT is stored in the CRAM and the attribute data to show character reverse and blinking is stored in the ARAM. M20, M24 and M25 are the selectors of the address lines. When the CPU assigns VRAM, VRAM becomes "L" and, except for this case, CRTC assigns VRAM.

M9 is the ARAM data line selector and M22 is the CRAM data line selector. They connect the data BUS to the CPU only when ARAM or CRAM are assigned by the memory address of the CPU. Since ARAM uses only 2 bits of memory, D2-D7 terminals of M23 are pulled up on VCC.

When the VRAM is accessed by the CRTC, the data stored in the CRAM is latched on the rising edge of the LOAD signal in M18 and assigns A3-A10, which are address lines of P-ROM for the character generator.

On the other hand, to A0-A2 terminals of the P-ROM, RA0-RA2 signals are assigned from the CRTC. Through these address lines of the P-ROM, the character data varies with the raster address and is output from D0-D7 terminals of the P-ROM. M15 converts this parallel data to the serial data by one dot. M4 delays ARAM data by two pulses of the LOAD signal. When the character display is in reverse mode, M5 EX-ORs the ARAM data with the serial data and, in blinking mode, M2 ANDs the serial data with 1 Hz of signal which is generated by dividing VSYNC signal (about 60 Hz) from the CRTC by 64 in M8.

M2 ANDs the serial data with the DISPTMG signal from the CRTC and the ANDed signal is input onto the base of T1. At the same time, onto the base of T1, synchronous idle which M5 composes VSYNC (vertical sync) signal and HSYNC (horizontal sync) signal generated in CRTC is also input then, T1 generates composite video signal for CRT composing these two input signals.

When using a CRT monitor, this composite video signal is used directly; but for home TV sets, it is used after it is modulated to 61.25 MHz (channel-3) or 67.25 MHz (channel-4) through the RF modulator. The switch installed in the RF modulator controls switching of the modulation frequencies.

Table 4-4 shows the functions of the principal signals from CRTC.
Figure 4-8 shows block diagram of the CRT interface circuit.
Figure 4-9 shows the display timing chart at 40 characters mode and Figure 4-10 shows that at 80 characters mode.
Figure 4-11 shows the waveforms of video signal.

Symbol	Name of terminal	Description
HSYNC	Horizontal Sync	HSYNC is an active "H" level signal which provides horizontal synchronization for the displaying device.
VSYNC	Vertical Sync	VSYNC is an active "H" level signal which provides vertical synchronization for the display device.
DISPTMG	Display timing	DISPTMG is an active "H" level signal which defines the display period in horizontal and vertical raster scanning. The video signal should be "enable" only when DISPTMG is at "H" level.
CUDISP	Cursor display	CUDISP is an active "H" level video signal which is used to display the cursor on the CRT screen. This output is inhibited as long as DISPTMG is at "H" level.
RA0-RA4	Raster address	RA0-RA4 are raster address signals which are used to select the raster of the character generator.
MA0-MA13	Refresh memory address	MA0-MA13 are refresh memory address signals which are used to refresh the CRT screen periodically.

Table 4-4. Function of the Principal Signals

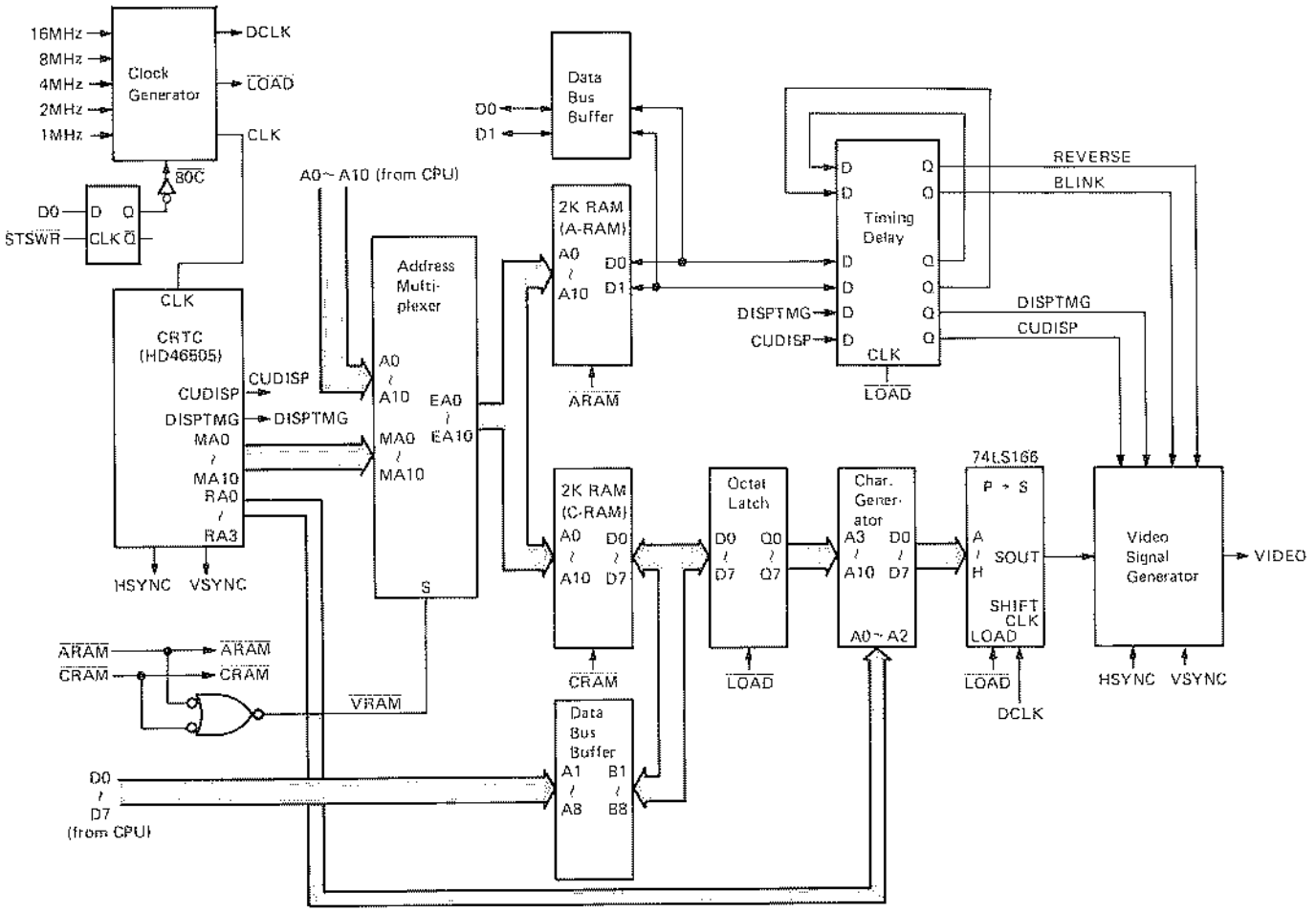


Figure 4-8. CRT Interface Block Diagram

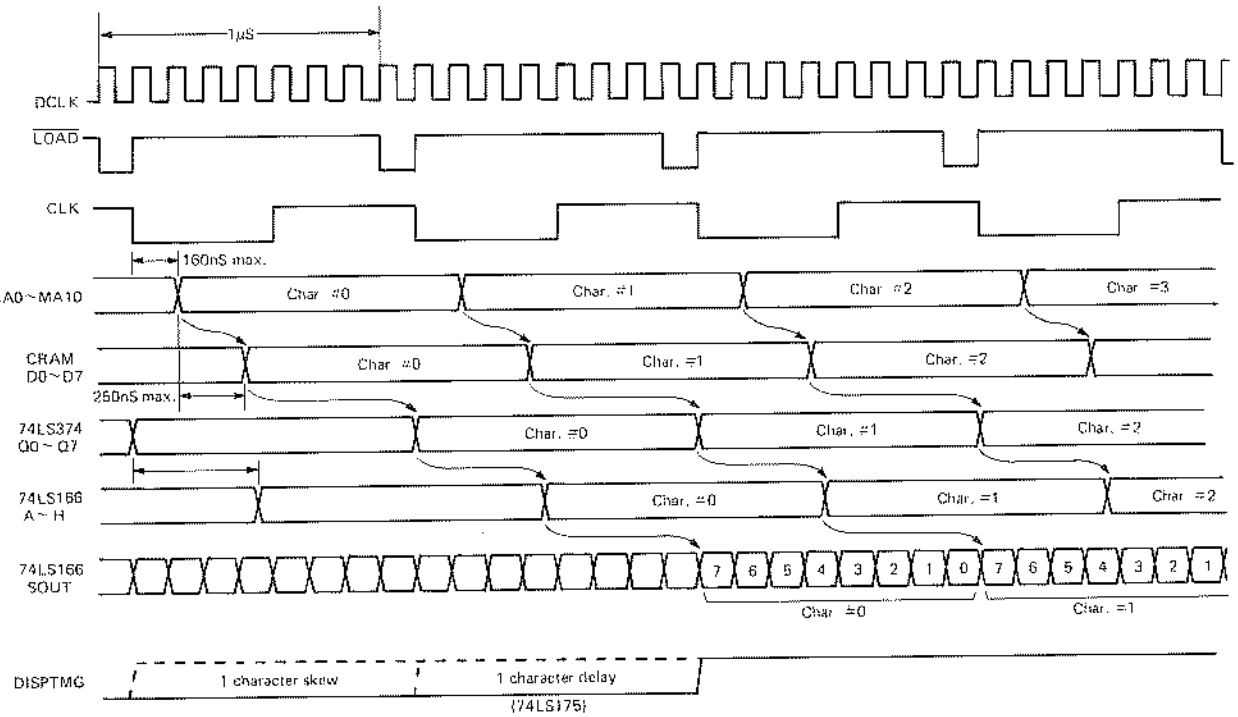


Figure 4-9. Display Timing Chart (40 Characters Mode)

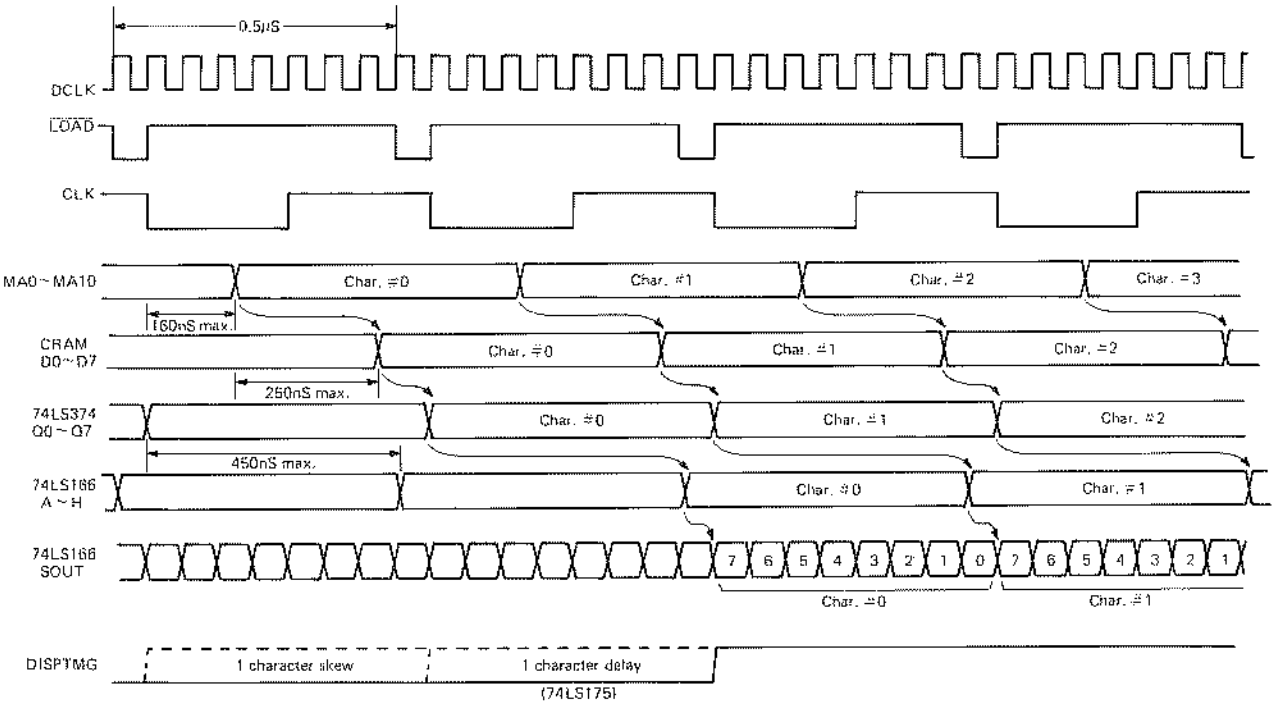


Figure 4-10. Display Timing Chart (80 Characters Mode)

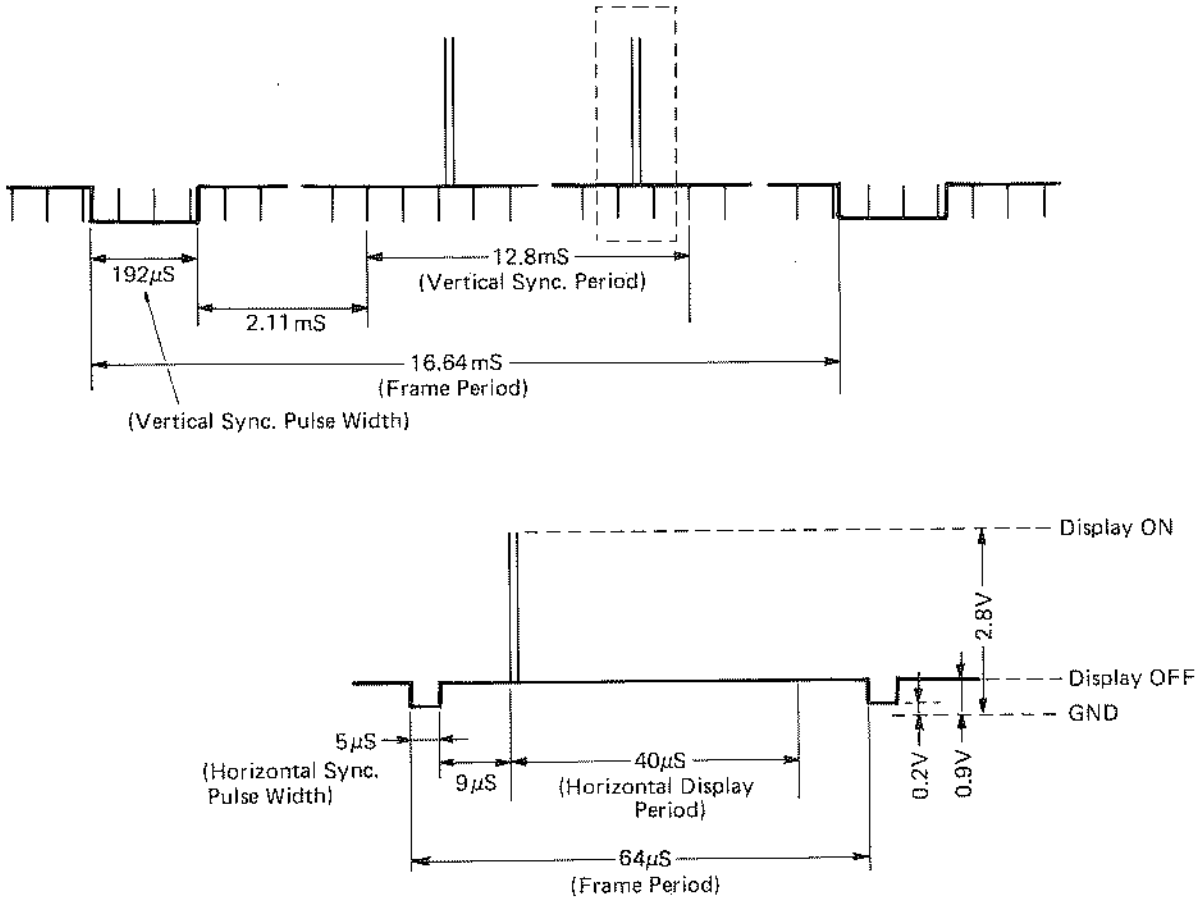


Figure 4-11. Waveform of Video Signal

Flicker Suppressing Circuit

As shown in Figure 4-12, during vertical retrace (during display), Q-output of M11 becomes "L"; otherwise, it becomes "H". For example, if the HLDEN signal is "H", $\overline{\text{BUSRQ}}$ becomes "L" so that the CPU is set in "wait condition" while displaying characters. This condition prevents the CPU from accessing VRAM during the vertical displaying period.

VSRET signal is read out of the gate of M29 into the CPU and, through this signal, the CPU can detect the condition of the display.

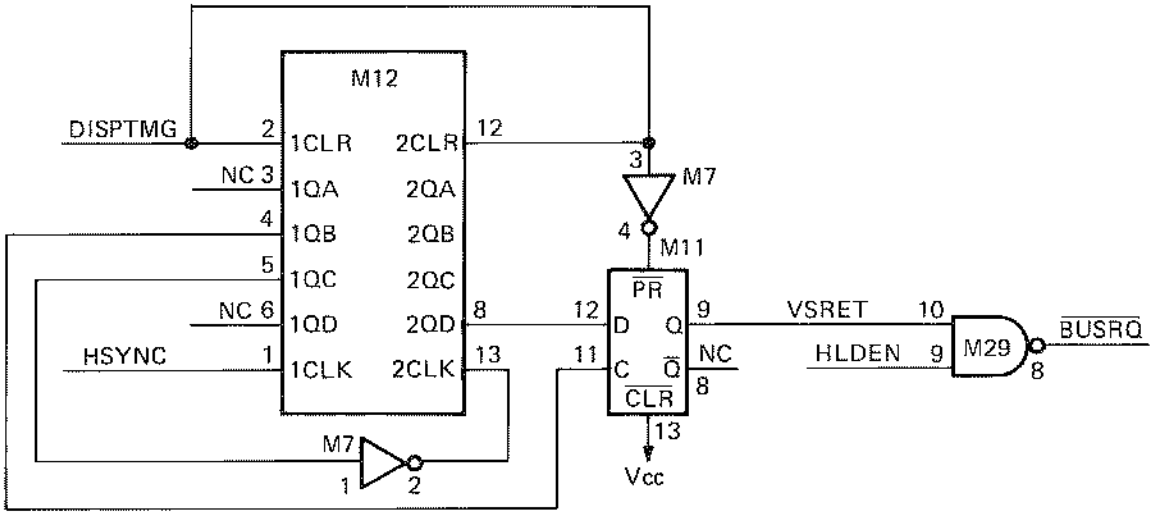


Figure 4-12. Flicker Suppression Circuit

FDD Interface Signals

Figure 4-13 shows the FDD (Floppy Disk Drive) interface block diagram. Each signal has a specified function for FDD.

1. **DRIVE0 and DRIVE1 (to FDD)**

   When either of the two input lines becomes "L", only the "L" signal drive can respond to the input lines, gate the output lines and turn the drive select LED on. DRIVE SELECT (0 or 1) is determined by plugging in the shorting plug.

2. **DIR (to FDD)**

   DIR is a control signal which defines the direction of motion of the R/W head. If the input signal is "L", the R/W head moves toward the center of the disk (STEP IN). If the input signal is "H", the R/W head moves towards the outside edge of the disk (STEP OUT). Direction change of the head motion must be made before the FDD receives a STEP pulse.

3. **STEP (to FDD)**

   STEP moves the R/W head by one track per one pulse. After receiving the final STEP pulse, the drive must wait at least "seek + settling" time to assure secure read/write.

4. **WG (to FDD)**

   "L" level signal allows the FDD to write data on the diskette. This signal becomes ineffective when WRITE PROTECT signal is "L" or the drive is not selected. "H" level signal allows the FDD to read the data stored on the diskette.

5. **WD (to FDD)**

WD provides the FDD the data on the diskette. Each transition "H" to "L" or "L" to "H" of MFM signal reverses the direction of the current through R/W head and writes a bit of data. This line becomes "enable" when WRITE GATE is "L", WRITE PROTECT is "H" and DRIVE SELECT is "L".

6. **MOTOR ON (to FDD)**

When this signal is "L", the spindle motor rotates and, when "H", it stops. The spindle motor reaches to the rated speed within 0.5 second. This line responds to the input signal regardless of the DRIVE SELECT signal.

7. **IP (from FDD)**

The "L" signal is provided by the drive every one rotation of the diskette indicating the beginning of the track.

8. **RDATA (from FDD)**

This line provides a "clock + data" pulse which is converted from analog data detected by the R/W head.

9. **TR00 (from FDD)**

Low state of this signal indicates that the R/W head is positioned at track 00.

10. **WPRT (from FDD)**

"L" signal indicates that a write protected diskette is installed in the FDD.

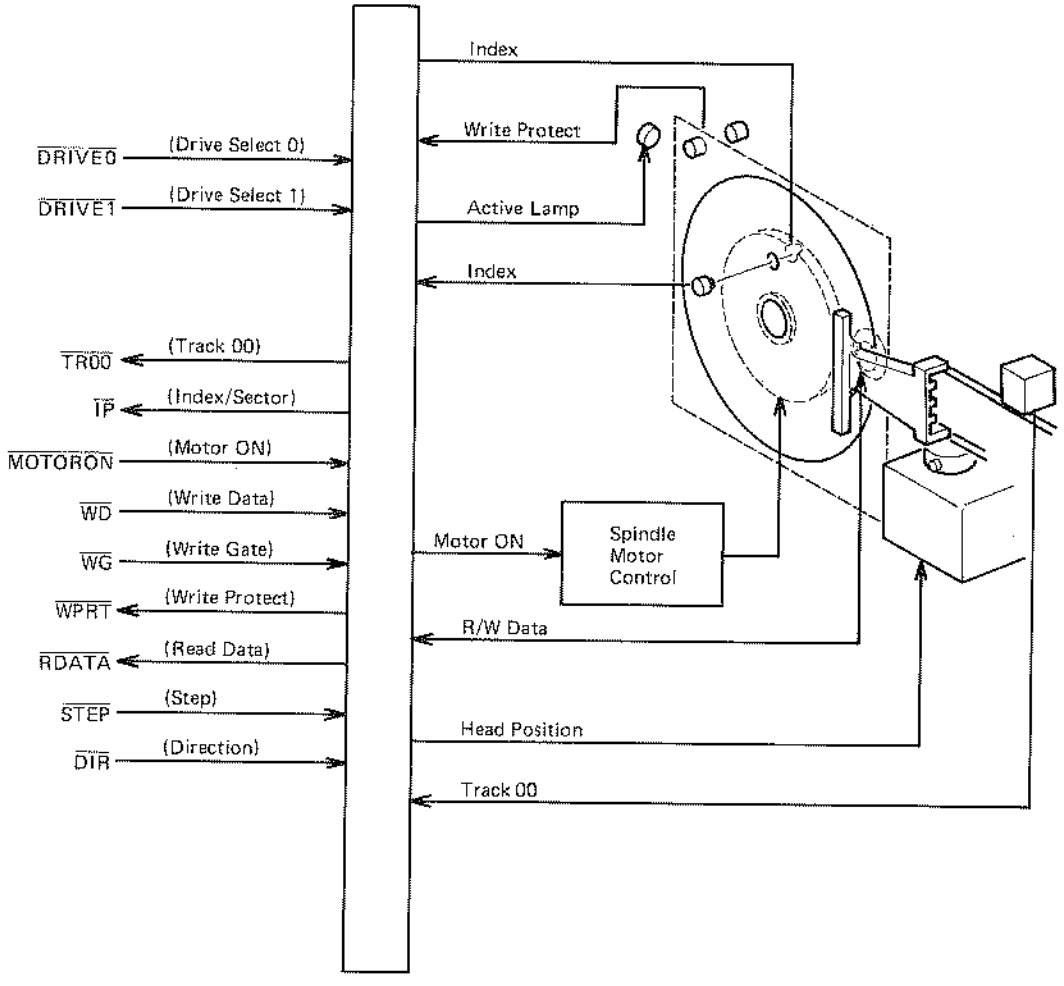


Figure 4-13. FDD Interface Block Diagram

FDD Control Circuit

FDD control circuit consists of FDC (M26), data separator (M27), pre-compensation circuit, and wait control circuit.

1. FDC (Floppy Disk Controller)

FDC consists of one LSI (M26) and, using D BUS, transfers commands and data corresponding to the FDD from the CPU. To detect the selection by the CPU, Y2 output signal ($\overline{FDC}$) by I/O port decoder M38 and A0/A1 signal are used. Combining these signals with $\overline{IORD}$ and $\overline{IORW}$ signals, FDC identifies the signals from the CPU as to whether they are the command, read/write data or request of status.

Table 4-5 shows the combination of the signals:

A0	A1	$\overline{IORD}$	$\overline{IOWR}$	Description
0	0	0	0	Reading of the status register
0	0	1	0	Writing onto the command register
0	1	0	1	Reading of track register
0	1	1	0	Writing onto the track register
1	0	0	1	Reading of the sector register
1	0	1	0	Writing onto the sector register
1	1	0	1	Transfer of read data
1	1	1	0	Transfer of write data

Table 4-5. FDC Function Table

The table below shows the functional description of the principal terminals. If you want to have additional information about this LSI, refer to the TRS-80 Model II Technical Reference Manual since this LSI is functionally identical to the 1791 used in the FDC Printer Interface Board of the Model II, except that the data BUS is true as opposed to inverted.

Symbol	Name	Input/Output	Description
DRQ	Data request	Output	In disk read mode, DRQ indicates that the data is assembled in the data register. In disk write mode, it indicates that the data register is empty. DRQ is reset by the read or write data operation.
IRQ	Interrupt	Output	IRQ becomes active at the completion request of command and is reset when the CPU reads the status or writes the command.
STEP	Step	Output	Step pulse output (Active high).
DIR	Direction	Output	High level means that the head is stepping in and low level means that the head is stepping out.
EARLY	Early	Output	This signal is used for write pre-compensation. It indicates that the write data pulse should be shifted early.
LATE	Late	Output	This signal is also used for write pre-compensation. It indicates that the write data pulse should be shifted late.
HLD	Head load	Output	This output signal controls the rotation of the motor of the FDD. The motor must be rotated by this high level output.
IP	Index pulse	Input	This input indicates that an index hole of the diskette is encountered.
TR00	Track00	Input	This signal tells the device that the head is located on track00. Active low.

Symbol	Name	Input/Output	Description
WPRT	Write protect	Input	Low level signal of this input informs the device that the drive is in write protect state. Before disk write operation starts, this signal is sampled and an active low signal terminates the current command, and sets IRQ. Write protect status bit in the status register is also set.
DDEN	Double density mode select	Input	This input determines the operation mode of the device. DDEN=0 selects double density mode.
RCLK	Read clock	Input	This signal is used internally for the data window. Phasing relation to the raw read data is specified, but the polarity (RCLK high or low) is not important.
RG	Read gate	Output	This signal shows the external data separation that the syncfield is detected.
RAWRD	Raw read	Input	This input signal from the drive shall be low for each recorded flux transition.
WG	Write gate	Output	This signal becomes active before disk write operation occurs.
WD	Write data	Output	This signal consists of data bits and clock bits. It becomes active for every flux transition.
RESET	Reset	Input	Active low. The device is reset by this signal and automatically loads "03" into the command register. The not-ready-status bit is also reset by this signal. When reset input is made high, the device executes restore command unless ready is active and the device loads "01" to the sector register.

Table 4-6. Description of the Principal Terminals

2. Data Separator (SED9421C)

SED9421C is an IC which generates a data window signal that separates clock bits and data bits among the data (RDATA) read out of the FDD. Figure 4-14 shows the functions of this IC.

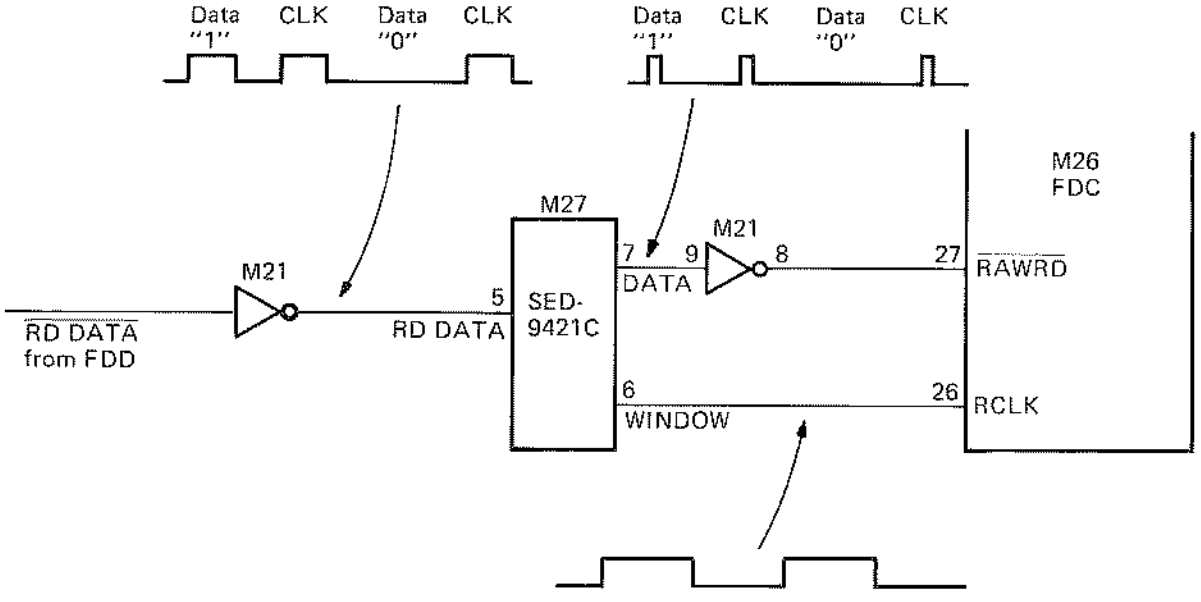


Figure 4-14. Data Separator

3. Pre-Compensation Circuit

This circuit adjusts timing of the write data delivered from FDC to the FDD. This circuit compensates data which will be shifted in writing since peak of the data may shift during data reading, depending on their data pattern.

The time available to compensate is 125 nanoseconds, i.e., one pulse width of 8 MHz.

In Figure 4-15, FDC outputs an EARLY or LATE signal, depending on the writing data pattern; then, D0, D1 or D2 terminals of M46 becomes "H" so that the number of flip-flops through which WD (write data) passes is determined.

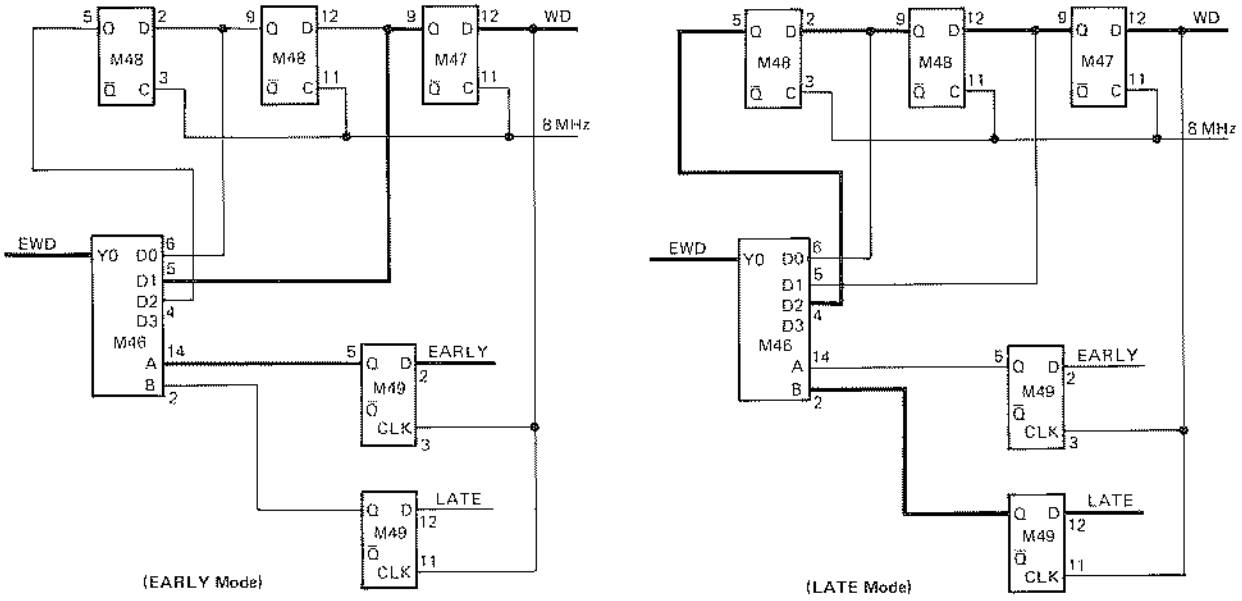


Figure 4-15. Pre-Compensation Circuit

4. Wait Control Circuit

As shown in the figure below, this circuit controls read/write data transaction between the CPU and the FDC.

During read operation, the CPU transfers a read command to the FDC setting A4="H" and FDC="L". Then, the CPU executes a dummy read operation once setting A4="L" and FDC="L".

At this time, Pin-9 of M1 becomes "L" and the CPU enters "wait condition". In this condition, as soon as the FDC reads the data from FDD and the buffer is filled by 8 bits of data, DRQ becomes "H", Q terminal of M1 becomes "L" and WAIT becomes "H". Then, the CPU releases "wait condition" and reads the data stored in the FDC.

The CPU repeats the above procedures and reads the data from the FDC continuously.

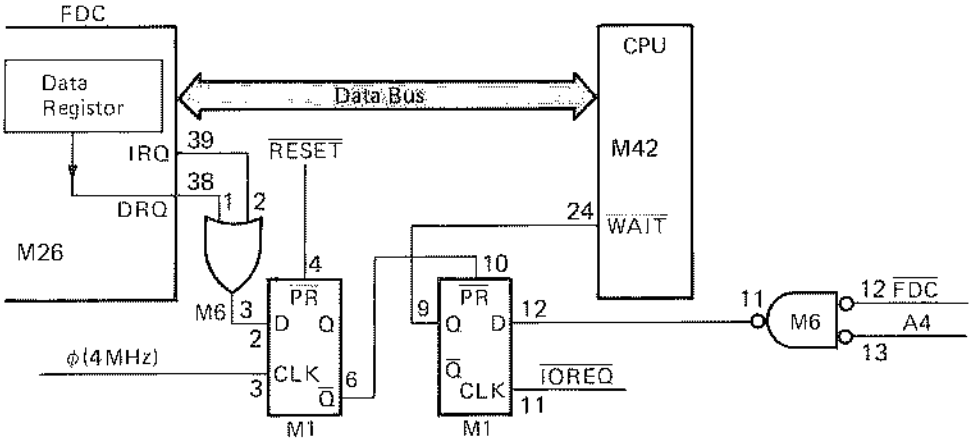


Figure 4-16. Wait Control Circuit

Power Supply and Reset Circuit

The power supply circuit consists of a regulator IC, capacitors, resistors, coils, and a diode (ZD101) determined for the reference voltage of VCC. This circuit generates +5-volt and +12-volt power — +12 volt is supplied to the FDD and RF modulator, and +5 volt is supplied to all of the ICs except M41 and M44 in the system BUS interface circuit.

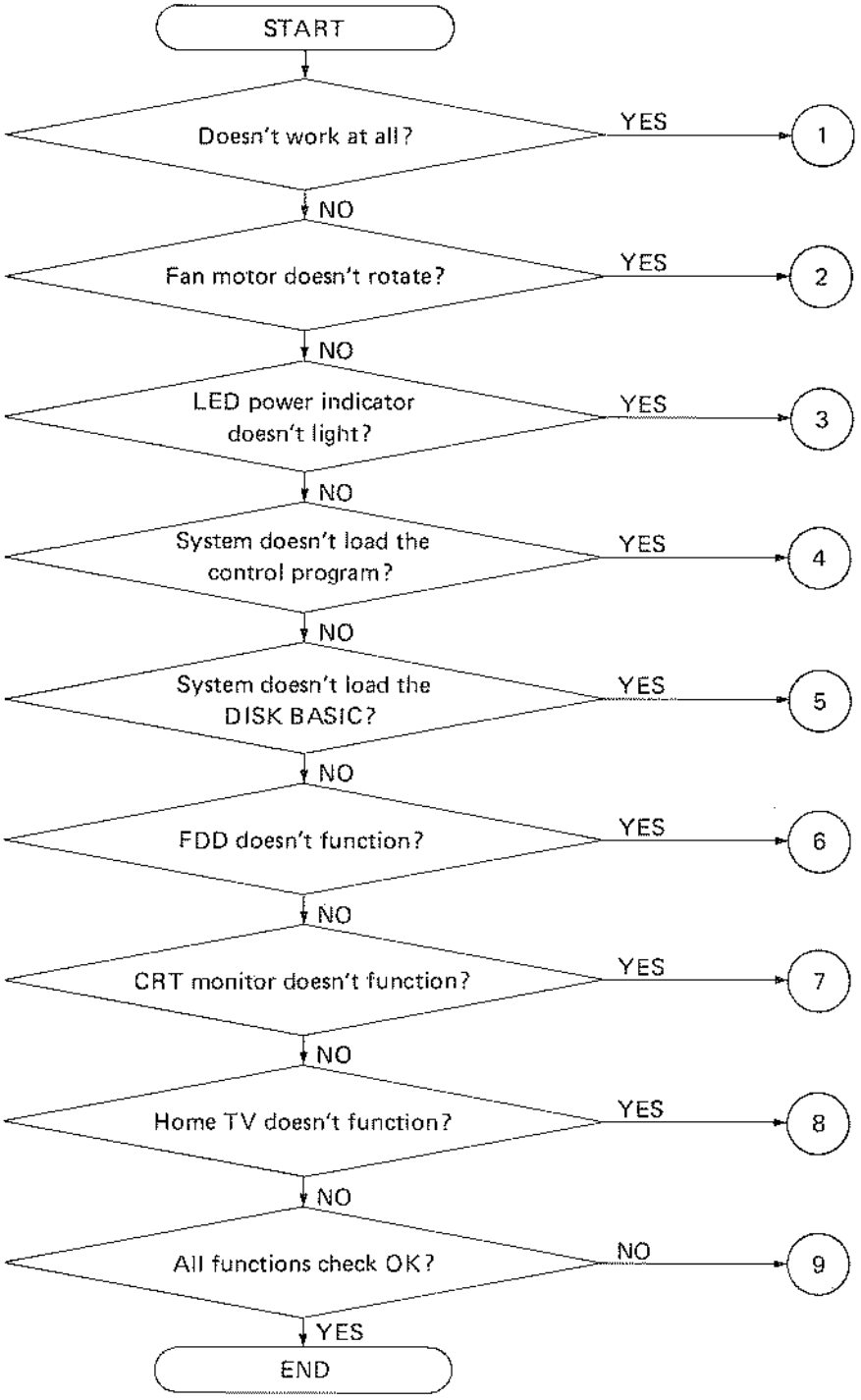
The RESET circuit consists of T101, T102, and the other components. T102 detects when the DC voltage reaches the proper level; R101 and T101 provide hysteresis to the RESET signal.

5/Troubleshooting

This section shows you how to go about solving a problem or malfunction that has been identified. All you have to do, is find the problem in the Troubleshooting Flowchart and refer to the section indicated by the number. Each section then identifies the components associated with the circuit in question and provides remedial instructions.

After completing any repairs, you should re-check each functional item according to the CHECK LIST. You can make use of the CHECK LIST even if the location and condition of the malfunction are not readily clear.

Troubleshooting Flowchart



Checking Procedure

1. Doesn't work at all.

(1)

Check the power.

1. Is the plug of AC cord plugged into the AC outlet?
2. Is the power switch ON?
3. Isn't the fuse blown? (It is in the fuse holder located on the rear side.)
   — If blown, check the power transformer and D101 – D104 and C101 on the Power Supply PCB unit. Then replace the fuse. (AC250V 1A)

Check the power supply circuit.

1. Isn't the fuse F101 blown?
   — If blown, check the resistance between pin 15 and pin 6 of M101. Then replace the fuse. (AC125V 3A)
2. Is 15 – 25V applied to the cathode of D101?
   — If not, check power transformer and D101 – D104.
3. Check output voltages.
   a) VCC . . . +5V ±0.25V
      If not, check ZD101, VR101, R107, R109, R110, C105, C107, C108, C109, L102, L103 and M101.
   b) +12V . . . +12V ±0.6V
      If not, check R106, C104, C105, C106, L101 and M101.

Check the RESET signal.

1. Is it high level (2.5 – 5.25V) at pin 10 of M21?
   — If not, check below.
2. Is the voltage at the collector of T102 low level (0 – 0.5V)?
   — If not, check R103, R104, R105 and T102.
3. Is the voltage at the cathode of D106 high level (4.5 – 5.25V)?
   — If not, check R102, R111, D106 and T101.
   If OK, check the cable from Power Supply PCB to Main PCB, C77 and M21.

Check the connection of all connectors.

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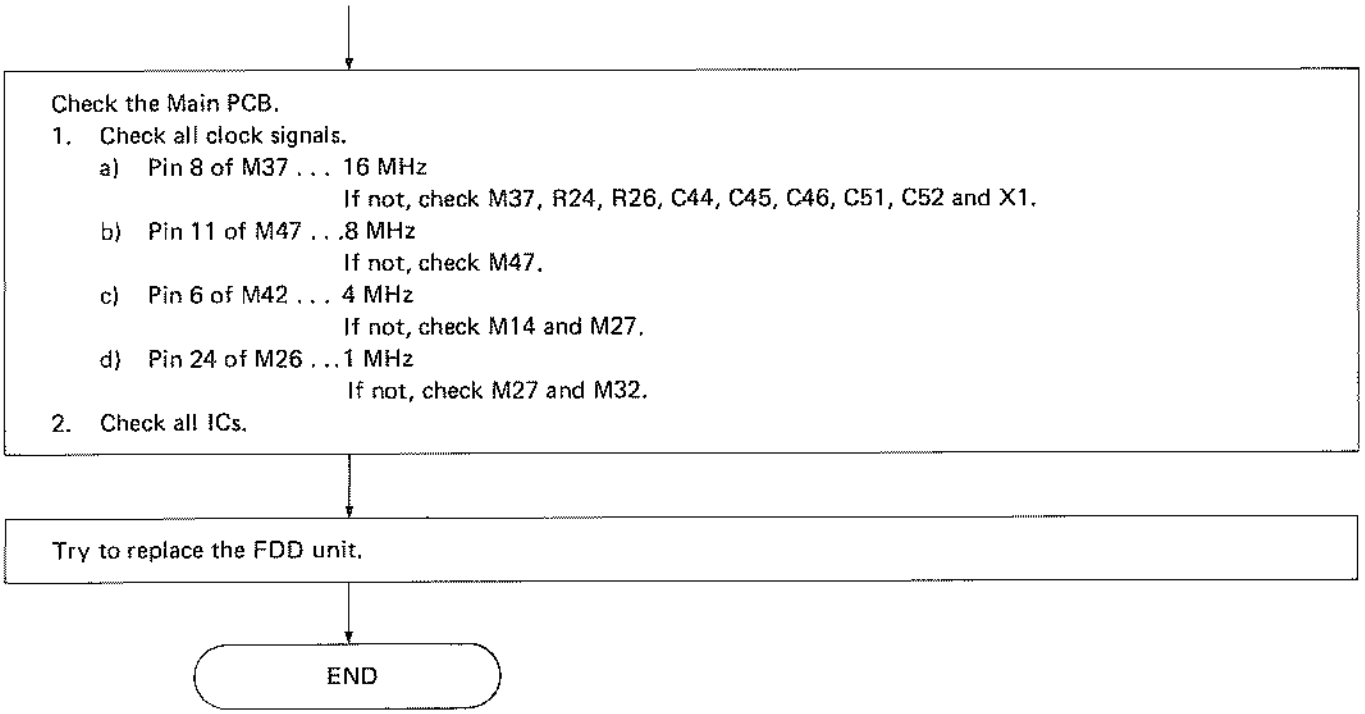
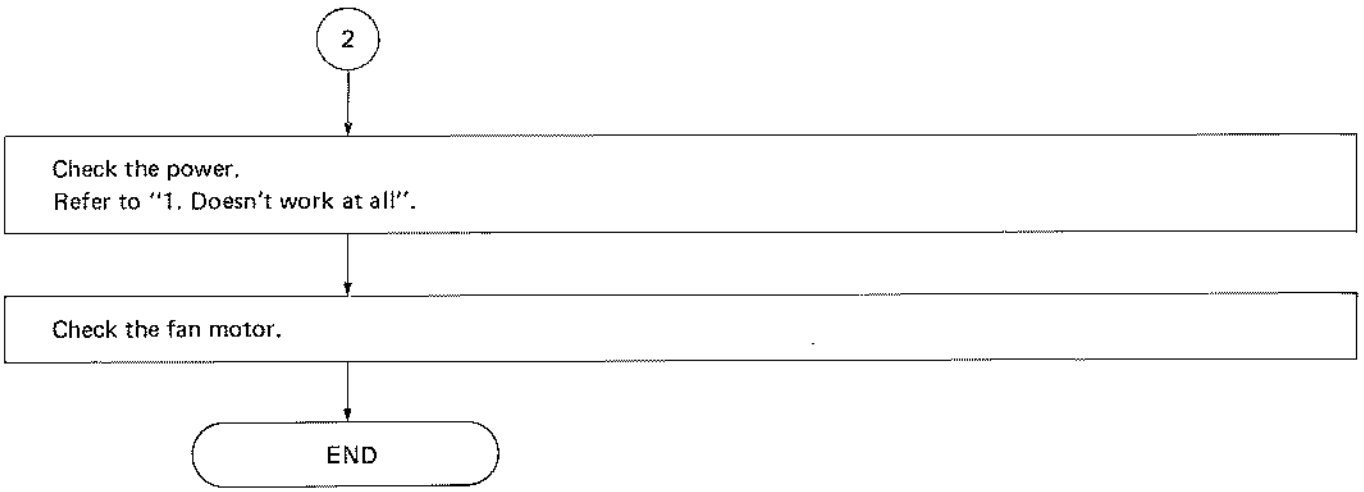
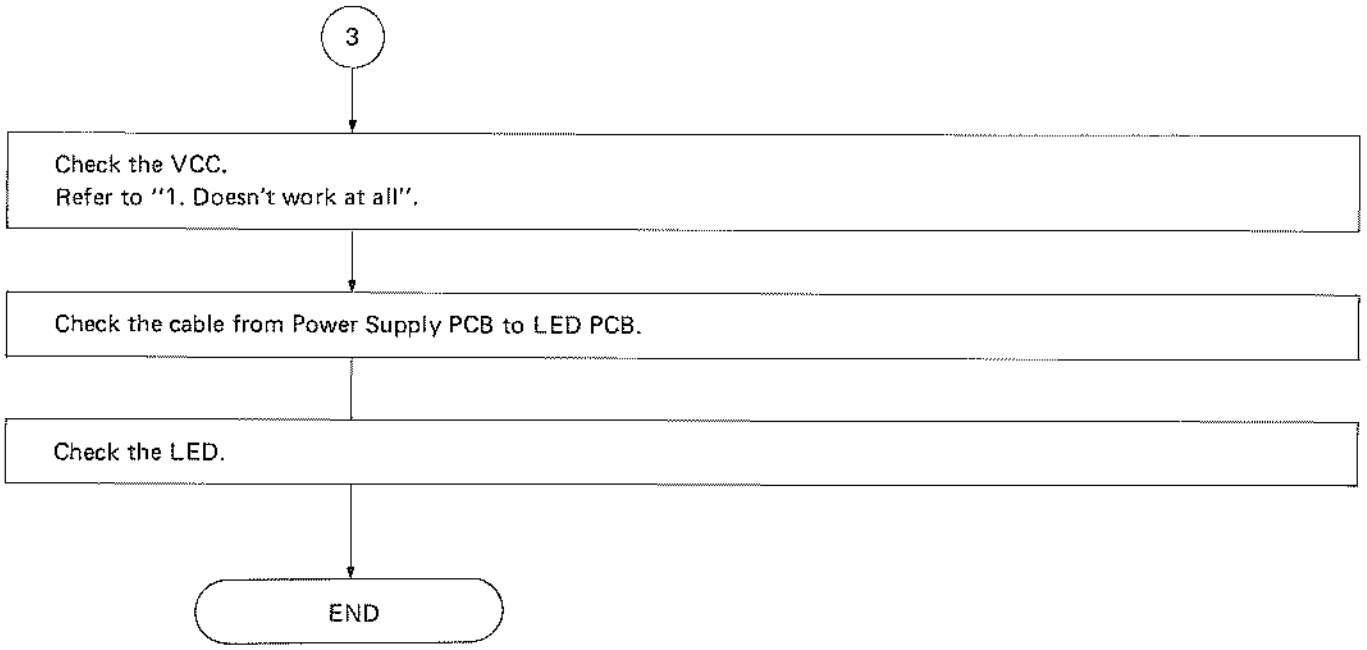


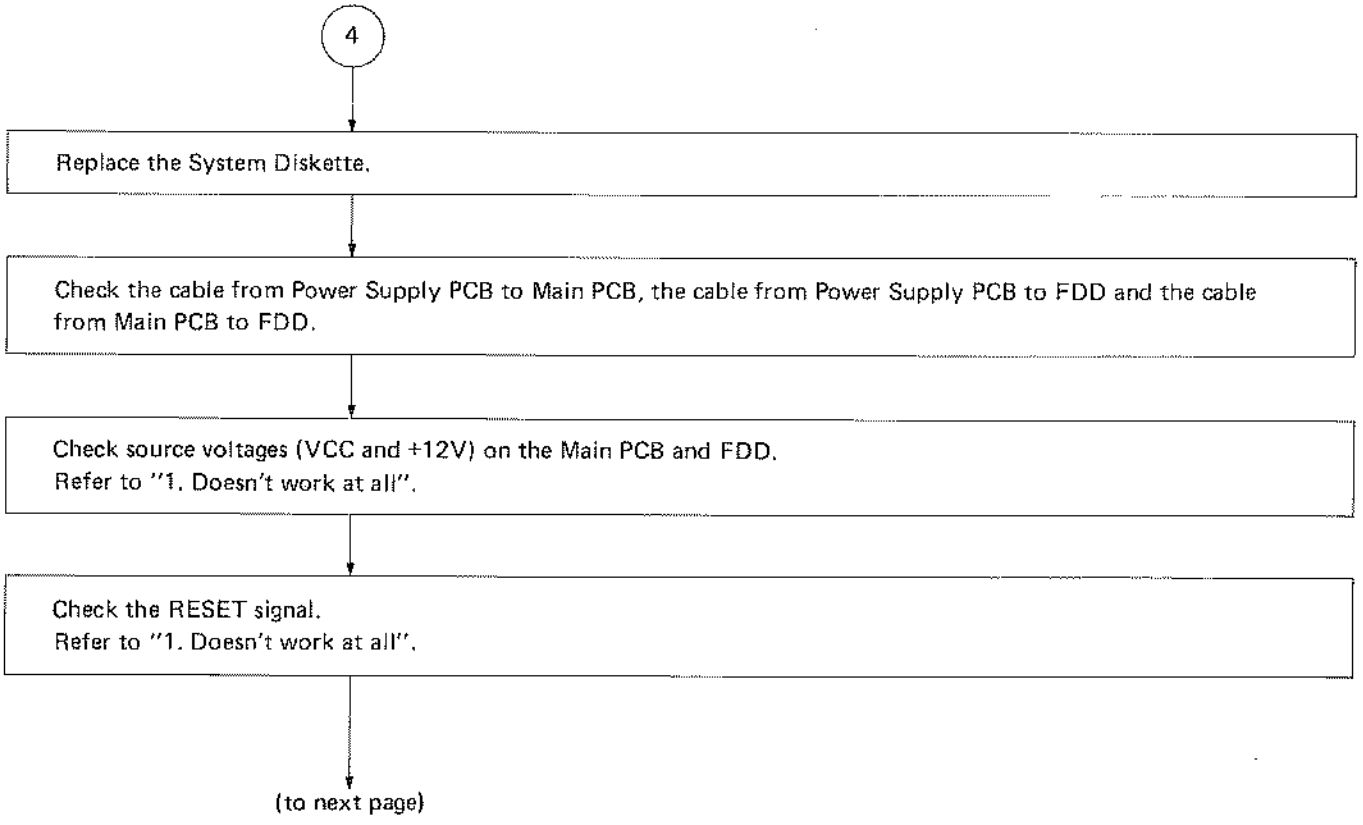
2. Fan motor doesn't rotate.

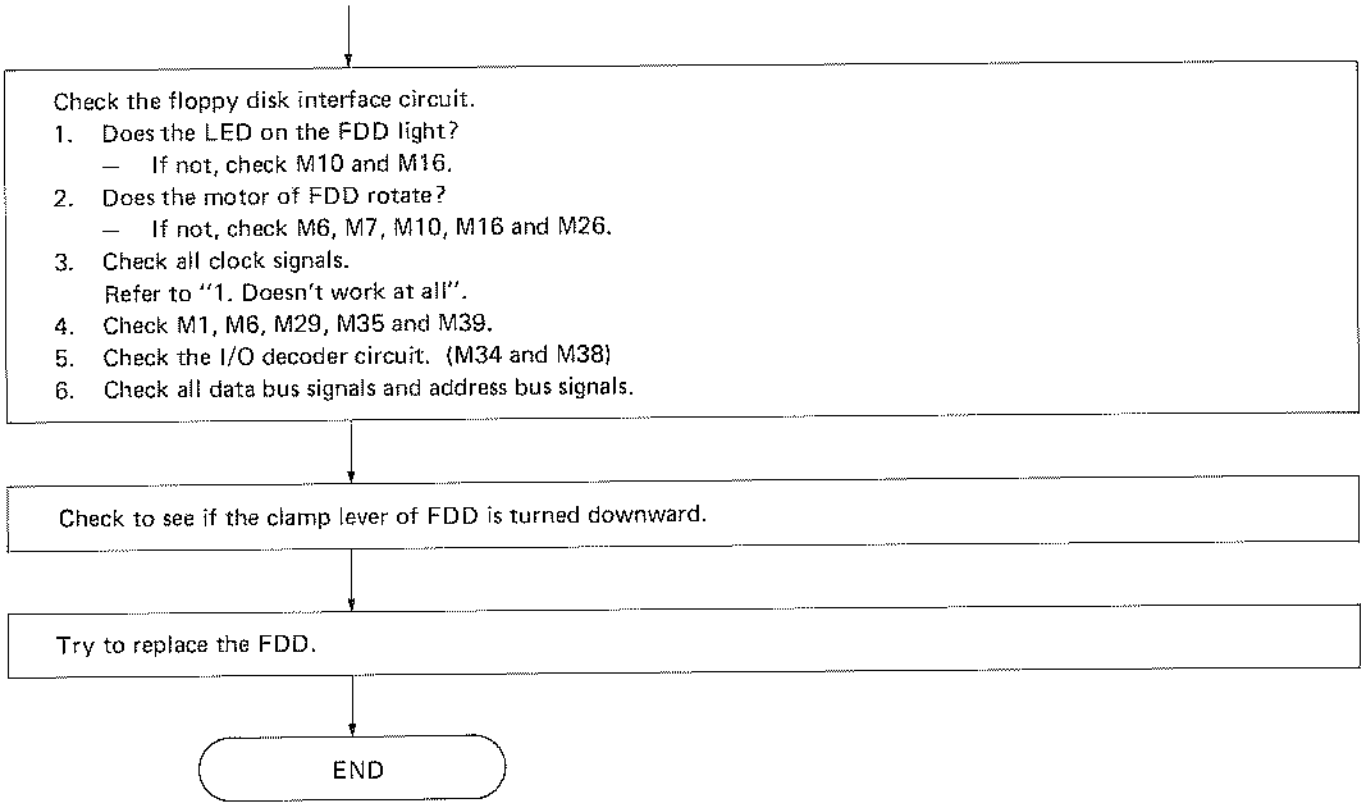


3. LED power indicator doesn't light.

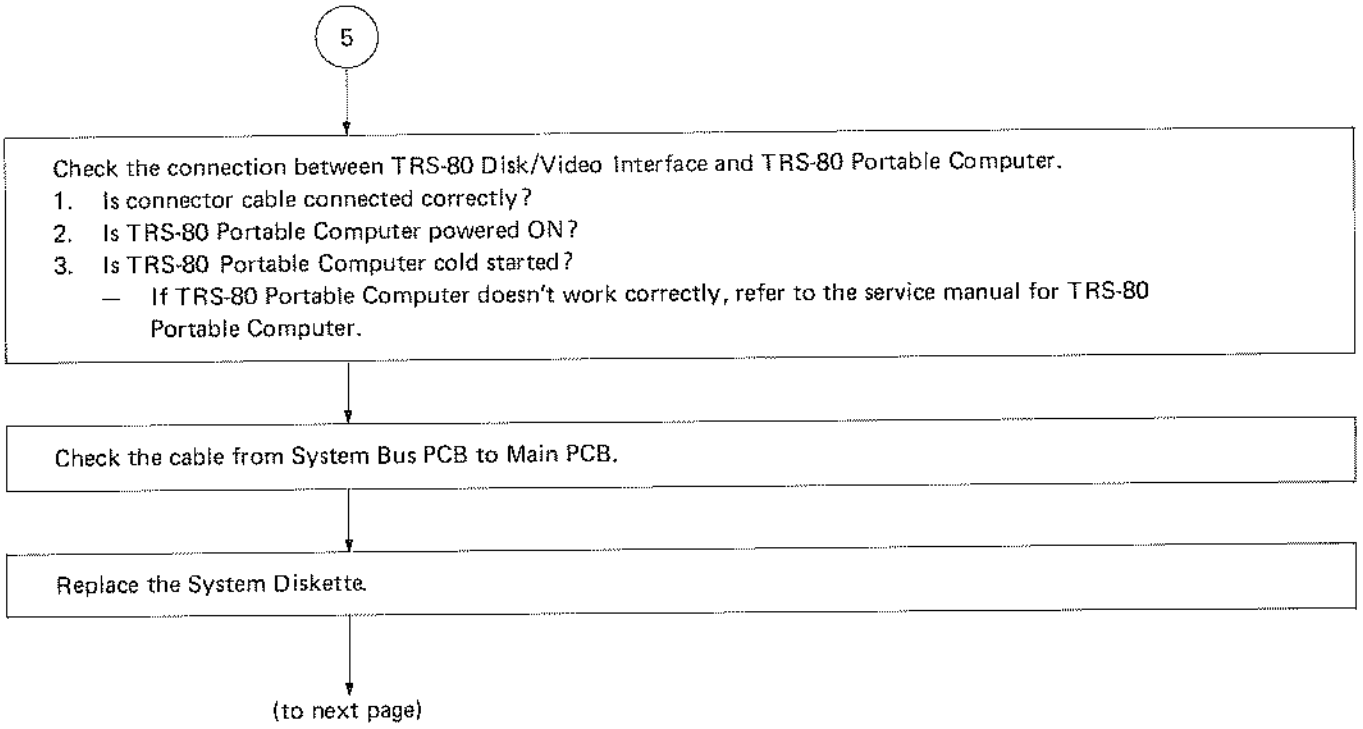


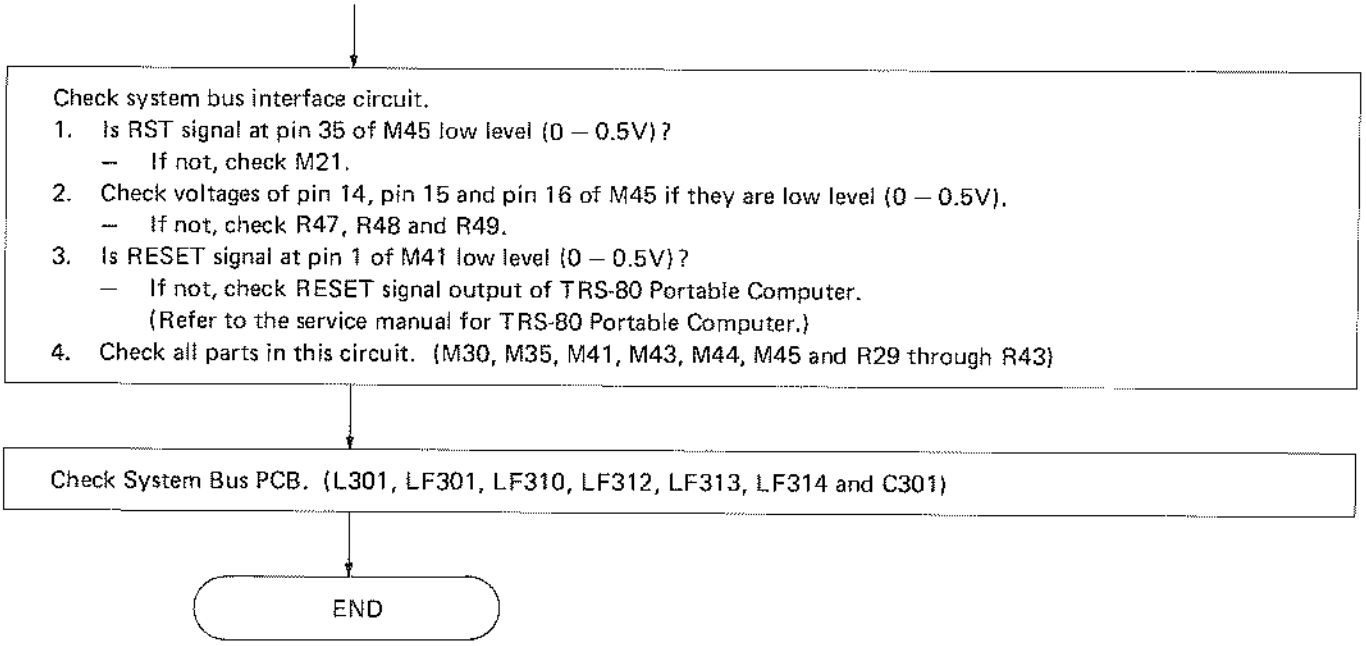
4. System doesn't load the control program.





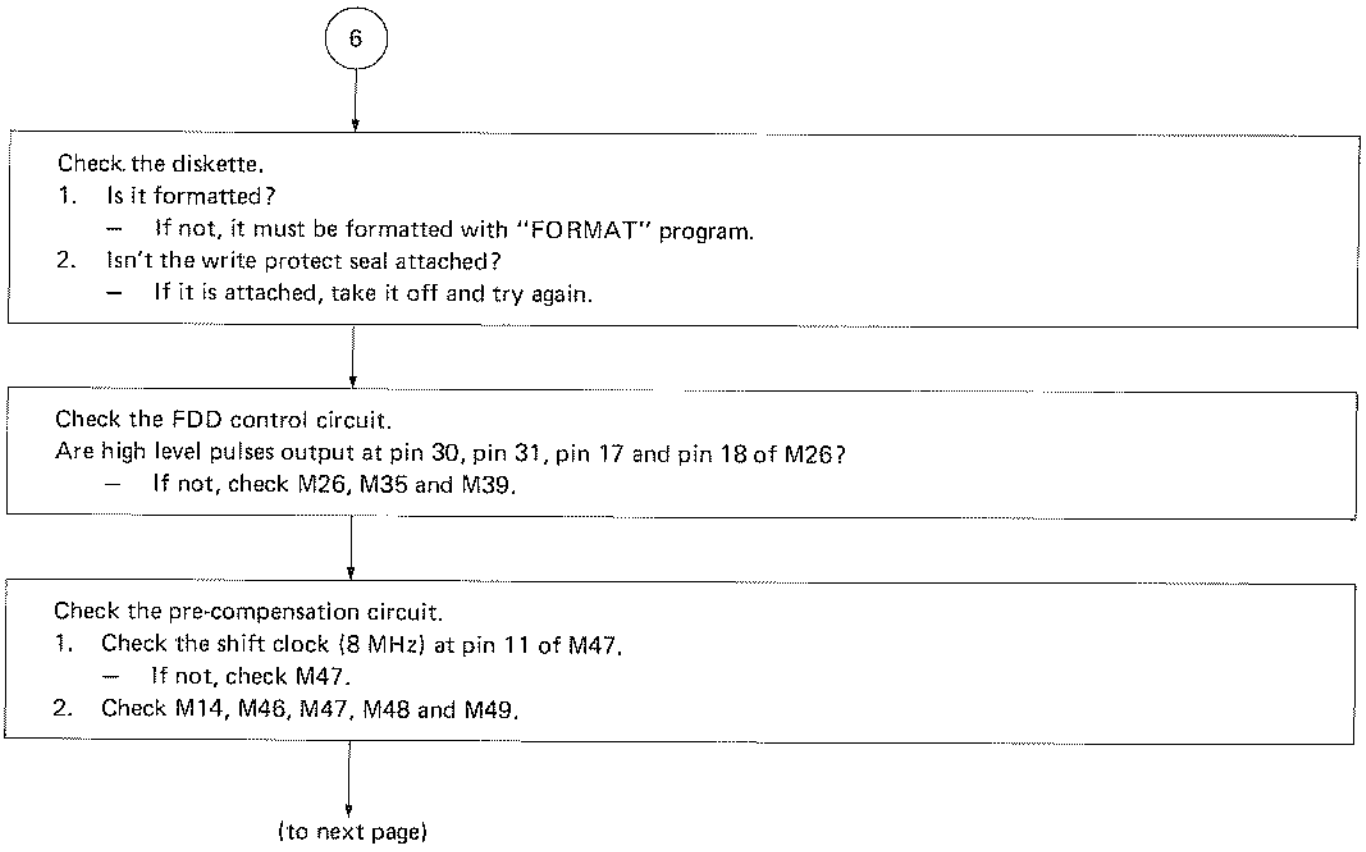
5. System doesn't load the DISK BASIC.

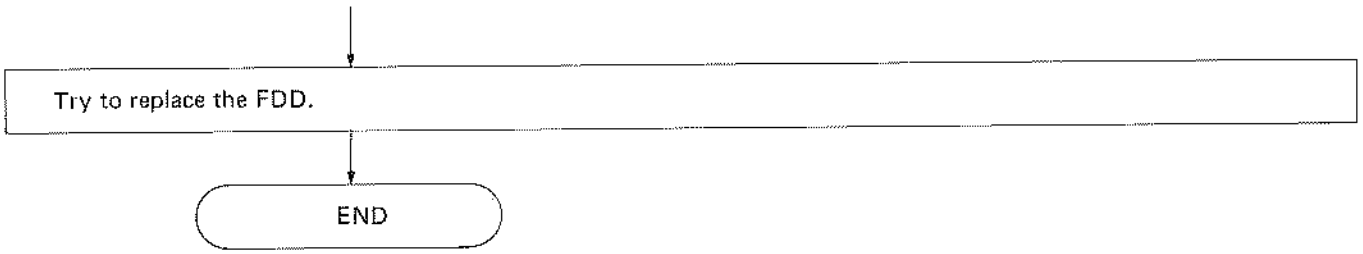




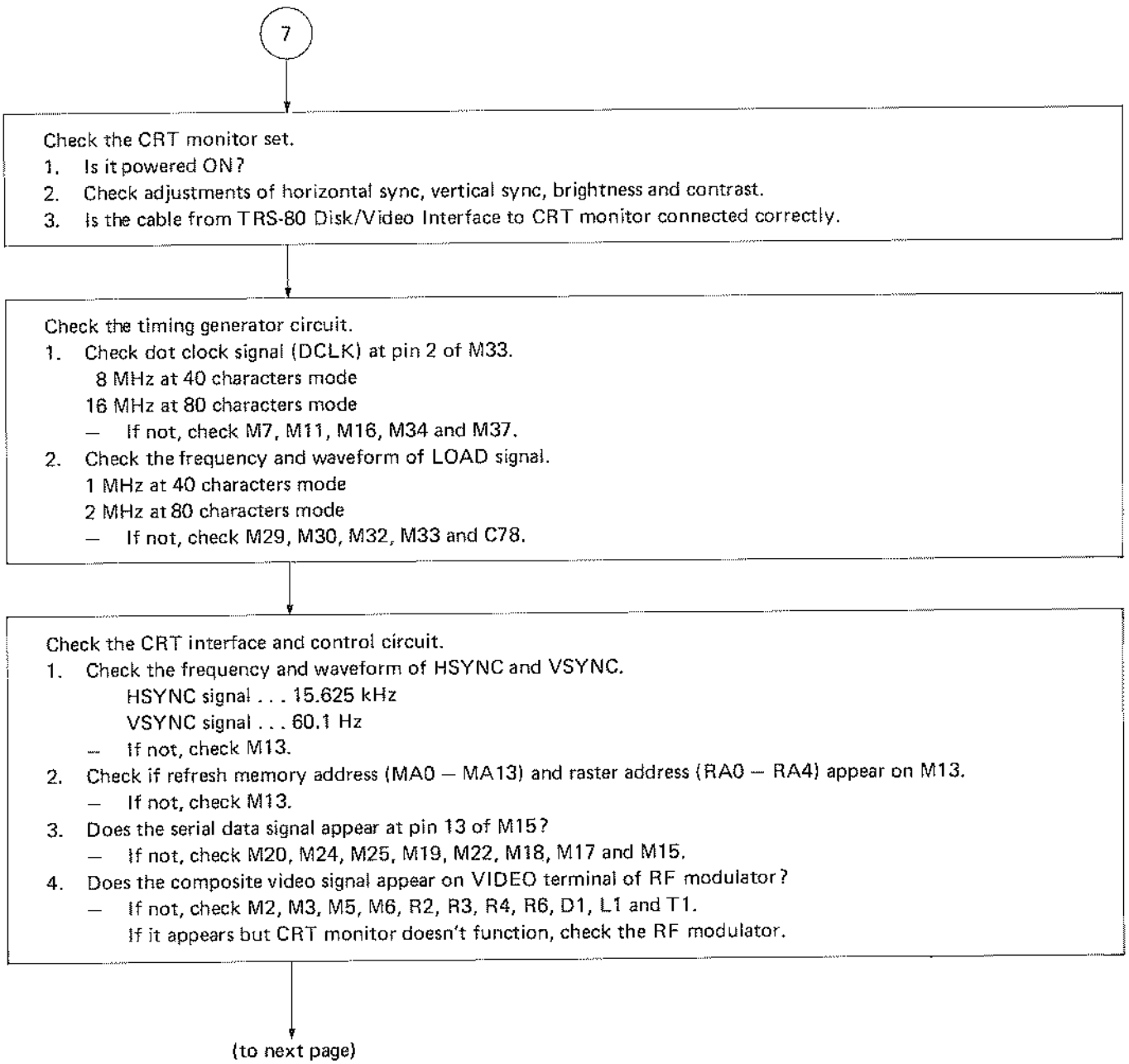
6. FDD doesn't function.

If system doesn't read the contents of the diskette, refer to "4. System doesn't load the control program" or "5. System doesn't load the DISK BASIC".
If system doesn't save data or program to diskette, check below.





7. CRT monitor doesn't function.



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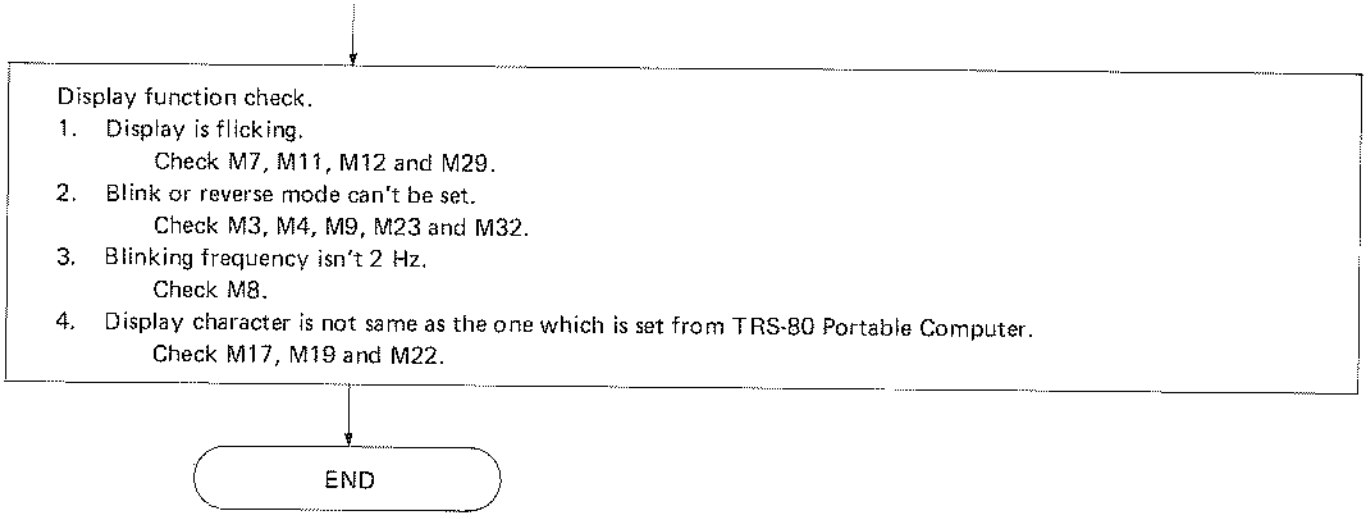
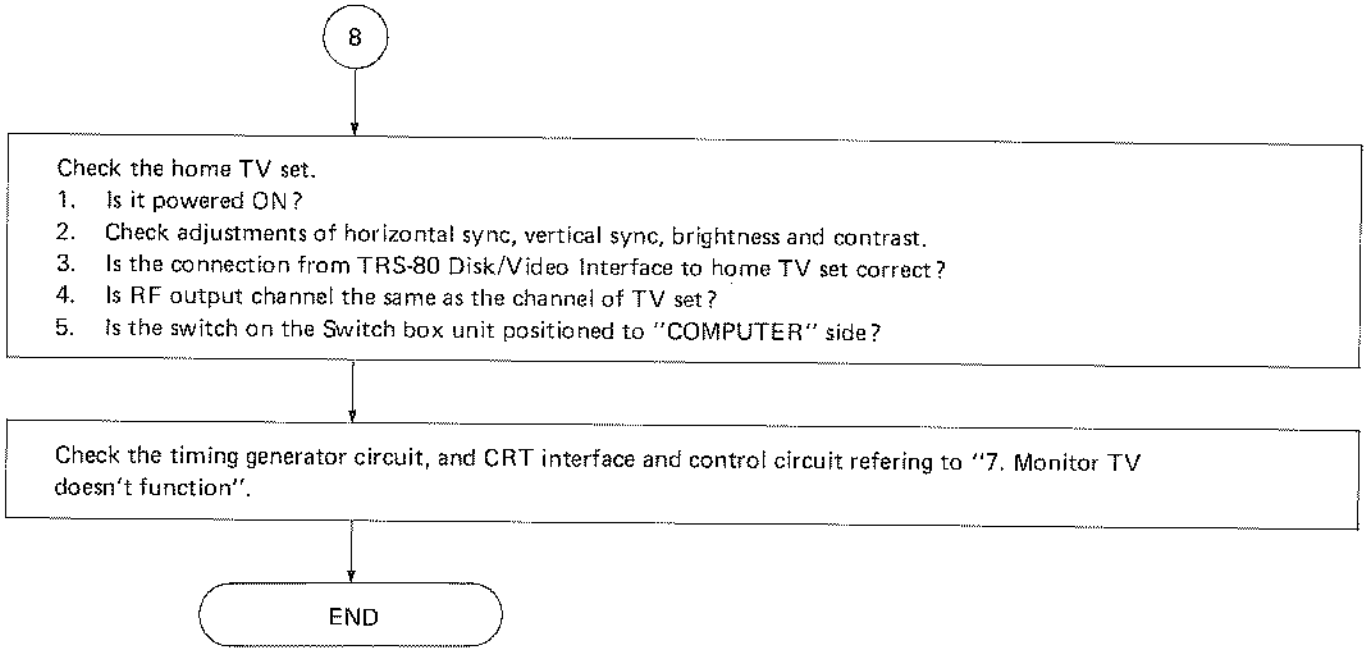


8. Home TV doesn't function



9. Check system again, as described in the "Troubleshooting Flowchart".

Check List

After completing all repairs and adjustments, check all functions according to the TEST program shown below. Before beginning the checking, TRS-80 Portable Computer must be cold started and the DISK BASIC is loaded to it.

1. Checking the floppy disk control

(1) Put the System Disk into Drive0 FDD.

(2) Execute the format program.
Type RUN "0:FORMAT" (ENTER).

(3) When the following message appears, press 0 (ENTER).

message . . . This utility formats diskettes.
— All data will be lost —
Which drive will be used (0 or 1)?

(4) The next message appears. Place the blank diskette into Drive 0 FDD and press (ENTER).

message . . . Put the diskette to be formatted in Drive0.
Press (ENTER) when ready.

Then the diskette is being formatted.

(5) If the message "FORMAT COMPLETE" appears on the display, the diskette is correctly formatted.

(6) Then type NEW (ENTER) for clearing the format program and execute the TEST program listed below.

. . . TEST program . . .

```
 10  CLEAR 1000:A$=" ":B$=" "
 20  FOR I=32 TO 159
 30  A$=A$+CHR$(I)
 40  NEXT I
 50  T=0:S=0:GOSUB 500
 60  S=1:GOSUB 500
 70  T=39:S=0:GOSUB 500
 80  S=1:GOSUB 500
 90  T=0:S=0:GOSUB 1000
100  S=1:GOSUB 1000
110  T=39:S=0:GOSUB 1000
120  S=1:GOSUB 1000
130  BEEP:PRINT"FLOPPY TEST . . . OK!!"
140  GOTO 1540
500  FOR I=1 TO 18
510  DSKO$0, T, I, S, A$
520  NEXT I
530  RETURN
1000 FOR I=1 TO 18
1010 B$=DSKI$(0, T, I, S)
1020 B$=LEFT$(B$, 128)
1030 IF A$<>B$ THEN GOTO 1500
1040 NEXT I
1050 RETURN
1500 CLS:BEEP:PRINT"FLOPPY TEST . . . NG!!"
1510 PRINT"TRACK=";T,"SECTOR=";I
1520 PRINT"WRITE DATA":PRINT A$
1530 PRINT"READ DATA":PRINT B$
1540 PRINT:INPUT"TRY AGAIN (y or n)";C$
1550 IF C$="y" THEN GOTO 10
1560 IF C$="n" THEN END
1570 GOTO 1540
```

After executing this program, if the message "FLOPPY TEST . . . OK!!" appears, checking of floppy disk control is completed correctly.

2. Checking the display

(1) Connect either monitor, CRT monitor or home TV set.
(2) Clear the previous program by typing NEW (ENTER).
(3) Then input the following TEST program and execute it.

```
. . . TEST program . . .
10  SCREEN1:A=40
20  WIDTH A
30  FOR I=32 TO 255
35  IF I=127  THEN50
40  PRINT CHR$ (I);
50  NEXT I
60  PRINT:PRINT"IF THE DISPLAY IS OK, PRESS ENTER"
70  A$=INKEY$:IF A$<>" " THEN GOTO 70
80  IF A=40 THEN A=80:GOTO 20
90  A=40:GOTO 20
```

(4) After executing this program, all characters will appear on the screen. Then check all characters with both display mode (40 characters mode and 80 characters mode).

6/Exploded View and Parts List

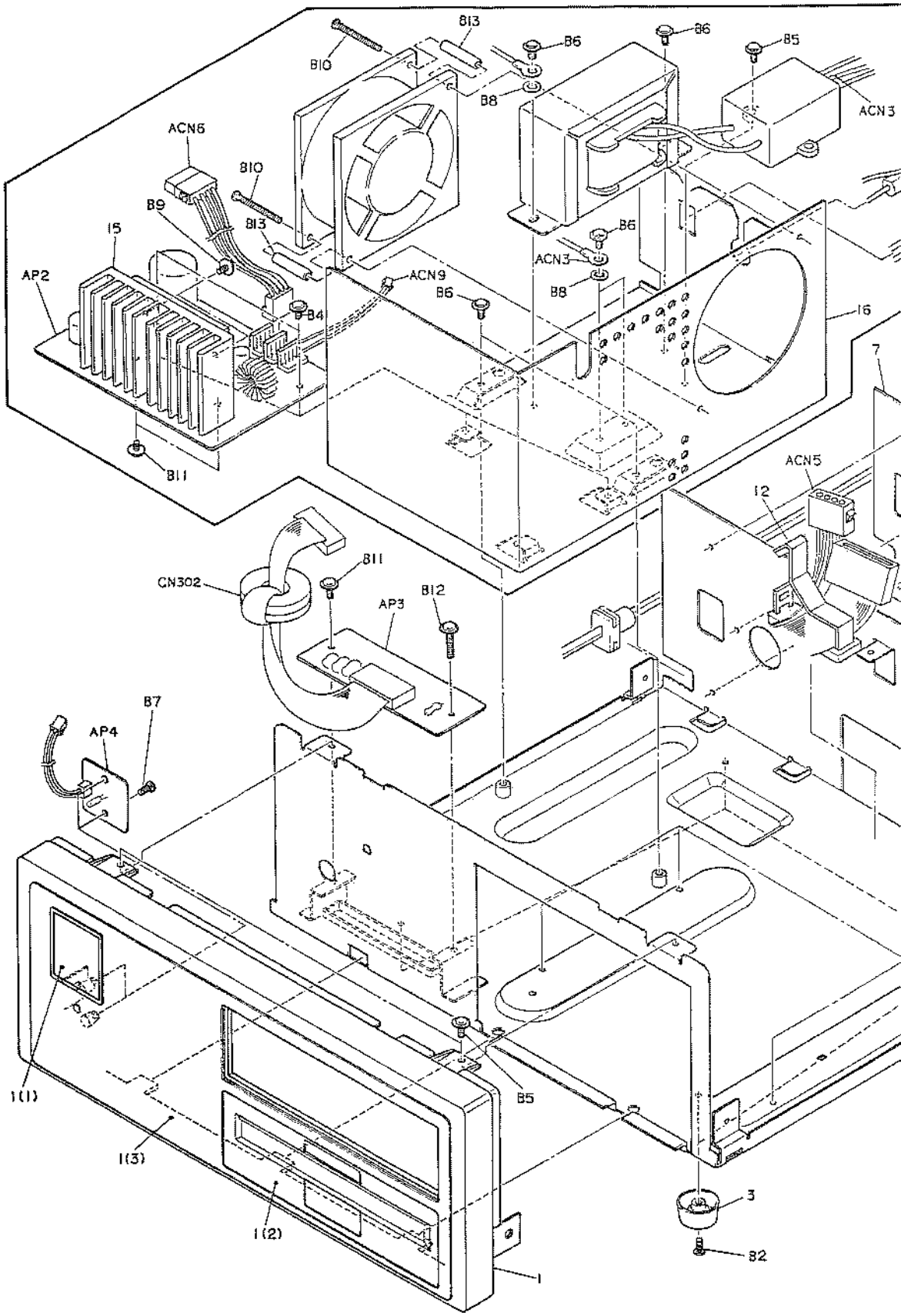


Figure 6-1. Ex

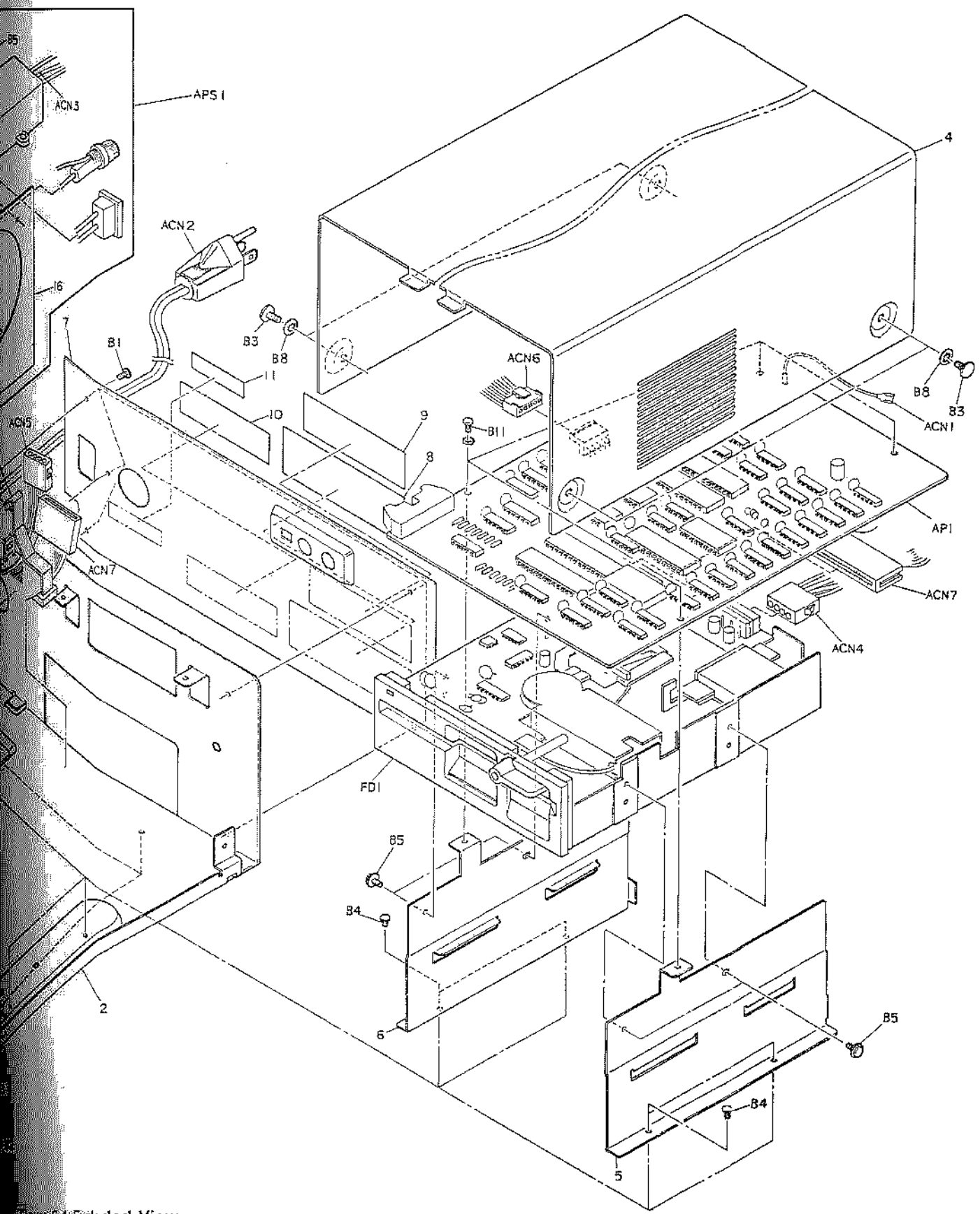


Figure 6-1 Exploded View

MAIN P.C.B. ASSEMBLY

Ref. No.	Description		RS Part No.	Mfr's Part No.
CAPACITORS				
C1	Not used			
C2	Capacitor, Ceramic	0.1μF/25V/+80 −20%		CBF1E104ZT
C3	Capacitor, Electrolytic	100μF/16V/±20%		CEVD101A3N
C4	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C5	Capacitor, Tantalum	22μF/16V/±20%		CSKD220MDC
C6	Capacitor, Ceramic	0.1μF/12V/±20%		CBF1B104MY
C7	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C8	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C9	Capacitor, Ceramic	0.1μF/12V/±20%		CBF1B104MY
C10	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C11	↓	↓		↓
C12				
C13				
C14	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C15	Capacitor, Ceramic	0.1μF/12V/±20%		CBF1B104MY
C16	Capacitor, Ceramic	0.1μF/12V/±20%		CBF1B104MY
C17	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C18	Capacitor, Tantalum	1μF/10V/±20%		CSKC010MDC
C19	Capacitor, Ceramic	0.1μF/12V/±20%		CBF1B104MY
C20	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C21	Capacitor, Ceramic	0.1μF/12V/±20%		CBF1B104MY
C22	Capacitor, Electrolytic	100μF/10V/+75 −10%		CEVC101ALN
C23	Capacitor, Ceramic	0.1μF/12V/±20%		CBF1B104MY
C24	Capacitor, Tantalum	1μF/10V/±20%		CSKC010MDC
C25	Capacitor, Ceramic	0.1μF/12V/±20%		CBF1B104MY
C26	Capacitor, Tantalum	1μF/10V/±20%		CSKC010MDC
C27	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C28	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C29	Capacitor, Ceramic	0.1μF/12V/±20%		CBF1B104MY
C30	Capacitor, Tantalum	1μF/10V/±20%		CSKC010MDC
C31	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C32	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C33–34	Not used			
C35	Capacitor, Mylar*	0.047μF/50V/±5%		CQMB473JTH
C36	Capacitor, Tantalum	1μF/10V/±20%		CSKC010MDC
C37	Capacitor, Tantalum	1μF/10V/±20%		CSKC010MDC
C38	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C39	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C40	Capacitor, Mylar	0.047μF/50V/±5%		CQMB473JTH
C41	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C42	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C43	Capacitor, Tantalum	1μF/10V/±20%		CSKC010MDC
C44	Capacitor, Trimmer	25pF	AC-0986	CTZ7250H01
C45	Capacitor, Ceramic	220pF/50V/±10%		CCFB221K0T
C46	Capacitor, Ceramic	33pF/50V/±10%		CCFB330K0T
C47	Capacitor, Ceramic	0.1μF/12V/±20%		CBF1B104MY
C48	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C49	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C50	Capacitor, Tantalum	1μF/10V/±20%		CSKC010MDC
C51	Capacitor, Ceramic	220pF/50V/±10%		CCFB221K0T
C52	Capacitor, Ceramic	33pF/50V/±10%		CCFB330K0T
C53	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY

* Mylar is a registered trademark of E.I.Du Pont de Nemours and Company.

Ref. No.	Description		RS Part No.	Mfr's Part No.
C54	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C55	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C56	Capacitor, Tantalum	1μF/10V/±20%		CSKC010MDC
C57	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C58	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C59	Capacitor, Tantalum	1μF/10V/±20%		CSKC010MDC
C60	Capacitor, Ceramic	0.047μF/25V/±10%		CBF1E473KY
C61	Capacitor, Ceramic	470pF/50V/±10%		CKFB471KBM
C62	↓	↓		↓
C63				
C64	Capacitor, Ceramic	470pF/50V/±10%		CKFB471KBM
C65	Capacitor, Tantalum	1μF/10V/±20%		CSKC010MDC
C66	Capacitor, Ceramic	100pF/50V/±10%		CCFB101K0T
C67	Capacitor, Electrolytic	22μF/16V/±20%		CEVD220A3N
C68	Capacitor, Ceramic	470pF/50V/±10%		CKFB471KBM
C69	Capacitor, Ceramic	1000pF/50V/±10%		CKFB102KBT
C70	↓	↓		↓
C71				
C72	Capacitor, Ceramic	1000pF/50V/±10%		CKFB102KBT
C73	Capacitor, Ceramic	470pF/50V/±10%		CKFB471KBM
C74–75	Not used			
C76	Capacitor, Ceramic	470pF/50V/±10%		CKFB471KBM
C77	Capacitor, Electrolytic	4.7μF/25V/+75 −10%		CEVE4R7ALN
C78	Capacitor, Ceramic	33pF/50V/±10%		CCFB330K0T
C79	Capacitor, Ceramic	0.1μF/12V/±20%		CBF1B104MY
C80	↓	↓		↓
C81				
C82	Capacitor, Ceramic	0.1μF/12V/±20%		CBF1B104MY
C83	Capacitor, Ceramic	56pF/50V/±10%		CCFB560K0T
C84	Capacitor, Ceramic	56pF/50V/±10%		CCFB560K0T
CONNECTORS				
CN1	Jack, Junction	to System Bus	AJ-7527	YJF20S022U
CN2	Jack, Junction	to Floppy Disk	AJ-7528	YJF34S013U
CN4	Jack, Junction	to Power Supply	AJ-7526	YJF05S023Z
DIODE				
D1	Diode, Silicon	1S2076		QDSS2076#B
COIL				
L1	Coil, Choke	4.7μH/500mA	ACB-2551	LF4R7KE04Y

Ref. No.	Description		RS Part No.	Mfr's Part No.
INTEGRATED CIRCUITS				
M1	I.C., TTL, Flip-Flop	HD74LS74AP or		QQT07474CB
		SN74LS74AN or		QQT07474AU
		M74LS74AP or		QQT07474DE
		MB74LS74A		QQT07474GF
M2	I.C., TTL, AND Gate	HD74LS08P or		QQT07408FB
		SN74LS08N or		QQT07408BU
		M74LS08P or		QQT07408EE
		MB74LS08		QQT07408GF
M3	I.C., TTL, OR Gate	HD74LS32P or	MX-5964	QQT07432CB
		SN74LS32N or		QQT07432BU
		M74LS32P or		QQT07432EE
		MB74LS32		QQT07432FF
M4	I.C., TTL, Flip-Flop	HD74LS174P or		QQT74174BB
		M74LS174P or		QQT74174AE
		SN74LS174N or		QQT74174DU
		MB74LS174		QQT74174CF
M5	I.C., TTL, EX-OR Gate	HD74LS86P or		QQT07486CB
		SN74LS86N or		QQT07486AU
		M74LS86P or		QQT07486GE
		MB74LS86		QQT07486HF
M6	I.C., TTL, OR Gate	HD74LS32P or	MX-5964	QQT07432CB
		SN74LS32N or		QQT07432BU
		M74LS32P or		QQT07432EE
		MB74LS32		QQT07432FF
M7	I.C., TTL, Inverter	HD74LS04P or		QQT07404HB
		SN74LS04P or		QQT07404AU
		M74LS04P or		QQT07404FE
		MB74LS04		QQT07404JF
M8	I.C., TTL, Counter	HD74LS393P or	MX-5969	QQT74393BB
		SN74LS393N or		QQT74393AU
		M74LS393P		QQT74393CE
M9	I.C., TTL, Buffer	HD74LS125AP or	MX-5965	QQT74125CB
		M74LS125AP or		QQT74125AE
		SN74LS125AN or		QQT74125EU
		MB74LS125A		QQT74125DF
M10	I.C., TTL, Driver	HD7416P or	MX5963	QQT07416BB
		SN7416N		QQT07416AU
M11	I.C., TTL, Flip-Flop	HD74LS74AP or		QQT07474CB
		SN74LS74AN or		QQT07474AU
		M74LS74AP or		QQT07474DE
		MB74LS74A		QQT07474GF
M12	I.C., TTL, Counter	HD74LS393P or	MX-5969	QQT74393BB
		SN74LS393N or		QQT74393AU
		M74LS393P		QQT74393CE
M13	I.C., N-MOS, CRTC	HD46505SP	MX-5959	QQN46505AB
M14	I.C., TTL, Driver	HD7416P or		QQT07416BB
		SN7416N		
M15	I.C., TTL, Shift Register	SN74LS166AN or		QQT74166CU
		M74LS166AP		QQT74166DE
M16	I.C., TTL, Flip-Flop	HD74LS174P or		QQT74174BB
		M74LS174P or		QQT74174AE
		SN74LS174N or		QQT74174DU
		MB74LS174		QQT74174CF

Ref. No.	Description		RS Part No.	Mfr's Part No.
M17	I.C., N-MOS, P-ROM for Char. Gen.	HN462732G (For USA and Canada)	MX-5961	QQ0C1027AB
		(For UK, Belgium and Australia)		QQ0C1027BB
M18	I.C., TTL, Flip Flop	HD74LS374P or	MX-5968	QQT74374BB
		SN74LS374N or		QQT74374CU
		M74LS374P or		QQT74374AE
		MB74LS374		QQT74374DF
M19	I.C., C-MOS, RAM	HM6116LP-4 or	MX-5970	QQ006116BB
		HM6116P-4		QQ006116AB
M20	I.C., TTL, Selector	HD74LS157P or		QQT74157BB
		SN74LS157N or		QQT74157AU
		M74LS157P or		QQT74157DE
		MB74LS157		QQT74157FF
M21	I.C., TTL, Inverter	HD74LS14P or	MX-5962	QQT07414CB
		SN74LS14N or		QQT07414AU
		M74LS14P or		QQT07414EE
		MB74LS14		QQT07414FF
M22	I.C., TTL, Transceiver	HD74LS245WP or	MX-5967	QQT74245DB
		SN74LS245N or		QQT74245AU
		M74LS245P or		QQT74245BE
		MB74LS245		QQT74245EF
M23	I.C., C-MOS, RAM	HM6116LP-4 or	MX-5970	QQ006116BB
		HM6116P-4		QQ006116AB
M24	I.C., TTL, Selector	HD74LS157P or		QQT74157BB
		SN74LS157N or		QQT74157AU
		M74LS157P or		QQT74157DE
		MB74LS157		QQT74157FF
M25	I.C., TTL, Selector	HD74LS157P or		QQT74157BB
		SN74LS157N or		QQT74157AU
		M74LS157P or		QQT74157DE
		MB74LS157		QQT74157FF
M26	I.C., N-MOS, FDC	M5W1793-02P or	MX-5957	QQN01793AE
		MB8877A		QQN08877AF
M27	I.C., C-MOS, FD Data Separator	SED9421C0B	MX-5973	QQ09421CB6
M28	I.C., C-MOS, RAM	HM6116LP-4 or	MX-5970	QQ006116BB
		HM6116P-4		QQ006116AB
M29	I.C., TTL, NAND Gate	HD74LS00P		QQT07400GB
M30	I.C., TTL, OR Gate	HD74LS32P or	MX-5964	QQT07432CB
		SN74LS32N or		QQT07432BU
		M74LS32P or		QQT07432EE
		MB74LS32		QQT07432FF
M31	I.C., TTL, Decoder	HD74LS138P or		QQT74138BB
		SN74LS138N or		QQT74138AU
		M74LS138P or		QQT74138DE
		MB74LS138		QQT74138FF
M32	I.C., TTL, Inverter	HD74LS04P or		QQT07404HB
		SN74LS04N or		QQT07404AU
		M74LS32P or		QQT07404FE
		MB74LS04		QQT07404JF
M33	I.C., TTL, Counter	HD74LS163P	MX-5966	QQT74163BB
M34	I.C., TTL, OR Gate	HD74LS32P or	MX-5964	QQT07432CB
		SN74LS32N or		QQT07432BU
		M74LS32P or		QQT07432EE
		MB74LS32		QQT07432FF

Ref. No.	Description		RS Part No.	Mfr's Part No.
M35	I.C., TTL, OR Gate	HD74LS32P or	MX-5964	QQT07432CB
		SN74LS32N or		QQT07432BU
		M74LS32P or		QQT07432EE
		MB74LS32		QQT07432FF
M36	I.C., C-MOS, RAM	HM6116LP-4 or	MX-5970	QQ006116BB
		HM6116P-4		QQ006116AB
M37	I.C., TTL, NAND Gate	HD74LS00P or		QQT07400GB
		SN74LS00N or		QQT07400BU
		M74LS00P or		QQT07400KE
		MB74LS00		QQT07400MF
M38	I.C., TTL, Decoder	HD74LS139P or		QQT74139AB
		SN74LS139N or		QQT74139BU
		M74LS139P or		QQT07400MF
		MB74LS139		QQT74139DF
M39	I.C., TTL, AND Gate	HD74LS08P or		QQT07408FB
		SN74LS08N or		QQT07408BU
		M74LS08P or		QQT07408EE
		MB74LS08		QQT07408GF
M40	I.C., N-MOS, P-ROM for Program	HN462732G (For USA and Canada)	MX-5960	QQ0C1026AB
		(For UK, Belgium and Australia)		QQ0C1026BB
M41	I.C., C-MOS, Buffer	TC40H365P	MX-5972	QQ040365AT
M42	I.C., N-MOS, CPU	μPD780C-1 or	MX-5956	QQN00780AA
		LH0080A or		QQN0080AA3
		MK3880-4 or		QQN03880BZ
		Z-80A		QQN80ACPUZ
M43	I.C., TTL, DRVR/DCVR	HD74LS244P or		QQT74244CB
		SN74LS244N or		QQT74244AU
		M74LS244P or		QQT74244BE
		MB74LS244		QQT74244DF
M44	I.C., C-MOS, Buffer	TC40H245P	AMX-5818	QQ040245AT
M45	I.C., N-MOS, PPI	M5L8255AP-5 or	MX-5958	QQN08255AE
		μPD8255AC-5		QQN08255BA
M46	I.C., TTL, Selector	HD74LS153P or		QQT74153EB
		M74LS153P or		QQT74153AE
		MB74LS153P or		QQT74153FF
		SN74LS153N		QQT74153DU
M47	I.C., TTL, Flip-Flop	HD74LS74AP or		QQT07474CB
		SN74LS74AN or		QQT07474AU
		M74LS74AP or		QQT07474DE
		MB74LS74A		QQT07474GF
M48	I.C., TTL, Flip-Flop	HD74LS74AP or		QQT07474CB
		SN74LS74AN or		QQT07474AU
		M74LS74AP or		QQT07474DE
		MB74LS74A		QQT07474GF
M49	I.C., TTL, Flip-Flop	HD74LS74AP or		QQT07474CB
		SN74LS74AN or		QQT07474AU
		M74LS74AP or		QQT07474DE
		MB74LS74A		QQT07474GF

Ref. No.	Description		RS Part No.	Mfr's Part No.
RESISTOR ARRAYS				
MR1	Resistor Array,	10K x 6, 1/8W/±10%	ARX-0384	RAB103K06D
MR2	Resistor Array,	100K x 6, 1/8W/±20%	ARX-0385	RAB104M06X
MR3	Resistor Array,	100K x 8, 1/8W/±20%		RAB104M08X
MR4	Resistor Array,	33K x 8, 1/8W/±20%		RAB333M08X
RESISTORS				
R1	Resistor, Carbon	10 ohm/1/4W/±5%		RD25PJ100X
R2	Resistor, Carbon	75 ohm/1/4W/±5%		RD25PJ750X
R3	Resistor, Carbon	33 ohm/1/4W/±5%		RD25PJ330X
R4	Resistor, Carbon	1.5K ohm/1/4W/±5%		RD25PJ152X
R5	Resistor, Carbon	240 ohm/1/4W/±5%		RD25PJ241X
R6	Resistor, Carbon	470 ohm/1/4W/±5%		RD25PJ471X
R7	Resistor, Carbon	330 ohm/1/4W/±5%		RD25PJ331X
R8	↓	↓		↓
R9				
R10	Resistor, Carbon	330 ohm/1/4W/±5%		RD25PJ331X
R11	Resistor, Carbon	10K ohm/1/4W/±5%		RD25PJ103X
R12	↓	↓		↓
R13				
R14				
R15	Resistor, Carbon	10K ohm/1/4W/±5%		RD25PJ103X
R16—17	Not used			
R18	Resistor, Carbon	10K ohm/1/4W/±5%		RD25PJ103X
R19	Resistor, Carbon	470 ohm/1/4W/±5%		RD25PJ471X
R20	Resistor, Carbon	1.2K ohm/1/4W/±5%		RD25PJ122X
R21	Resistor, Carbon	4.7K ohm/1/4W/±5%		RD25PJ472X
R22	Resistor, Carbon	330 ohm/1/4W/±5%		RD25PJ331X
R23	Resistor, Carbon	4.7K ohm/1/4W/±5%		RD25PJ472X
R24	Resistor, Carbon	1K ohm/1/4W/±5%		RD25PJ102X
R25	Resistor, Carbon	1K ohm/1/4W/±5%		RD25PJ102X
R26	Resistor, Carbon	1K ohm/1/4W/±5%		RD25PJ102X
R27	Resistor, Carbon	330 ohm/1/4W/±5%		RD25PJ331X
R28	Resistor, Carbon	1K ohm/1/4W/±5%		RD25PJ102X
R29	Resistor, Carbon	33K ohm/1/4W/±5%		RD25PJ333X
R30	Resistor, Carbon	1K ohm/1/4W/±5%		RD25PJ102X
R31				
R32				
R33	Resistor, Carbon	1K ohm/1/4W/±5%		RD25PJ102X
R34	Resistor, Carbon	33K ohm/1/4W/±5%		RD25PJ333X
R35	Resistor, Carbon	1K ohm/1/4W/±5%		RD25PJ102X
R36	↓	↓		↓
R38				
R39				
R40				
R41				
R42				
R43	Resistor, Carbon	1K ohm/1/4W/±5%		RD25PJ102X

Ref. No.	Description		RS Part No.	Mfr's Part No.
R44	Resistor, Carbon	1K ohm/1/4W/±5%		RD25PJ102X
R45—46	Not used			
R47	Resistor, Carbon	1K ohm/1/4W/±5%		RD25PJ102X
R48	↓	↓		↓
R49	Resistor, Carbon	1K ohm/1/4W/±5%		RD25PJ102X
R50	Resistor, Carbon	4.7K ohm/1/4W/±5%		RD25PJ472X
R51	Resistor, Carbon	4.7K ohm/1/4W/±5%		RD25PJ472X
R53	Resistor, Carbon	33K ohm/1/4W/±5%		RD25PJ333X
R54	Resistor, Carbon	33K ohm/1/4W/±5%		RD25PJ333X
RF MODULATOR				
RF1	RF Modulator	(For USA and Canada) (For UK and Belgium) (For Australia)	AX-9440	ZUV0000203 ZUV0003601 ZUV0000101
TRANSISTOR				
T1	Transistor, NPN, 2SC2002, Silicon, NO-Rank			QTC2002XCA
CRYSTAL				
X1	Crystal Oscillator 16.0 MHz		MX-1102	XBR1A1010X
MISCELLANEOUS				
ACN-1	Ground Wire with Terminals, for MAIN PCB			ACZZ157ULA
M17, M40	Socket, for I.C., DICF-24CS		AJ-7529	YSC24S001Z

POWER SUPPLY P.C.B. ASSEMBLY

Ref. No.	Description	RS Part No.	Mfr's Part No.
CAPACITOR			
C101	Capacitor, Electrolytic 6800μF/35V/±20%	CC-688MGAP	CEAF682AQR
C102	Capacitor, Electrolytic 1μF/50V/±20%		CEVG010A3N
C103	Capacitor, Ceramic 0.047μF/25V/±10%		CBF1E473KY
C104	Capacitor, Ceramic 0.01μF/25V/±10%		CBF1E103KT
C105	Capacitor, Electrolytic 22μF/16V/±20%		CEVD220A3N
C106	Capacitor, Electrolytic 1000μF/16V/±20%		CEAD102A3N
C107	Capacitor, Electrolytic 1000μF/10V/±20%		CEAC102A3N
C108	Capacitor, Electrolytic 220μF/10V/±20%		CEVC221A3N
C109	Capacitor, Ceramic 0.01μF/25V/±10%		CBF1E103KT
C110	Capacitor, Electrolytic 220μF/35V/±20%		CEAF221A3N
C111	Capacitor, Ceramic 0.1μF/50V/+80 −20%		CBF1H104ZT
CONNECTORS			
CN101	Jack, Junction to Power Transformer	AJ-7530	YJF02S039Z
CN102	Jack, Junction to FDD #0	AJ-7531	YJF04S038Z
CN103	Jack, Junction to FDD #1	AJ-7531	YJF04S038Z
CN104	Jack, Junction to Main PCB	AJ-7532	YJF05S017Z
CN105	Jack, Junction to LED	AJ-7322	YJF02S041Z
DIODES			
D101	Diode, Silicon S2V-10		QDS2V10XXK
D102	↓		↓
D103			
D104	Diode, Silicon S2V-10		QDS2V10XXK
D105	Diode, Silicon 1S2076		QDSS2076#B
D106	Diode, Silicon 1S2076		QDSS2076#B
FUSE and FUSE HOLDER			
F101	Fuse, 125V 3A	AHF-1293	ZFBP30202U
F101	Fuse Holder 85PN0819	AF-1249	YHF0P0008Z
COILS			
L101	Coil, Troidal SK11-3-150	ACA-8333	LWS151A01B
L102	Coil, Troidal PI-14	ACA-8334	LWS151A02C
L103	Coil, Troidal SF-T10-30	ACA-8335	LWS400301T

Ref. No.	Description	RS Part No.	Mfr's Part No.
INTEGRATED CIRCUIT			
M101	I.C., Regulator STK7551	MX-5974	QQH07551AC
RESISTORS			
R101	Resistor, Carbon 56K ohm/1/4W/±2%	N-0344CEC	RD25PG560Z
R102	Resistor, Carbon 1K ohm/1/4W/±5%		RD25PJ102X
R103	Resistor, Carbon 10K ohm/1/4W/±5%		RD25PJ103X
R104	Resistor, Carbon 51K ohm/1/4W/±2%		RD25PG5102
R105	Resistor, Carbon 33K ohm/1/4W/±2%		RD25PG3302
R106	Resistor, Carbon 47 ohm/1/4W/±5%		RD25PJ470X
R107	Resistor, Carbon 47 ohm/1/4W/±5%		RD25PJ470X
R108	Resistor, Carbon 270 ohm/1/4W/±5%		RD25PJ271X
R109	Resistor, Carbon 1K ohm/1/4W/±5%		RD25PJ102X
R110	Resistor, Carbon 56 ohm/1/4W/±5%		RD25PJ560X
R111	Resistor, Carbon 1K ohm/1/4W/±5%		RD25PJ102X
R112	Resistor, Metal Oxide 10 ohm/1W/±5%		RX1BNJ100B
TRANSISTORS			
T101	Transistor, PNP, 2SA1115, Silicon, NO-Rank		QTA1115XUE
T102	Transistor, PNP, 2SA1115, Silicon, NO-Rank		QTA1115XUE
POTENTIOMETER			
VR101	Potentiometer, 2K ohm B for +5V	AP-7385	RPSNB20205
ZENER DIODE			
ZD101	Diode, Silicon, Zener HZ2CLL		QDZHZ2CLXB
MISCELLANEOUS			
ACN-9	Connector with Cords and Resistor		ACCNG15GEA
15	Heat Sink, for Regulator I.C.		MU663AX001
B-9	Screw, Sems, Machine M3 x 16, S-ZnCr	AHD-2753	BSPJ3016NZ
B-11	Screw, Bind Head with Outside Toothed Washer, Machine M3 x 6, S-ZnCr	AHD-2754	BSP#3006NZ

SYSTEM BUS P.C.B. ASSEMBLY

Ref. No.	Description	RS Part No.	Mfr's Part No.
CAPACITORS			
C301	Capacitor, Tantalum 22μF/16V/±20%		CSKD220MDC
LF301	Noise Suppress Capacitor 270pF	ACF-7367	CZEC271M01
LF302–309	Not used		
LF310	Noise Suppress Capacitor 270pF	ACF-7367	CZEC271M01
LF311	Not used		
LF312	Noise Suppress Capacitor 270pF	ACF-7367	CZEC271M01
LF313	Noise Suppress Capacitor 270pF	ACF-7367	CZEC271M01
LF314	Noise Suppress Capacitor 270pF	ACF-7367	CZEC271M01
CONNECTORS			
CN301	Jack, Junction to Portable Computer	AJ-7533	YJF40S009U
CN302	Connector With Cords and Ferrite Core	AW-3182	ACCNG16GEA
COIL			
L301	Coil, Choke 22μH/55mA		LF220KE04Y
LED P.C.B. ASSEMBLY			
CN201	Connector with Cords, to Power Supply		ACCND59GEA
D201	L.E.D., RED, SLP-135B		QL1SP135BC
POWER SUPPLY ASSEMBLY			
ACN-2	Cord, AC Power (For USA and Canada)	AW-3181	ACAC196ULA
	(For UK)		ACAC202BSA
	(For Belgium)		ACAC203EEA
	(For Australia)		ACAC204ASA
ACN-3	Ground Wire With Terminal, for Noise Filter		ACZZ156ULA
AP-2	P.C.B. Assembly, Power Supply	AX-9441	APLX128BAA
NF1	Noise Filter, ZCBW203-11	AC-0987	FJ0060N03D
SW1	Switch, See-Saw, WK2A-44, (For USA and Canada)	AS-2891	SC010203VQ
	Power (For UK, Belgium and Australia)		SC020212AZ
PT1	Transformer, Power (For USA and Canada)	ATA-1053	TPF66V002P
	(For UK, Belgium and Australia)		TPG66E004P
F1	Fuse Holder, S-N1301 #51 (For USA and Canada)	AF-1250	YHF1S3009U
	(For UK, Belgium and Australia)		YHF1S2005Z
F1	Fuse, 250V, 1A (For USA and Canada)	AHF-1294	ZFBQ10207C
	Fuse, 250V, 315mA (For UK, Belgium and Australia)		ZFBQ32103S

Ref. No.	Description	RS Part No.	Mfr's Part No.
FM1	Fan Motor With Connector and Cords, DC12V, 0.16A, FBP-08A12M	AM-4732	ZNF0122701
16	Chassis, Power Supply		MB877SZ001
B-4	Screw, Sems, Machine, M3 x 6, S-ZnCr	AHD-2759	BSPN3006NZ
B-5	Screw, Cup Head, Machine, M3 x 6, S-ZnCr		BSP43006NZ
B-6	Screw, Cup Head, Machine, M4 x 6, S-ZnCr	AHD-2756	BSP44006NZ
B-10	Screw, Sems, Machine, M4 x 30, S-ZnCr	AHD-2755	BSPJ4030NZ
B-13	Spacer, M4 x 17		MM265SZ001
B-8	Washer, Inside Toothed, 4mm, S-Zn	AHD-8834	BWU40855SW

MECHANICAL AND ASSEMBLY PARTS

Ref. No.	Description	RS Part No.	Mfr's Part No.
AP-1	P.C.B. Assembly, Main (For USA and Canada)	AX-9439	APLX133AAG
	(For UK and Belgium)		APLX133ABG
	(For Australia)		APLX133ACG
AP-3	P.C.B. Assembly, System Bus	AX-9442	APLX134AAG
AP-4	P.C.B. Assembly, LED	AX-9443	APLX135AAG
APS-1	Power Supply Assembly (For USA and Canada)		AELX11*101
	(For UK)		AELX11*102
	(For Belgium)		AELX11*103
	(For Australia)		AELX11*104
ACN-4	Cords with Connectors, for FD-0 Power	AW-3183	ACCND55GEA
ACN-5	Cords with Connectors, for FD-1 Power	AW-3184	ACCND94GEA
ACN-6	Cords with Connectors, (For USA and Canada)	AW-3185	ACCND57GEA
	for Main PCB Power (For UK, Belgium and Australia)		ACCNG99GEA
ACN-7	Cords with Connectors, for FD Signals	AW-3186	ACCND58GEA
FD-1	Floppy Disk Assembly, FB-501-ST	AXX-5042	AXFP004GEA
1	Front Panel Assembly, Ivory	AZ-7100	AMX11*1001
1-(1)	Plate, Model	AHC-2395	MVMX11*102
1-(2)	Board, Blind, Black		VB751SB001
1-(3)	Panel, Front, Ivory		VB873SH003
2	Plate, Bottom		AMX11*1002
3	Foot, Rubber	AF-0369	VM283SB001
4	Case, Top, Ivory	AZ-7101	MB887SM008
5	Support, Floppy Disk-Right		ML772SZ001
6	Support, Floppy Disk-Left		ML772SZ002
7	Panel, Back, Ivory (For USA and Canada)	AZ-7102	MS872SM002
	(For UK and Belgium)		MS872SM003
	(For Australia)		MS872SM004
8	Plate, Serial, Number (For USA and Canada)		MVSX11*102
	(For UK)		MVSX11*104
	(For Belgium)		MVSX11*105
	(For Australia)		MVSX11*106
9	Label, FCC (USA Version Only)		KLX11*1001
10	Label, Caution		##E4388***
11	Label, Warning		KLX11*1003
12	Cable Clamper, for Drive #1 Signal Cable	AHC-2396	VX662NB001
B-1	Screw, Bind Head, Machine, M3 x 6, S-Ni	AHD-2757	BSPB3006NN
B-2	Screw, Sems, Machine, M3 x 10, S-ZnCr		BSPN3010NZ
B-3	Screw, Truss Head, Machine, M4 x 8, S-Ni	AHD-2758	BSPT4008NN
B-4	Screw, Sems, Machine, M3 x 6, S-ZnCr	AHD-2759	BSPN3006NZ
B-5	Screw, Cup Head, Machine, M3 x 6, S-ZnCr		BSP43006NZ
B-6	Screw, Cup Head, Machine, M4 x 6, S-ZnCr	AHD-2756	BSP44006NZ
B-7	Screw, Pan Head, Tapping, M3 x 6, S-ZnCr	AHD-2760	BTPP3006AZ
B-11	Screw, Bind Head with Outside Toothed Washer, Machine, M3 x 6, S-ZnCr	AHD-2754	BSP#3006NZ
B-12	Screw, Cup Head, Machine, M3 x 12, S-ZnCr		BSP43012NZ
B-8	Washer, Inside Toothed, 4mm, S-Zn	AHD-8834	BWU40855SW

Ref. No.	Description	RS Part No.	Mfr's Part No.
ACCESSORIES			
	Cords with Connectors, for System Bus	AW-3187	ACCND53GEA
	I.C. Socket, for System Bus, NP63 4006 S4	AJ-7534	YSC40S005Z
	System Diskette, (For USA and Canada)		ZVDM001302
	for Model 100 (For UK, Belgium and Australia)		ZVDM001303
	Cover, ROM, for Model 100		VS667SB005
	CRT Cable (For USA and Canada)		ACPP018GEA
	(For UK, Belgium and Australia)		ACPP020GEA
	Switch Box (USA and Canada Version Only)		AXSW012GEA
HARDWARE KIT			
	Screw, Bind Head, Machine M3 x 6, S-Ni	AHW-2603806	AYX11*1001
	Screw, Truss Head, Machine M4 x 8, S-Ni		
	Screw, Sems, Machine M3 x 10, S-ZnCr		

7/P.C.Board Views and Schematic Diagra

NOTE: Following two drawings are applicable for USA and Canada Versi

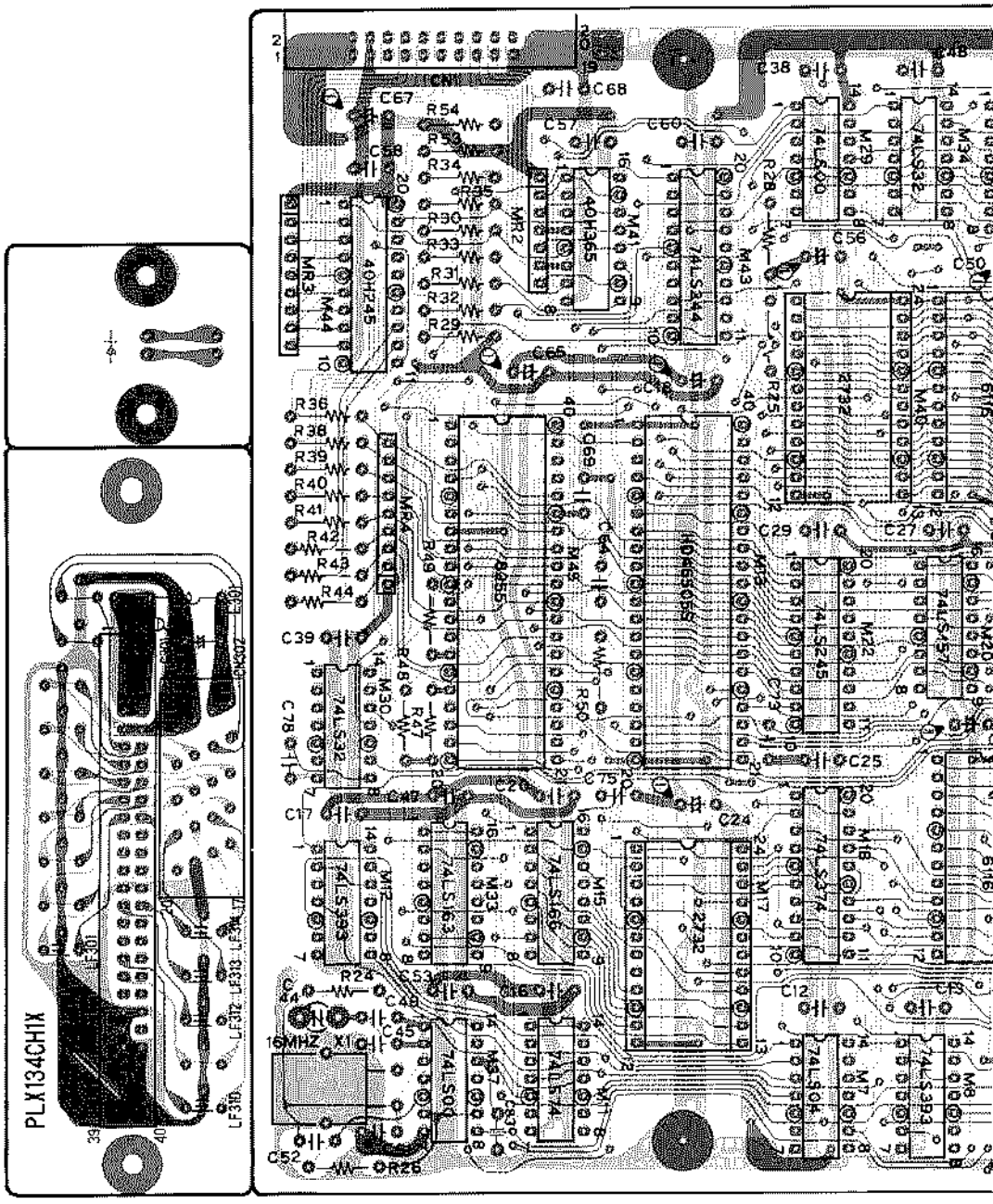
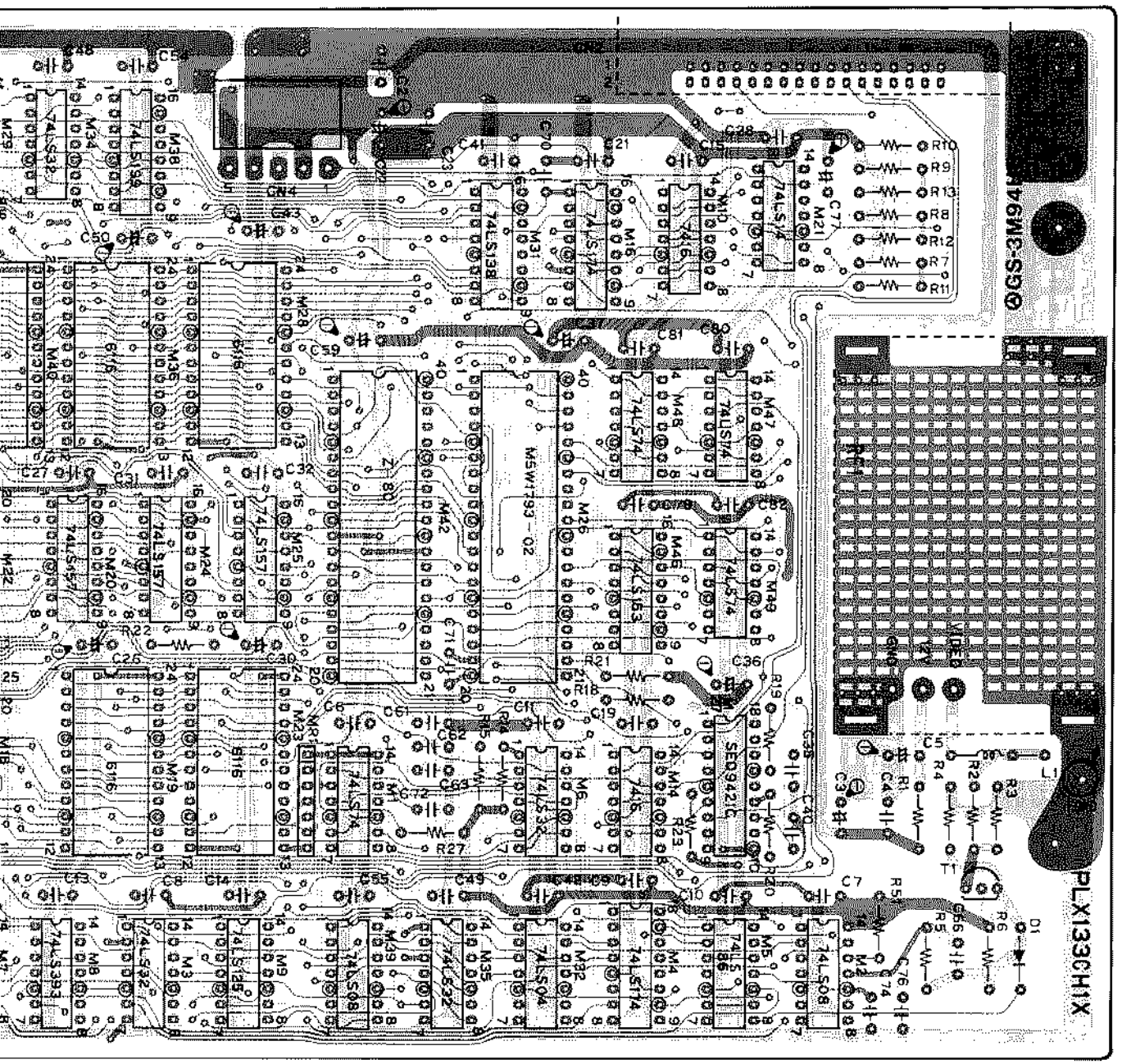


Figure 7-1. Main

agram

Canada Version.



re 7-1. Main P.C. Board (Top View)

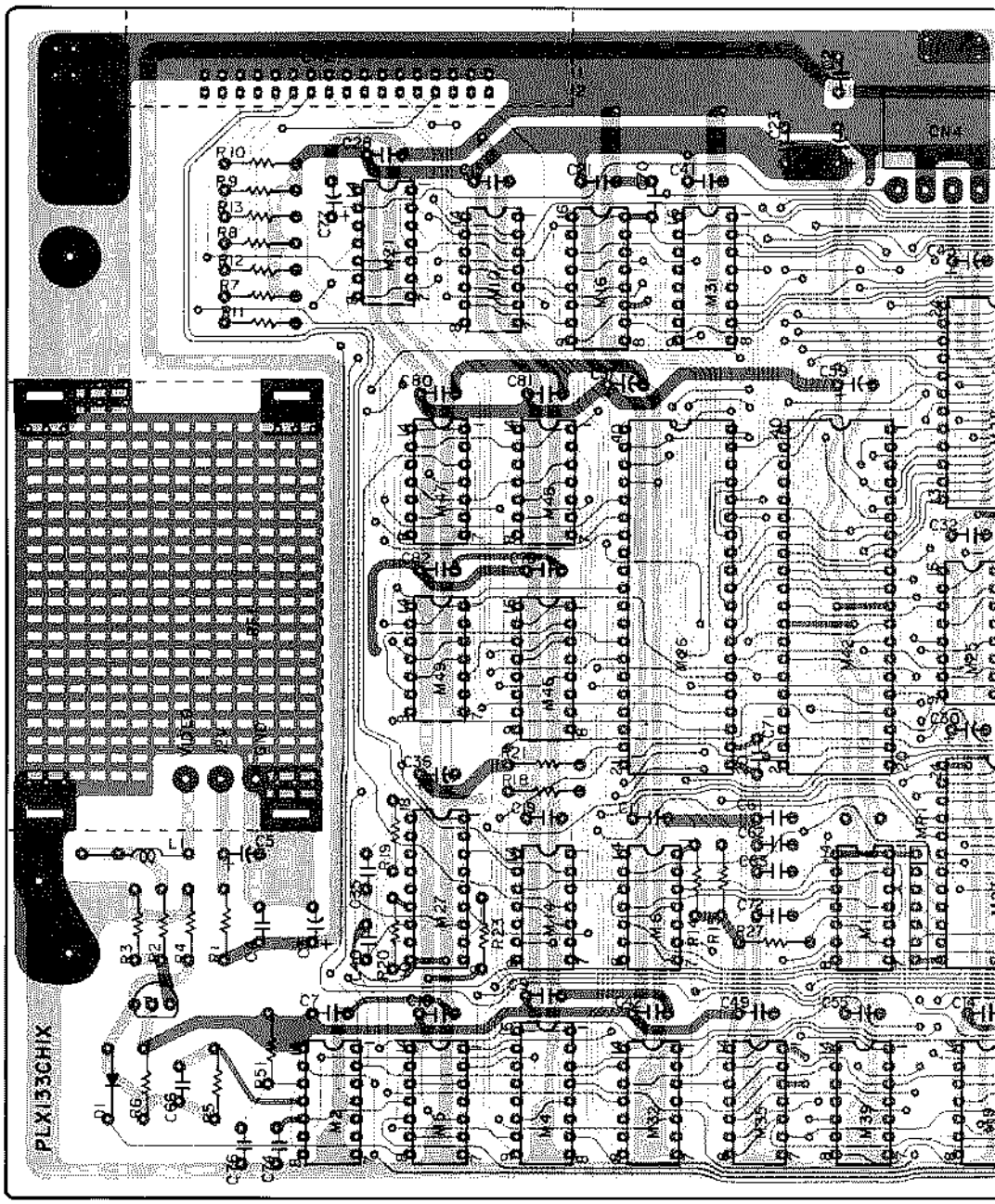
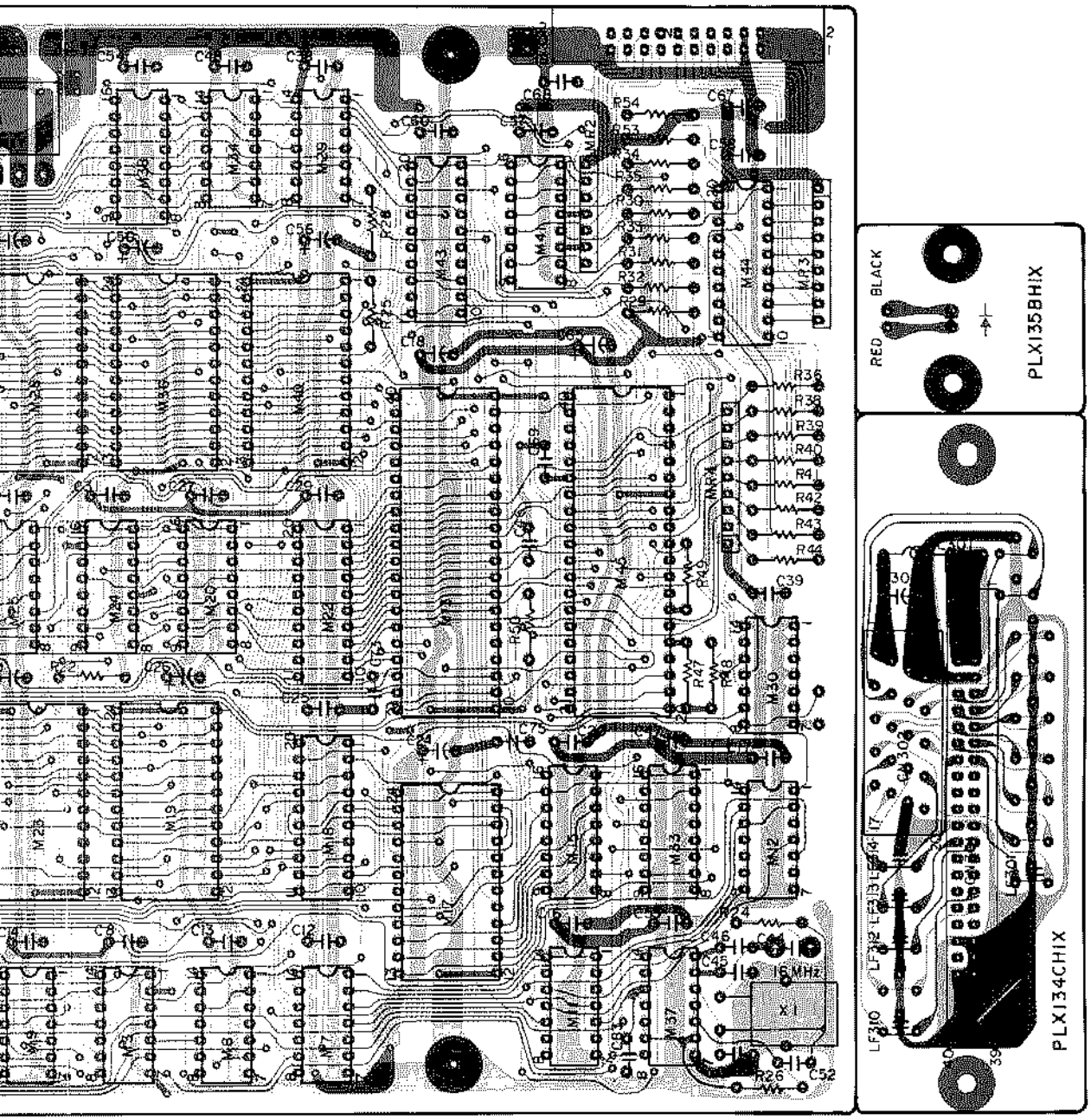


Figure 7-2. Main P



ain P.C. Board (Bottom View)

NOTE: Following two drawings are applicable for UK, Belgium and Australia Ver

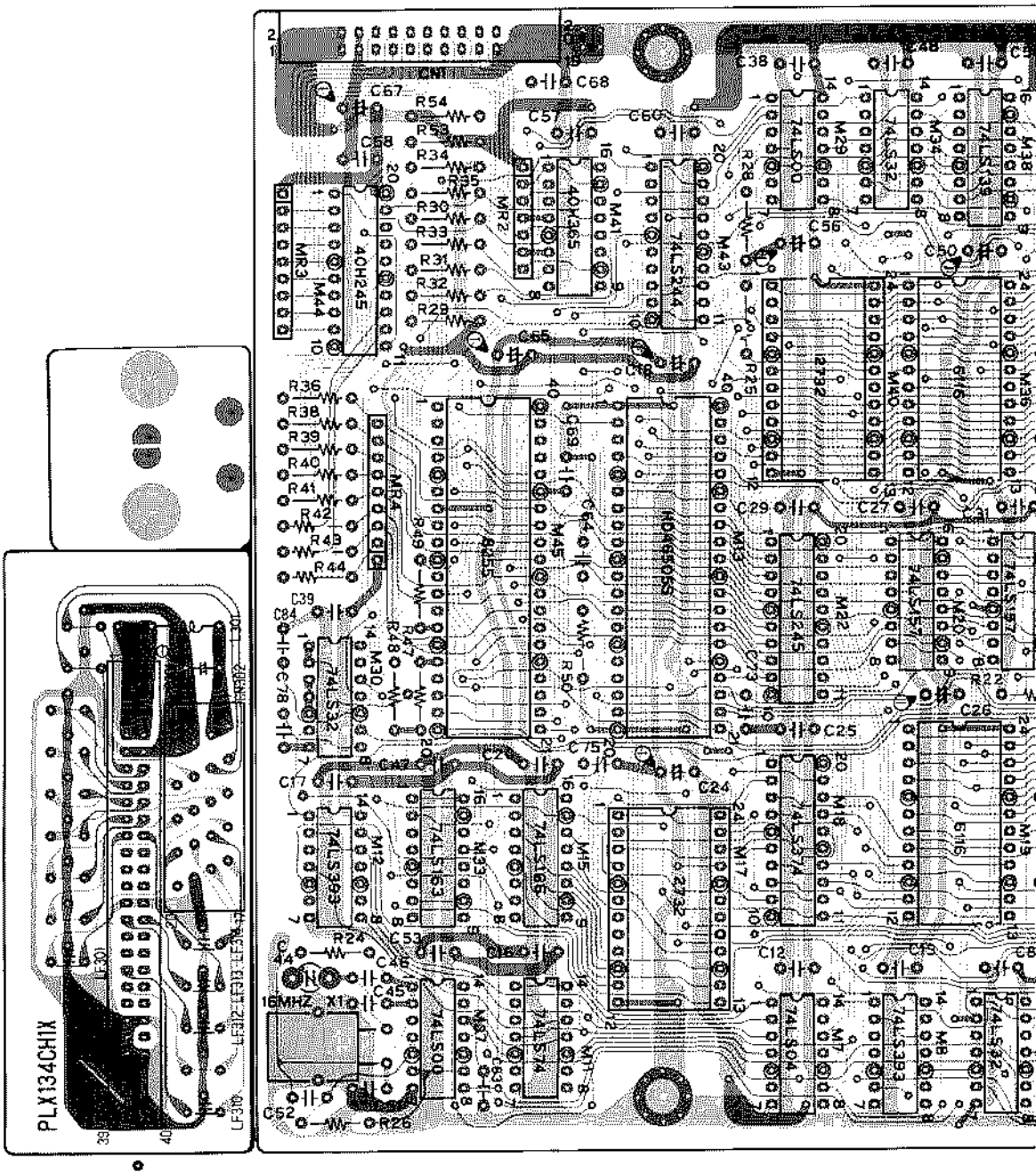
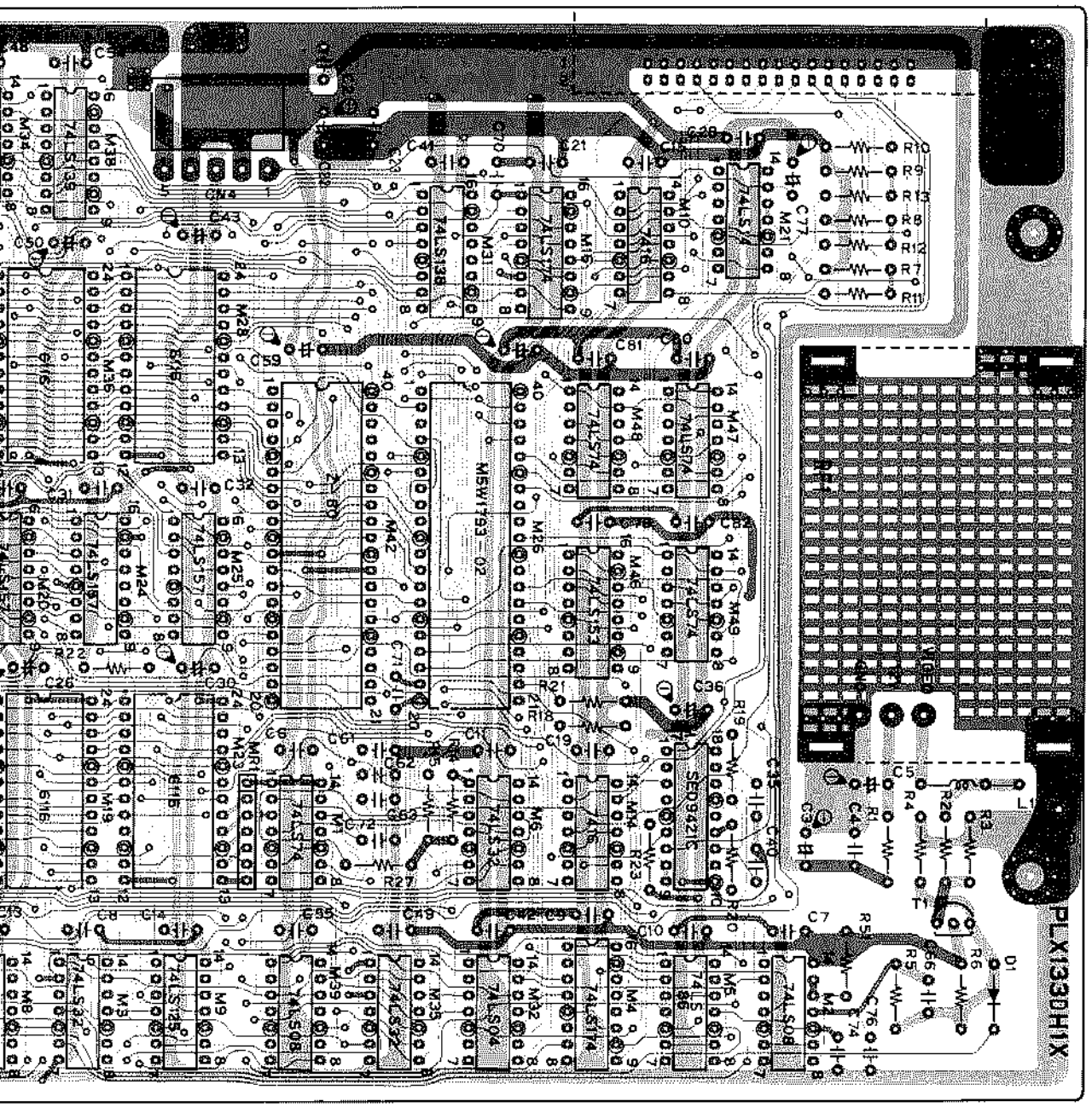


Figure 7-3. Main P.C. Board —

Australia Version.



C. Board — Revised (Top View)

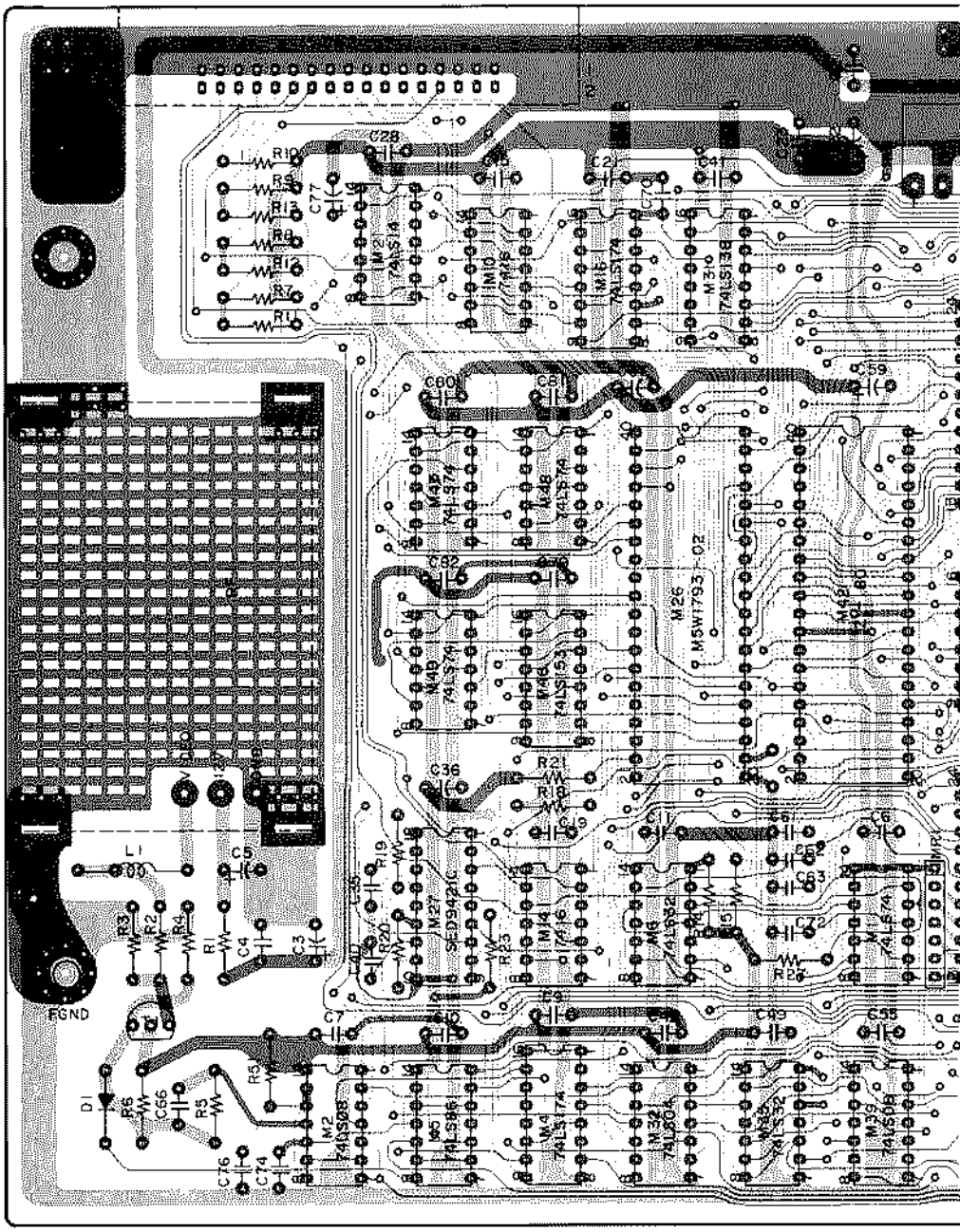
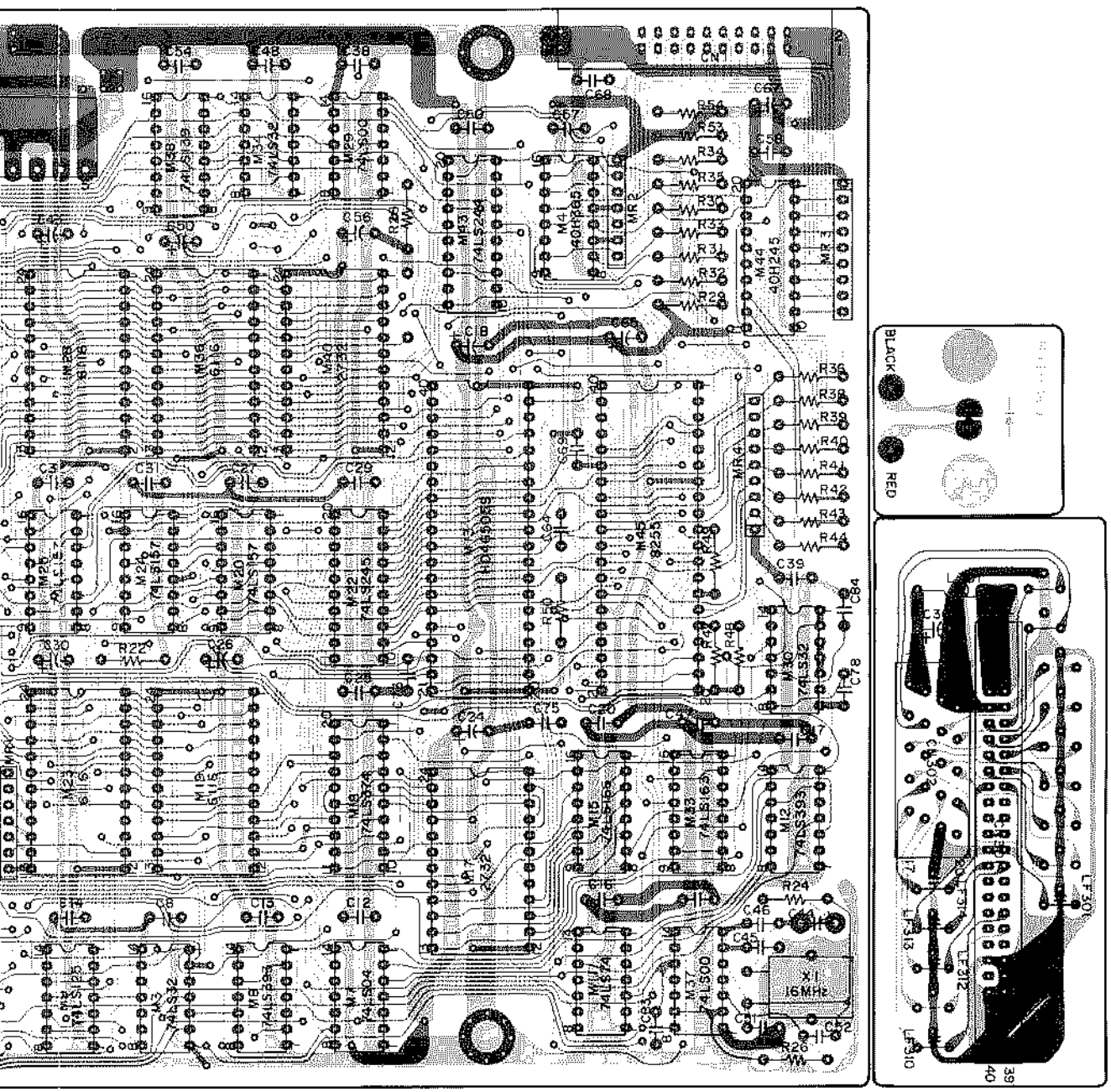


Figure 7-4 Mai



Main P.C. Board — Revised (Bottom View)

Power Supply P.C. Board

Top View

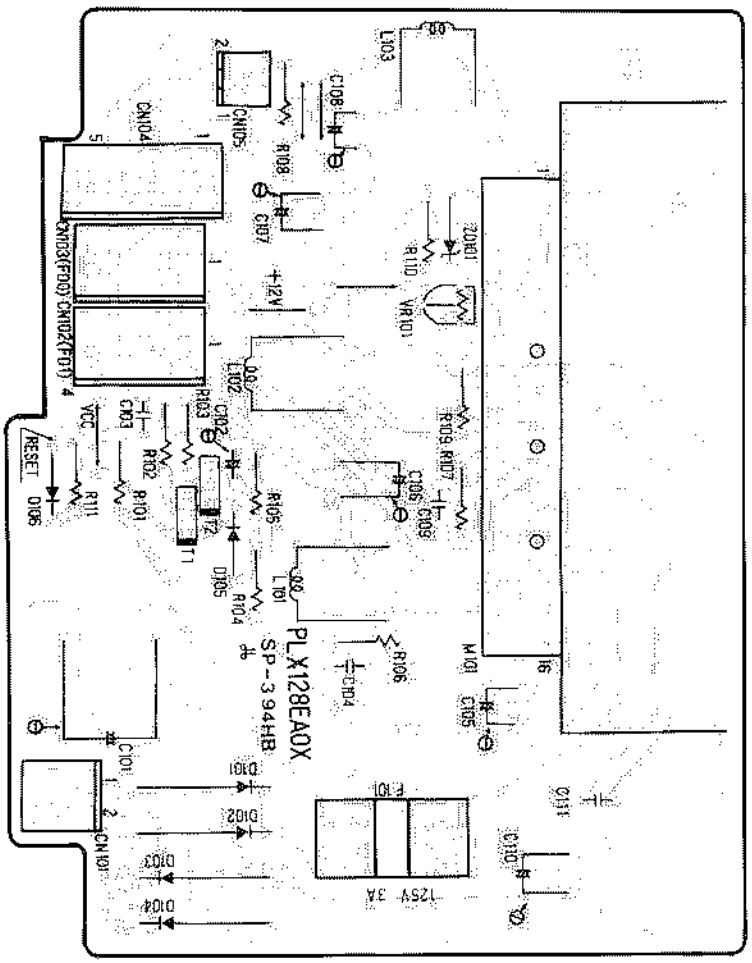


Figure 7-5. Power Supply P.C. Board (Top View)

Botton View

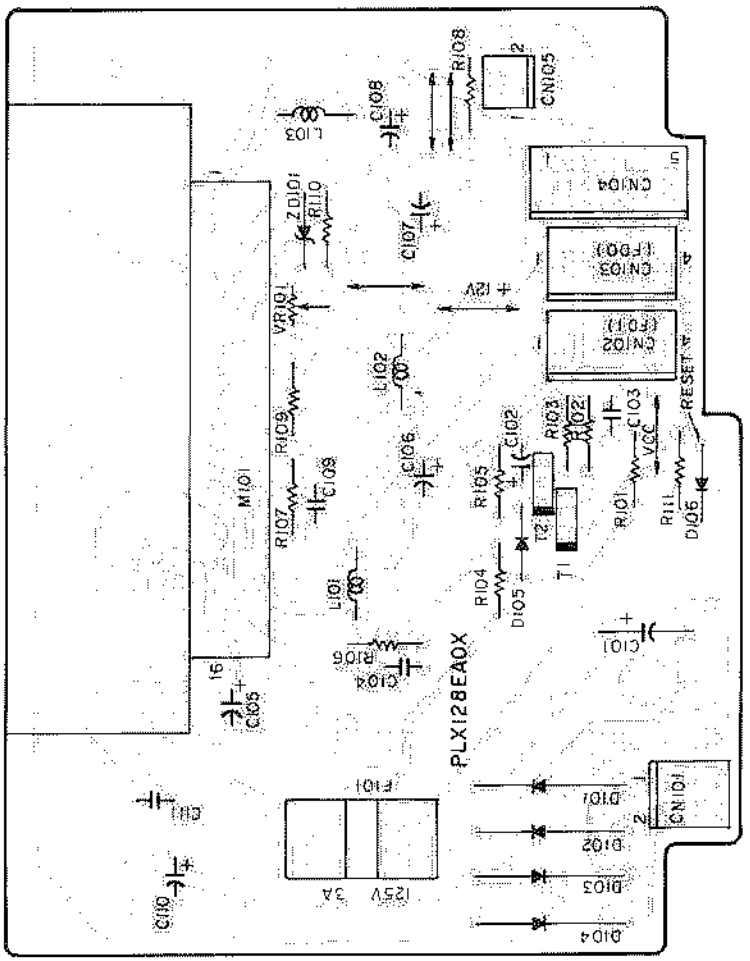
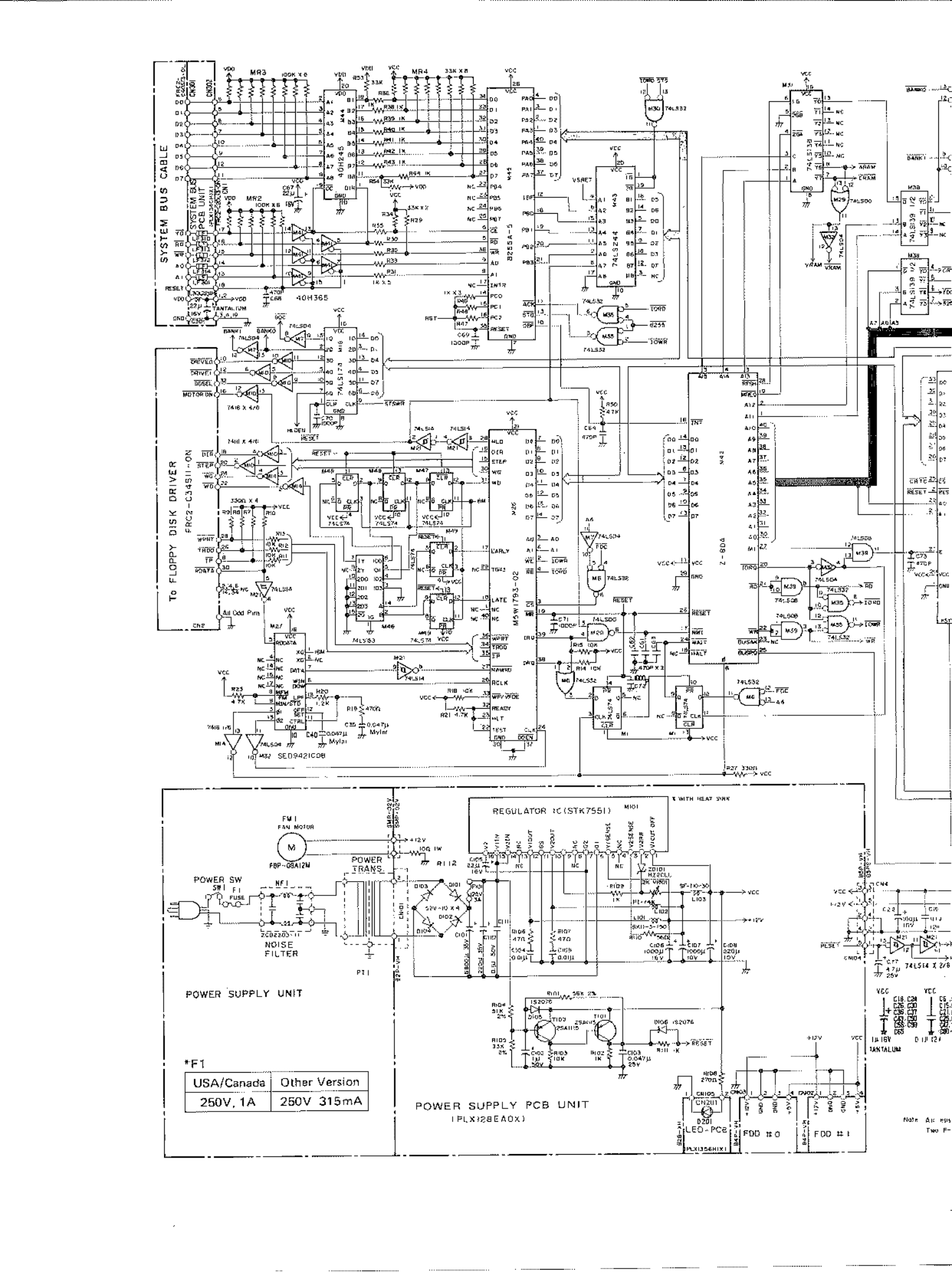
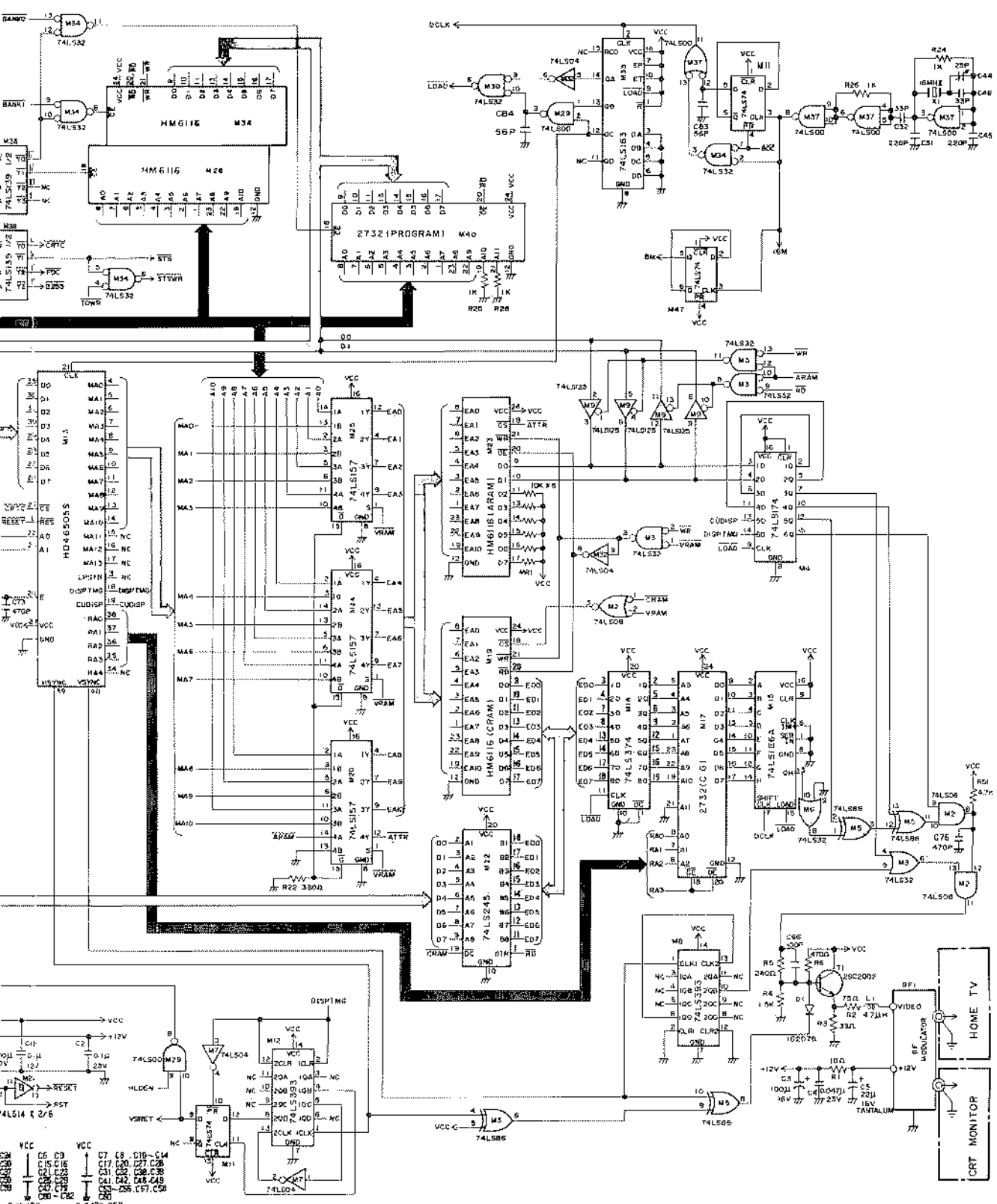


Figure 7-6. Power Supply P.C. Board (Bottom View)


SYSTEM BUS CABLE
To FLOPPY DISK DRIVER
POWER SUPPLY UNIT
POWER SUPPLY PCB UNIT
(PLX128EA0X)
REGULATOR IC(STK7551)
FAN MOTOR
POWER TRANS.
NOISE FILTER
POWER SW
FUSE
*F1
USA/Canada
Other Version
250V, 1A
250V 315mA
FDD #0
FDD #1
LED-PCB



MAIN PCB UNIT
(PLX133CH1X)

ote . All resisters denoted are 1/4W ±5% carbon resister
Two P-ROMS (27321 are with IC socket

Appendix A/Installation of Additional Disk Drive Unit

Before installing an optional disk drive, check the following two points for that disk drive.

1. Is a resistor array disconnected? If not, remove it from the 14-pin IC socket on the printed circuit board.
2. Is a terminating socket which determines a drive number inserted into the plug marked "DS1"? If not, remove the socket from the plug and reinsert it correctly.

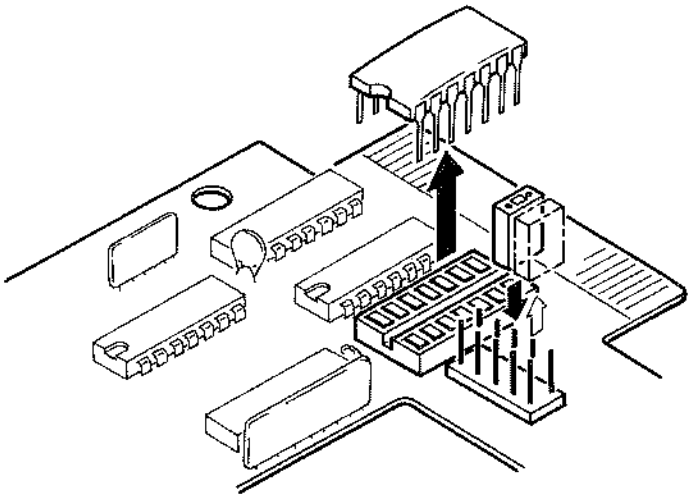


Figure A-1. Preparation on P.C.B. of FDD

Installation of the additional disk drive is as follows.

1. Remove the optional drive cover from the front panel with a thin blade knife.
2. Remove five screws (A) securing the ivory back cover and lift it away from the unit.
3. Fully insert the additional disk drive into the opening on the front panel and secure it with four 3ϕ x 6 mm screws (B) from the bottom of the unit.

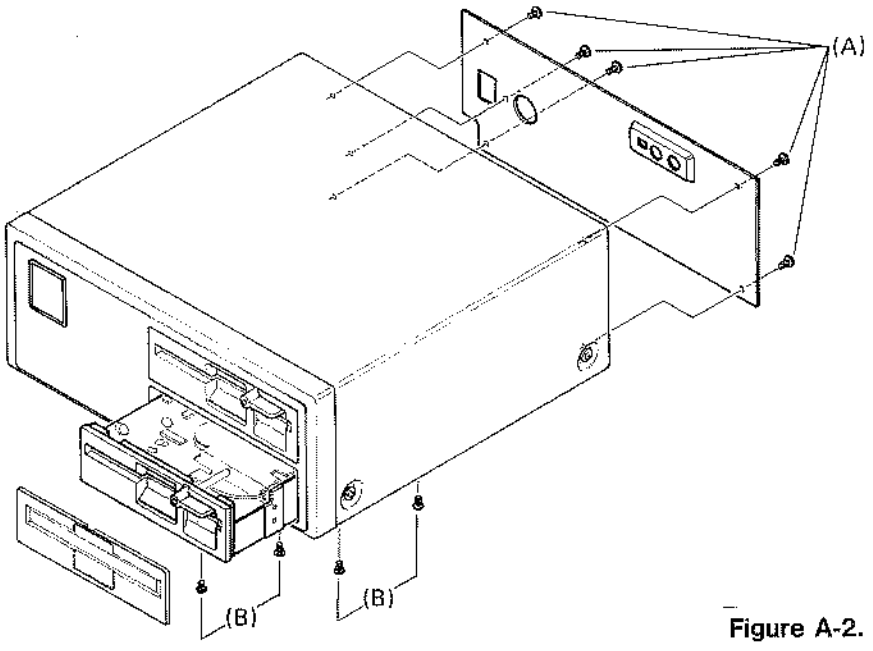


Figure A-2. Installation of FDD

4. Connect the power supply cables (ACN-5) to the connector on the disk drive and connect the FD signal cables (FD-1). These cables are already prepared inside the unit.

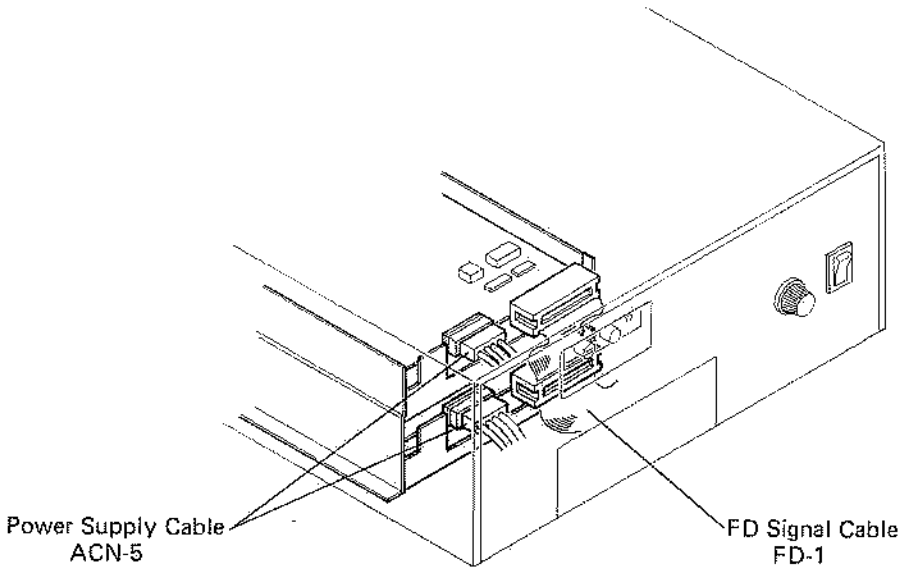


Figure A-3. Cable Connections

Appendix B/Connector Pin Assignments

System Bus Connector Pin Assignments

Pin No.	Symbol	Description
1	VDD	+5V Power supply from TRS-80 Model 100
2	VDD	+5V Power supply from TRS-80 Model 100
3	GND	Logic ground
4	GND	Logic ground
5	AD1	Address data signal bit 1
6	ADϕ	Address data signal bit ϕ
7	AD3	Address data signal bit 3
8	AD2	Address data signal bit 2
9	AD5	Address data signal bit 5
10	AD4	Address data signal bit 4
11	AD7	Address data signal bit 7
12	AD6	Address data signal bit 6
13	A9	Address signal bit 9
14	A8	Address signal bit 8
15	A11	Address signal bit 11
16	A10	Address signal bit 10
17	A13	Address signal bit 13
18	A12	Address signal bit 12
19	A15	Address signal bit 15
20	A14	Address signal bit 14
21	GND	Logic ground
22	GND	Logic ground
23	$\overline{WR}$*	Write enable signal
24	$\overline{RD}$*	Read enable signal
25	Sϕ	Status ϕ signal
26	IO/$\overline{M}$*	I/O or Memory signal
27	S1	Status 1 signal
28	ALE*	Address latch enable signal
29	$\overline{Y\phi}$	I/O Controller enable signal
30	CLK	2.54MHz Clock signal
31	RESET*	TRS-80 Model 100 reset signal
32	(A)*	Memory or I/O access enable signal
33	$\overline{INTA}$	Interrupt acknowledge signal
34	INTR	Interrupt request signal
35	GND	Logic ground
36	GND	Logic ground
37	NC	No connection
38	RAM RST	TRS-80 Model 100 RAM reset signal
39	NC	No connection
40	NC	No connection

Table B-1. System Bus Connector Pin Assignments

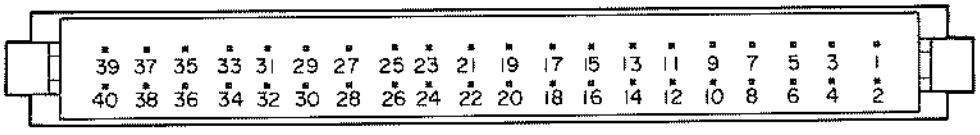
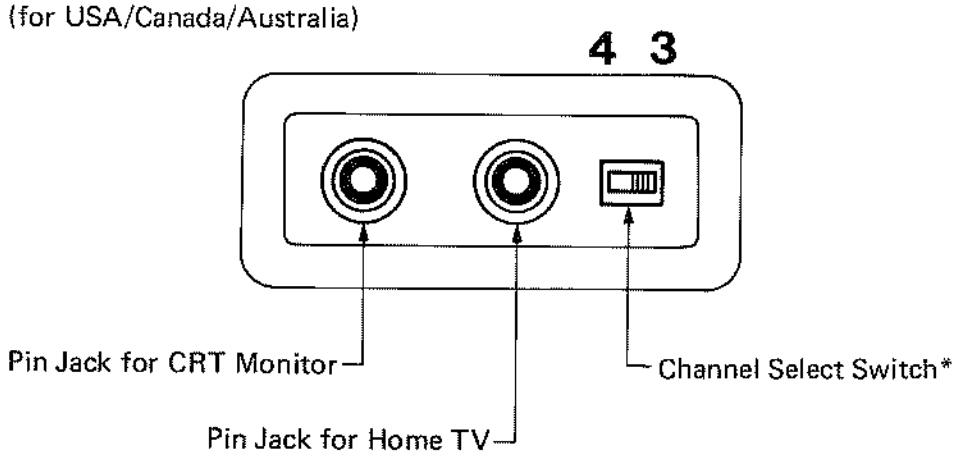


Figure B-1. System BUS Connector

RF Modulator

(for USA/Canada/Australia)



* Channel 2 and 1
for Australia version.

(for UK/Belgium)

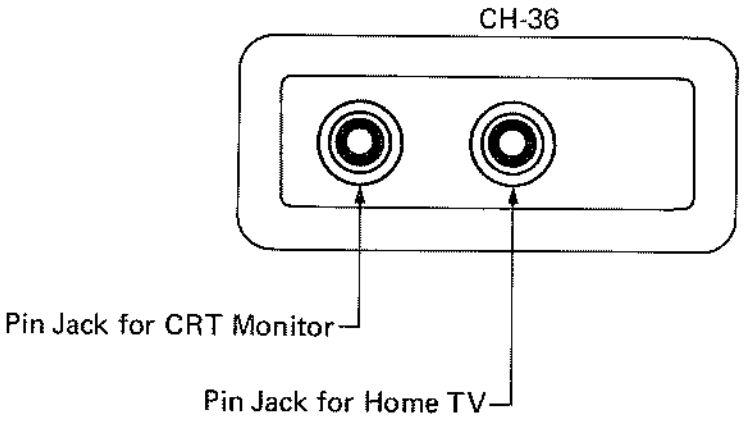


Figure B-2. RF Modulator

Appendix C/Servicing the Expansion FDD Unit

Part 1 Mechanical Section

1-1 Installation and Removal of Components

1-1-1 P.C. Board

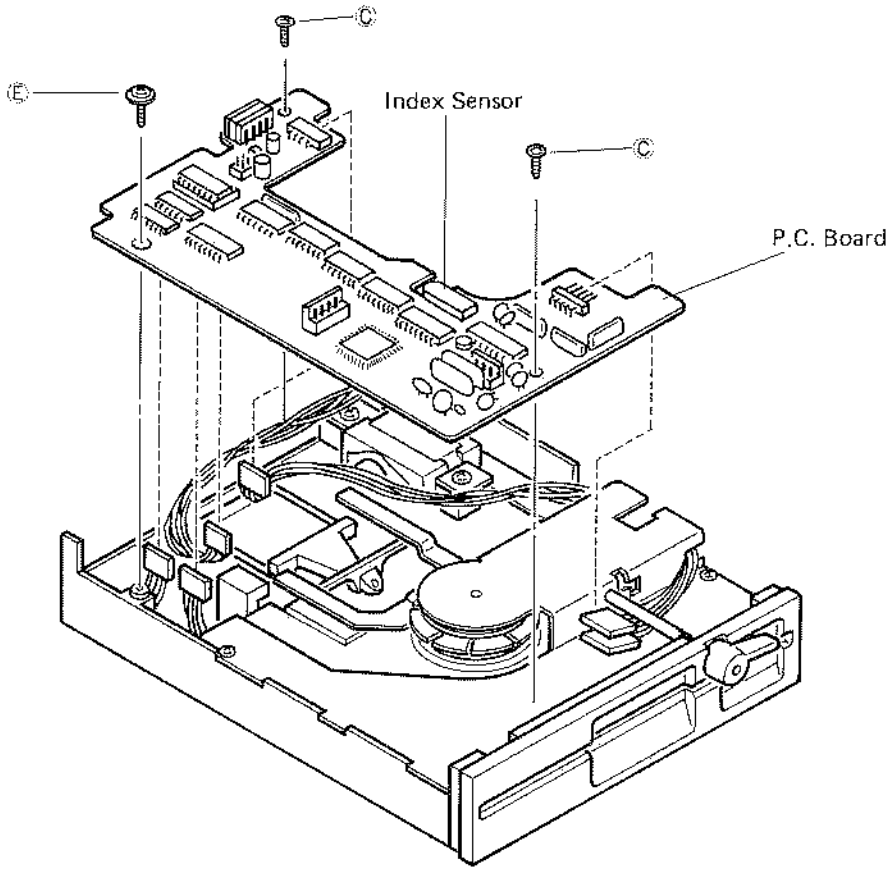


Figure C-1. P.C. Board Removal

To remove P.C. Board:

(1) Remove the three set screws (Ⓒ and Ⓔ) retaining the P.C. board to the base.
(2) Detach all the connector cables (Head, Step Motor, DD Motor, Zero Track Sensor).

To install the P.C. Board:

(1) Attach the connector cables to the P.C. Board.
Make sure that the connector cables are properly routed.
(2) Tighten the three set screws of the P.C. board.
(3) The write protector and index sensor are directly mounted on the P.C. board. The write protector requires no adjustment while it is necessary to adjust the index sensor whenever it is mounted on the P.C. board. The index sensor should be adjusted by referring to page C-7.

1-1-2 Clamp Base BK and Clamp Arm K

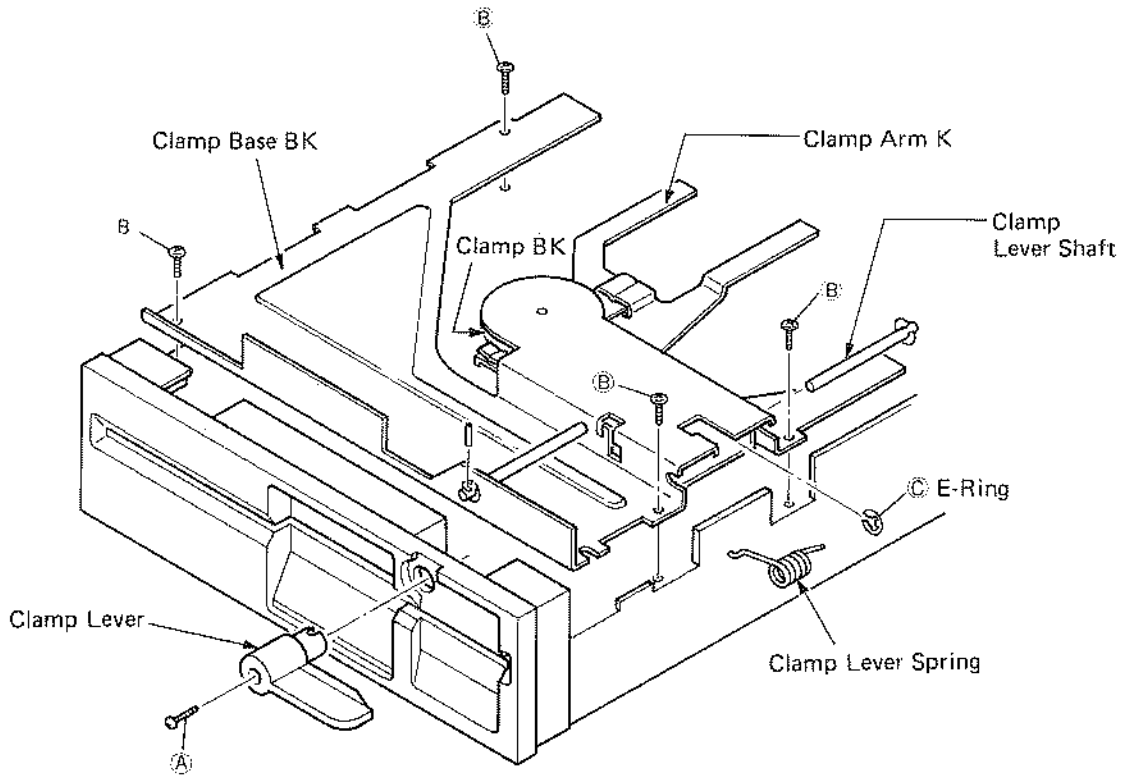


Figure C-2. Clamp Base BK and Clamp Arm K Removals

(1) Remove the P.C. board by referring to section 1-1-1 (page C-1).
(2) Remove the set screw Ⓐ retaining the clamp lever, and pull out the clamp lever from the shaft.
(3) Remove the four set screws Ⓑ retaining clamp base BK.
(4) Pull out the clamp lever shaft by removing the E-ring Ⓒ and clamp lever spring.
(5) In the above procedure, clamp arm K is separated clamp from base BK.
(6) Clamp BK can be removed by separating clamp base BK from the base and pushing down the clamp arm.
(7) Follow the above procedure in reverse for re-assembly.

1-1-3 Carrier BK

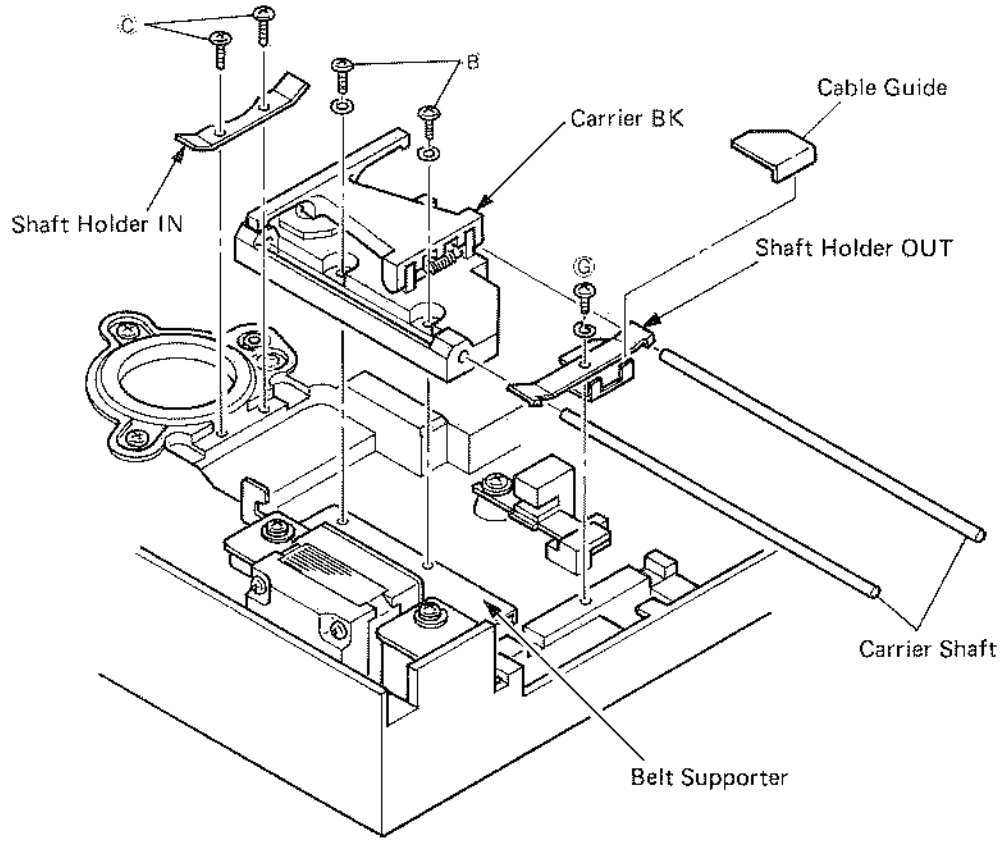


Figure C-3. Carrier BK Removal

(1) Remove the P.C. board by referring to section 1-1-1 (page C-1).
(2) Remove clamp base BK by referring to section 1-1-2 (page C-2).
(3) Remove the two screws Ⓑ connecting the belt supporter to carrier.
(4) Remove the head cable.
(5) Remove the set screws (Ⓒ and Ⓖ) of shaft holders OUT and IN, and remove the shaft holders OUT and IN.
(6) Remove both carrier shafts.
(7) When re-mounting the carrier, the adjustment required (see page C-11) must be performed.
(8) Follow the above procedure in reverse for re-assembly.

1-1-4 Pulse Motor BK

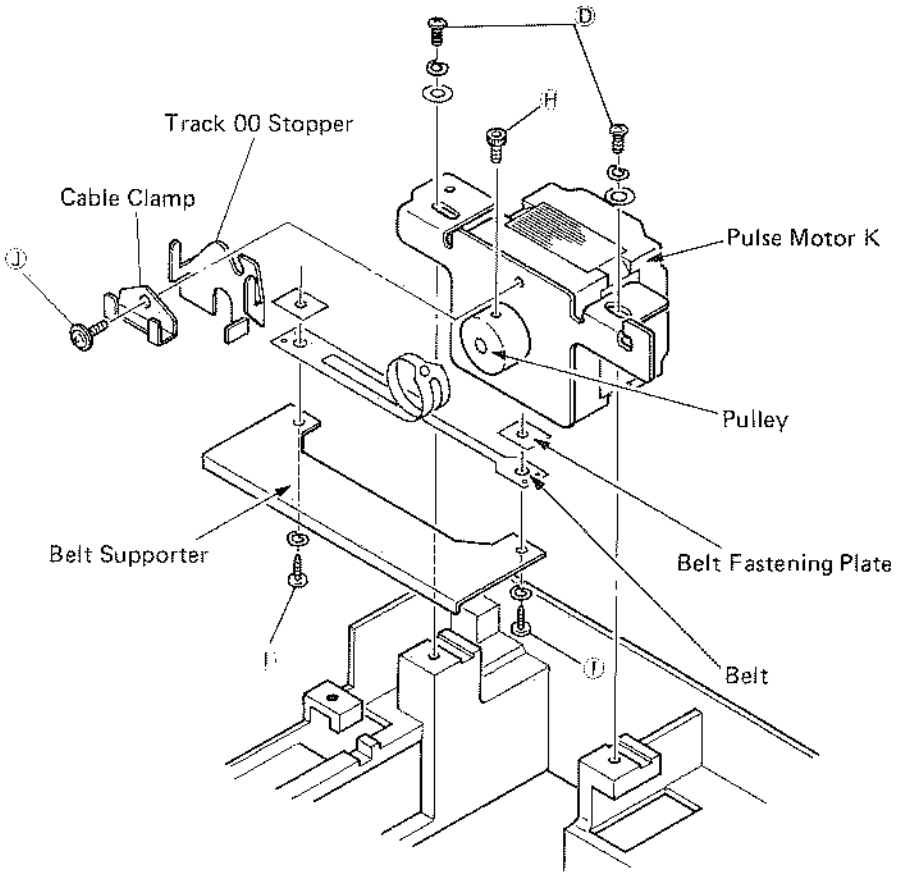


Figure C-4. Pulse Motor BK Removal

(1) Remove carrier BK from the base by referring to section 1-1-3 (page C-3).
(2) Remove the screws Ⓓ positioning and retaining pulse motor K.
(3) Remove the set screws Ⓘ of the belt supporter.
(4) Remove the pulley set screw Ⓗ of the pulley, which is retaining the belt.
(5) Follow the above procedure in reverse for re-assembly, after adjusting the steel belt tension. (see page C-8)

1-1-5 Spindle Motor K

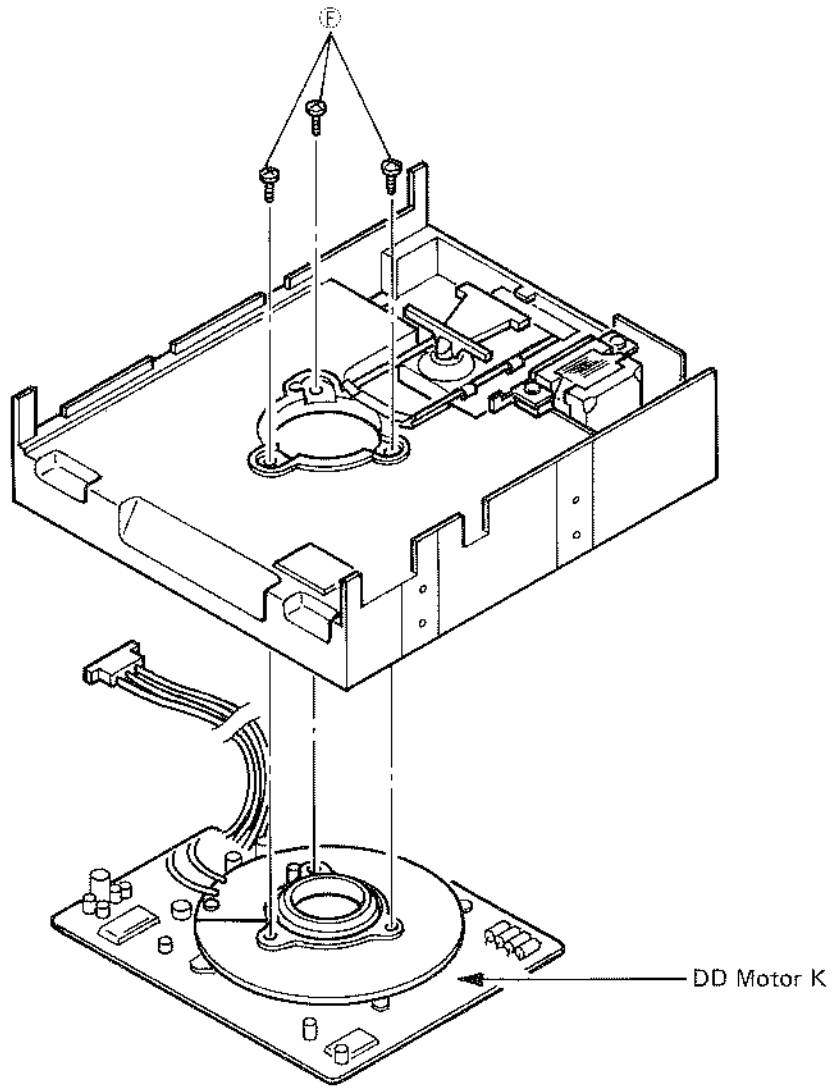


Figure C-5. Spindle Motor K Removal

(1) Remove the P.C. board by referring to section 1-1-1 (page C-1).
(2) Remove clamp base BK by referring to section 1-1-2 (page C-2).
(3) Remove the three set screws Ⓕ holding the spindle.
(4) Follow the above procedure in reverse for re-assembly.

1-1-6 Track Sensor

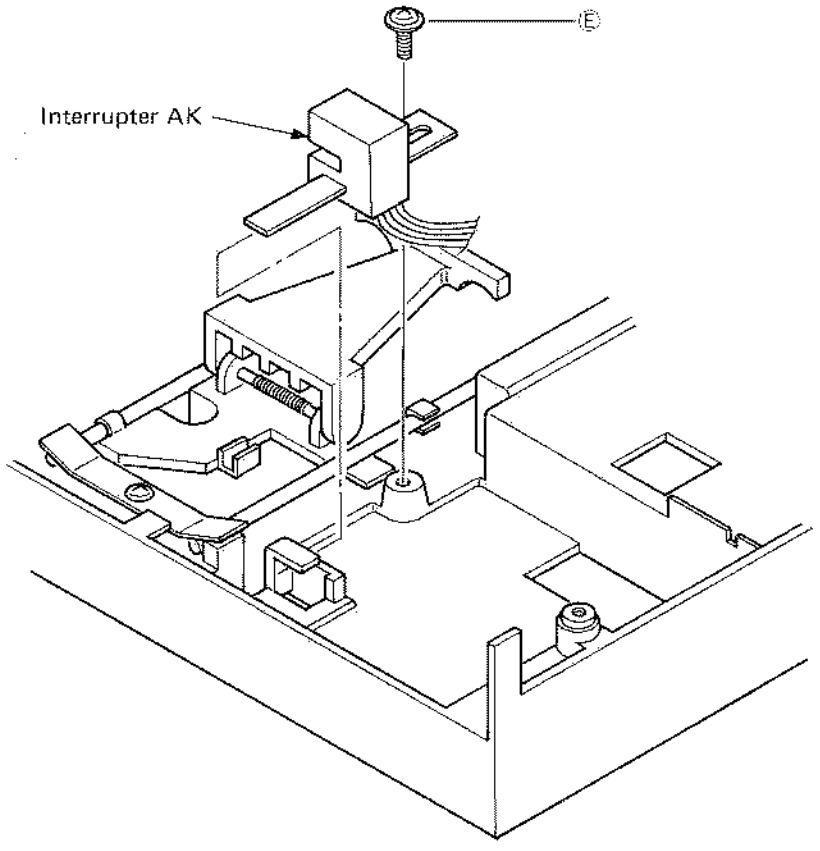


Figure C-6. Track Sensor Removal

(1) Remove the P.C. board by referring to section 1-1-1 (page C-1).
(2) Remove the positioning set screw Ⓔ of interrupter AK.
(3) Remove the interrupter.
(4) Temporarily tighten the positioning set screw when mounting the interrupter.
(5) Perform the Track 00 adjustment in Page C-13.

1-2 Adjustment

1-2-1 Index Sensor Adjustment

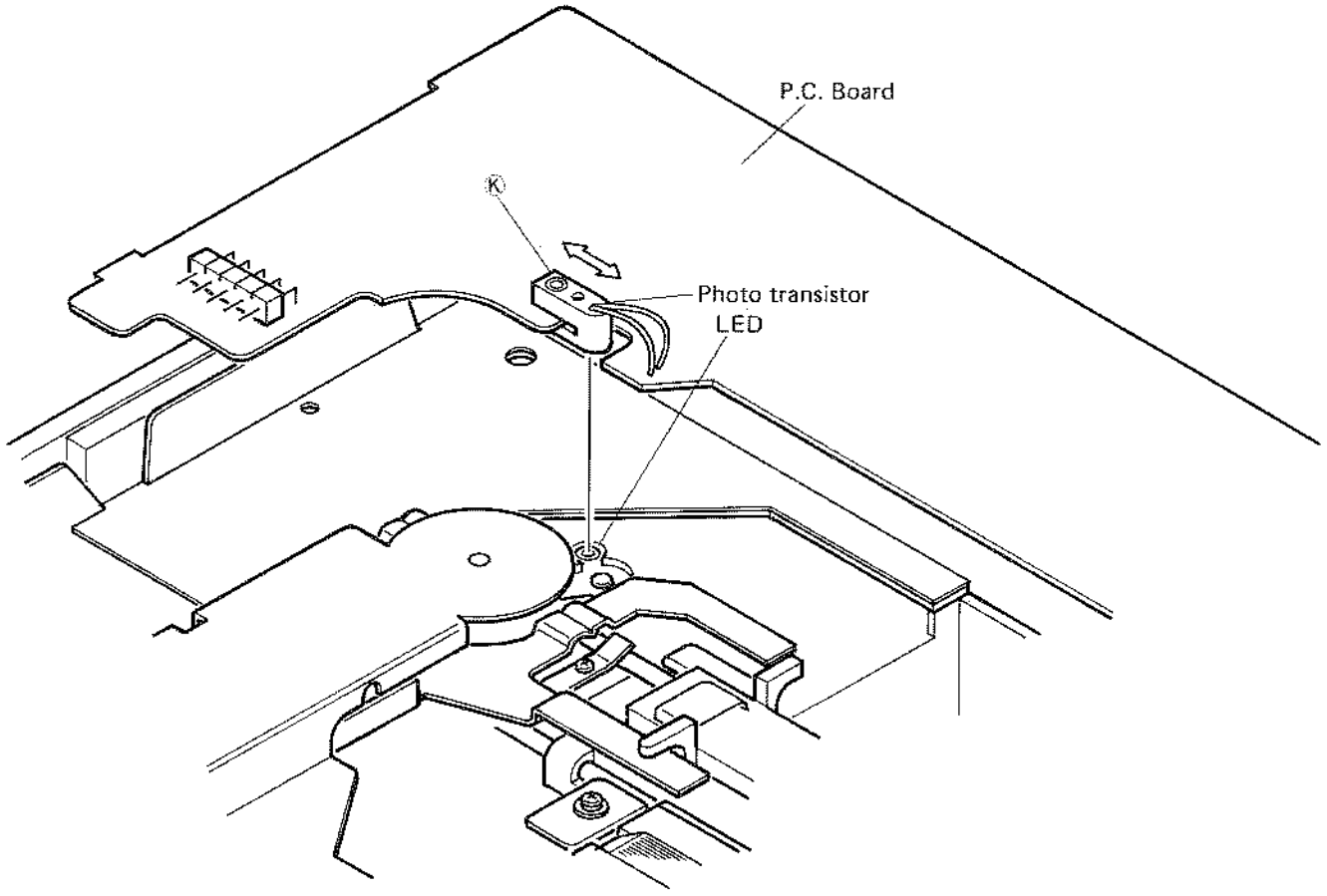


Figure C-7. Index Sensor Adjustment

(1) The index sensor optically detects the index hole of the disk.

(2) Adjust the index sensor in the following manner.

a. The LED of the index sensor is built in the DD motor K, thus, it cannot be adjusted in position.

b. The photo transistor is adjusted by loosening the socket screw Ⓚ .

c. Use an alignment diskette. The alignment diskette usually stores the index burst signal on two tracks, the outer track and inner track.

d. Connect the CH1 probe of the oscilloscope to pin 4 of TP-2, and the CH2 probe to pin 3 or 4 of TP-1. Connect the GND to pin 2 of TP-1 or pin 5 of TP-2. (CH level: 40 mV/div. d.c., time base: 50 μs/div.)

e. The index burst signal appears as follows:

Outer Track: Within 200 μs ± 100 μs

Inner Track: Within above ±50 μs

f. Move and adjust the transistor in position to meet the above values.

1-2-2 Tensioning and Adjustment of Steel Belt

(1) Leave the pulse motor K only by referring to the section on pulse motor BK removal (page C-4).

(2) Wind the steel belt on the pulley as shown in the left figure below, and temporarily fix it with the belt stopper and mounting screw ㊧ . Manually turn the pulley until the mounting screw ㊧ faces downward as shown in the right figure below.

Caution: Be sure to wear gloves when touching the steel belt.

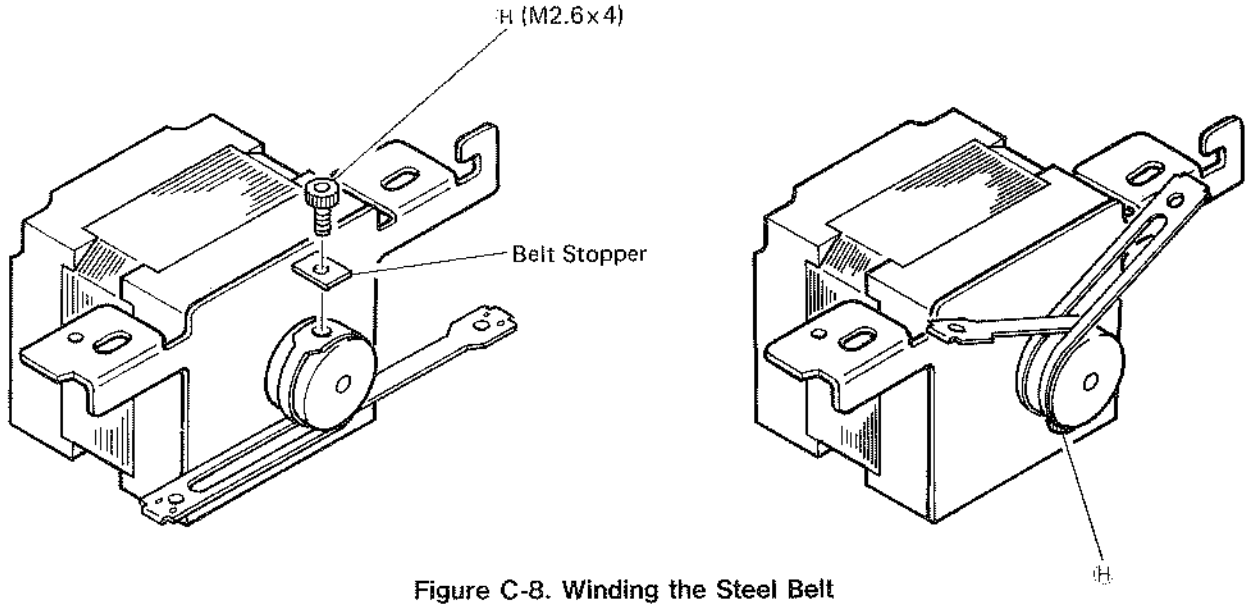


Figure C-8. Winding the Steel Belt

(3) Put the right and left ends of the steel belt between the belt supporter and belt holder plate as shown in the figure below, and temporarily fix them with the mounting screws ㊨ (2 pcs).

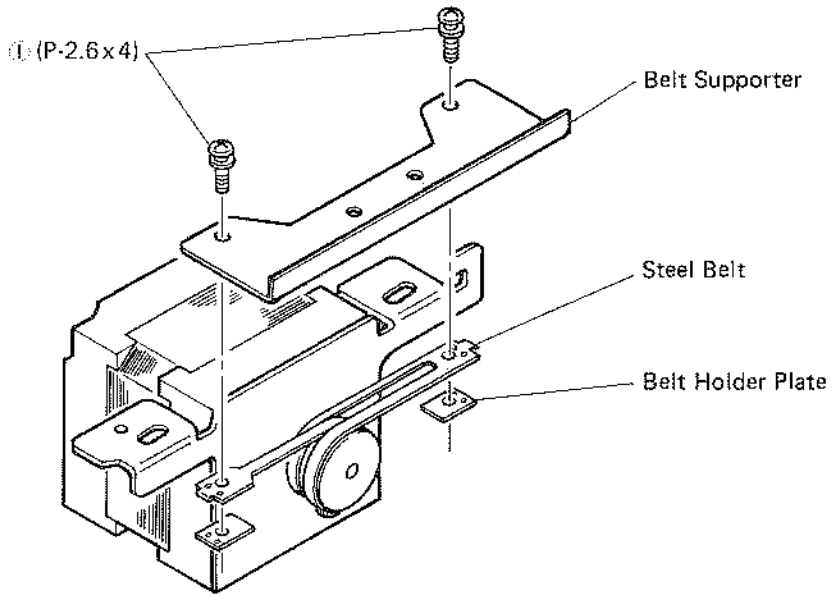


Figure C-9. Mounting the Belt Supporter

(4) Turn the lever of the jig until it is set horizontal as shown in the figure below. Then place the pulse motor K on the jig, allow the jig pins to be inserted into the right and left holes in the steel belt, and mount the pulse motor K on the jig with the mounting screws Ⓓ (2 pcs).

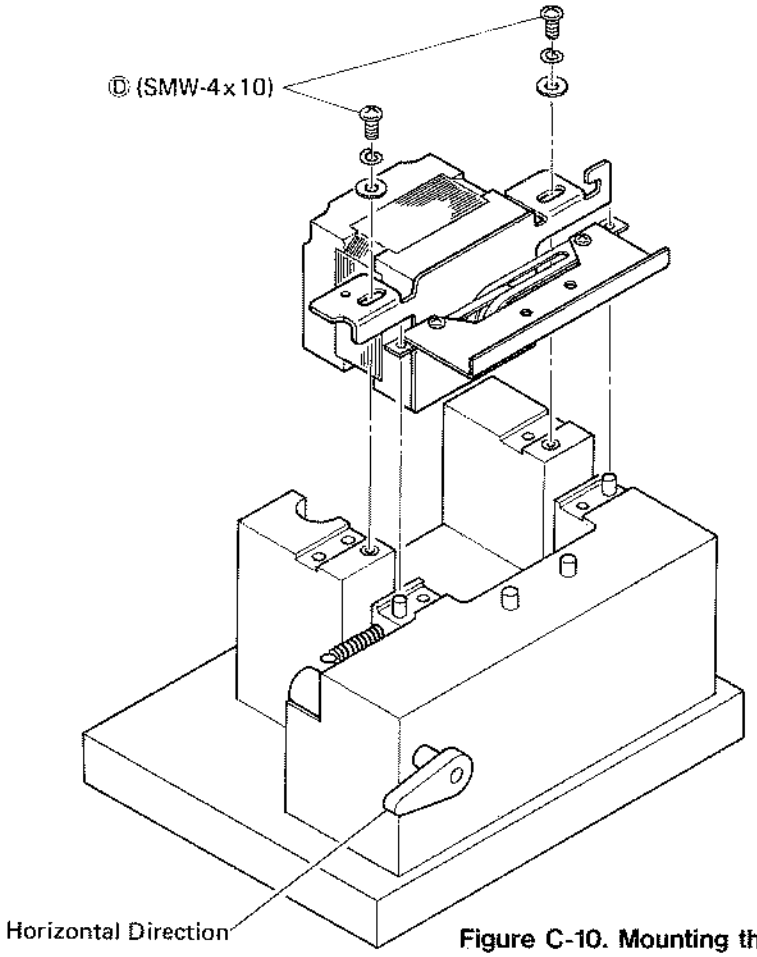


Figure C-10. Mounting the Pulse Motor K

(5) Turn the lever of the jig until it is set vertical to tension the belt, and tighten the mounting screws Ⓘ (2 pcs).

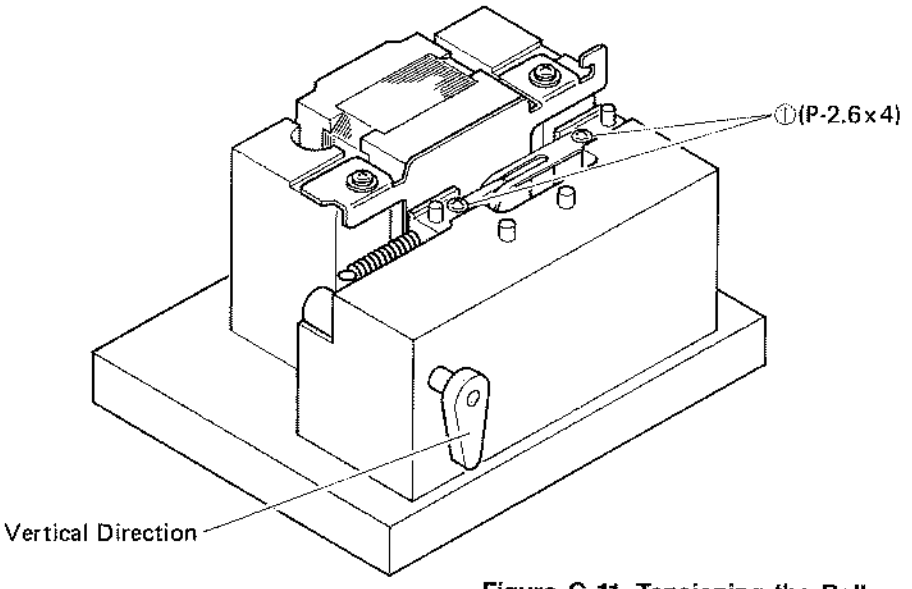


Figure C-11. Tensioning the Belt

(6) Turn the lever of the jig until it is set horizontal again. Then remove the mounting screws Ⓓ (2 pcs), and remove the pulse motor K from the jig.

(7) Tighten the mounting screw Ⓗ. Check that the steel belt gaps Ⓐ and Ⓑ are uniform when the belt supporter is slided horizontally to the right or left.

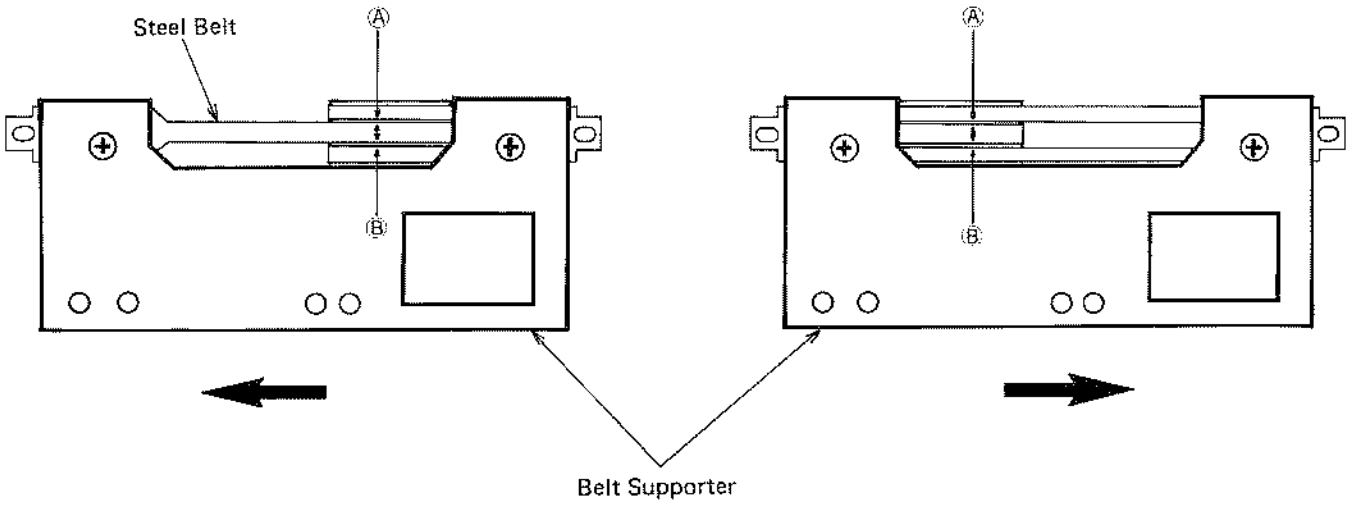


Figure C-12. Confirmation of the Belt Gaps

(8) Manually turn the pulley until the mounting screw Ⓗ faces upward. Temporarily fix the track 00 stopper with the mounting screw Ⓙ.

Finally, tighten the nut and spring washer in the original state.

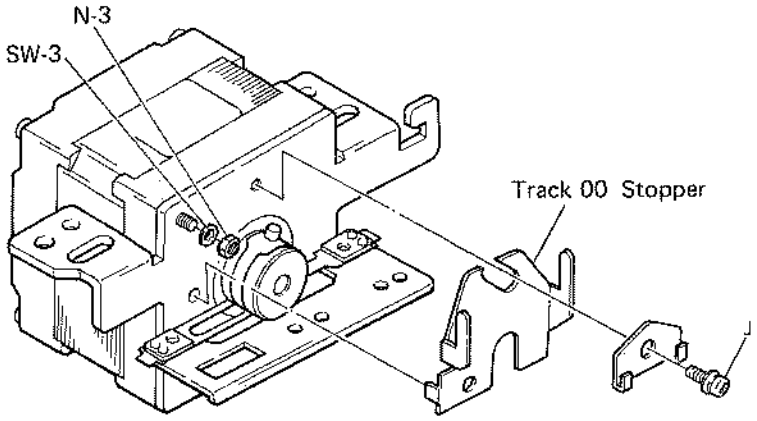


Figure C-13. Fixing the Track 00 Stopper

1-2-3 Head/Radial Adjustment (CE Adjustment)

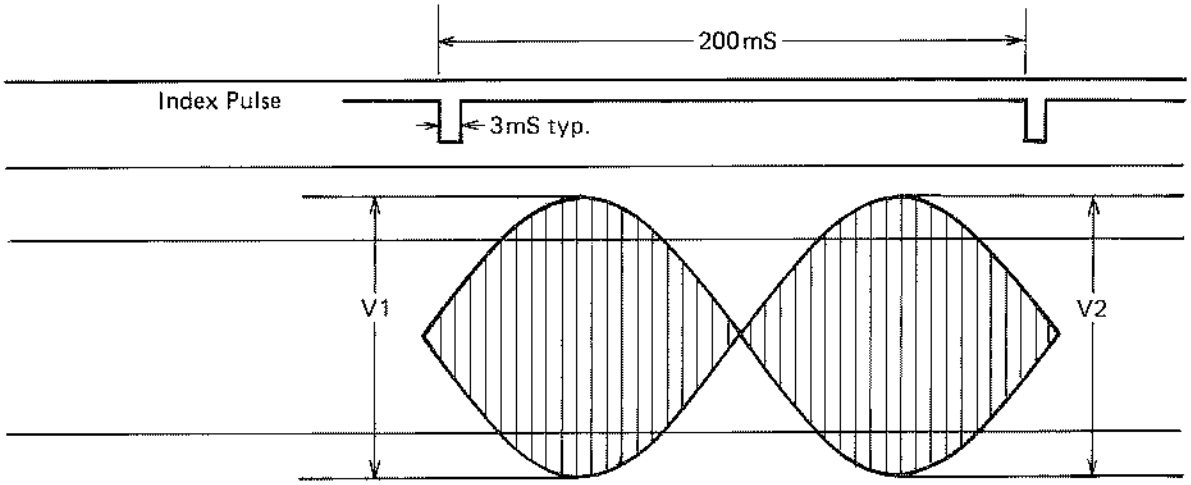


Figure C-14. Waveform of Index Pulse

(1) Measure and adjust the reproduced signal waveform of track 16 of an alignment disk.
Set the switches on oscilloscope as follows:
CH Level: 50 mV/div. DC
Time Base: 20 mS/div.
At this time, observe the waveform by moving the carrier from outer side and inner side.
(2) Obtain the waveform shown above.
(3) Externally trigger the fall of the index signal of pin 4 of TP-2.
The waveform should be stationary.
(4) Connect CH1 to pin 3 of TP-1, and CH2 to pin 4 of TP-1, and GND to pin 2 of TP-1 or pin 5 of TP-2.
(5) A temperature and humidity correction table is provided for the alignment disk in each manufacturer.
Adjust the measured value according to the table.

Measurement Reference

$100\% \geqq (V1/V2 \text{ or } V2/V1) \times 100\% \geqq 85\%$

Adjust to obtain the result of either of the above expressions.

Adjustment Points

Make adjustments by moving the pulse motor to the right or left.

1-2-4 Head Output Check

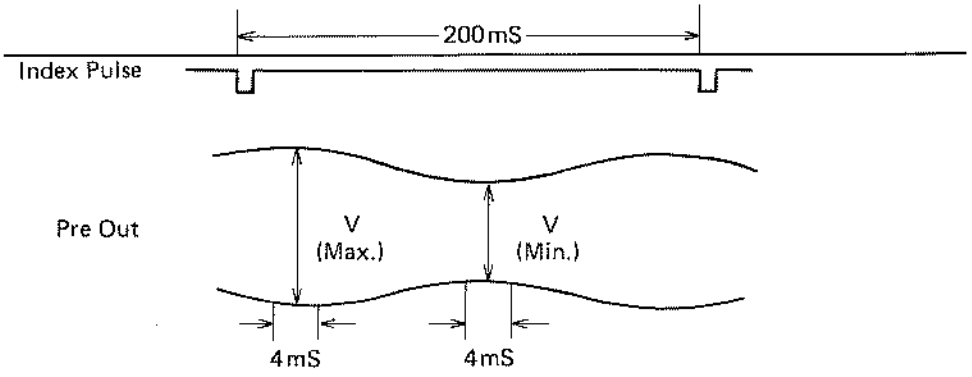


Figure C-15. Waveform of Head Output

Follow the procedure below to adjust the head output.

(1) Use a disk which is normal and erased enough to detect any fault in the head.
(2) Start the motor.
(3) Write 2F signals on track 00 and track 39, and reproduce them.
Read the reproduced signal waveforms with the synchroscope.
(4) Obtain the waveform shown above.
Use a synchroscope with two channels and an external trigger function.
(5) Connect the external trigger to pin 4 of TP-2 (5V/div., d.c.), and synchronize on the fall of the signal. Connect other channels 1 and 2 to pin 3 of TP-1 and pin 4 of TP-1 as the ground for each probe.
Set to ADD mode, set either pin 3 or 4 of TP-1 to INVERT, and set the time base at 20 ms/vis. Measure the average value of an area of at least 4 milliseconds as shown in Figure C-15.
(6) The adjustment criteria is 650/420 mVp-p with the 2F signal on track 39.
(7) Modulation: M

$$M \leqq 10\% \qquad M = \left(\frac{Vmax. - Vmin.}{Vmax. + Vmin.}\right) \times 100\%$$

1-2-5 Motor Speed Check

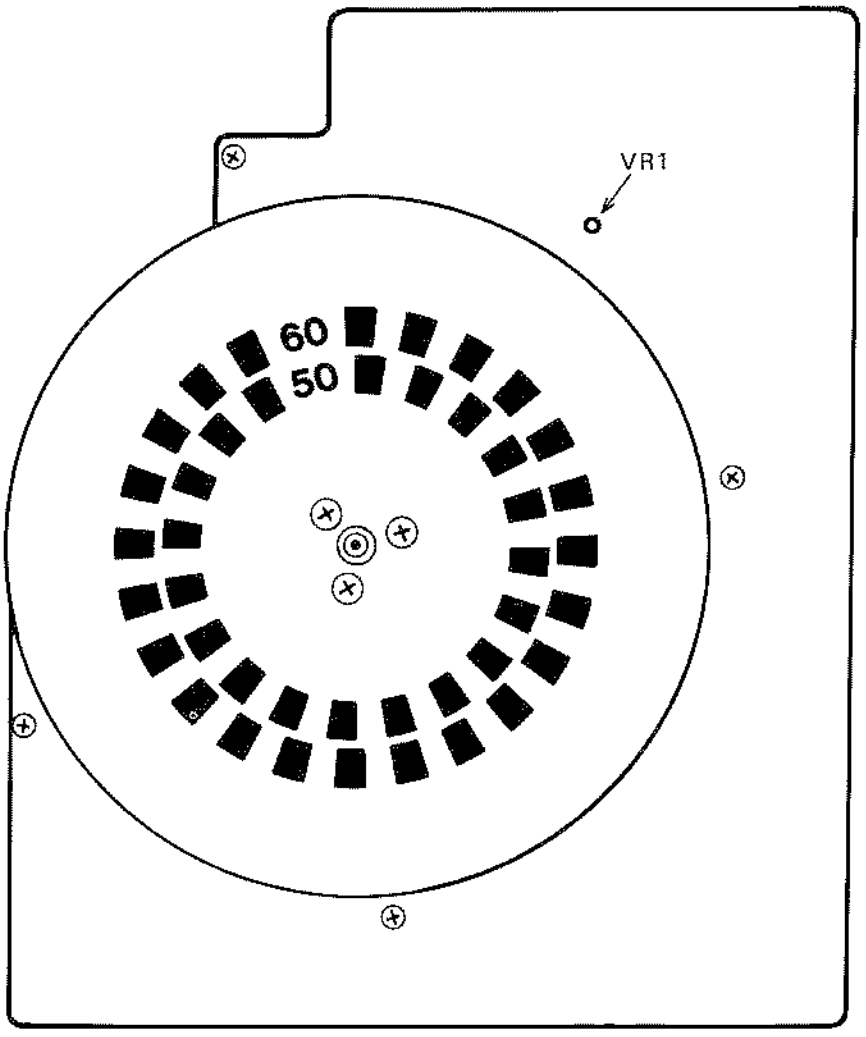


Figure C-16. Motor Speed Adjustment

(1) Insert the media after the motor ON signal is input.
(2) Adjust VR1 on the DD motor control PC board so that the black stripe of the stroboscope of the DD motor looks stationary under a 50-Hz or 60-Hz-fluorescent lamp.
The DD motor used is shown in Figure C-16.

1-2-6 Track 00 Adjustment

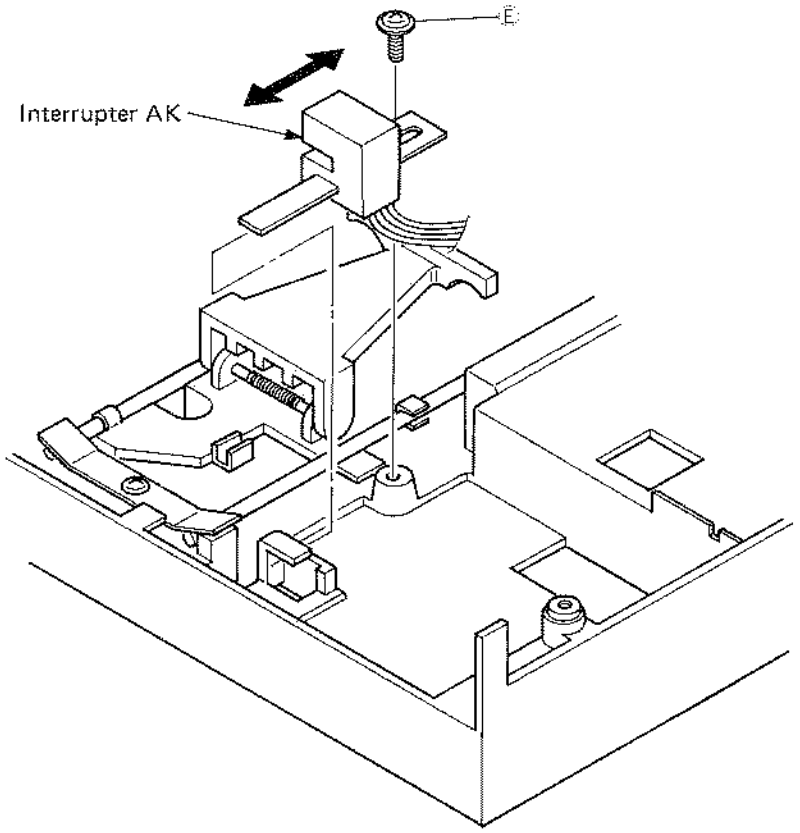


Figure C-17. Track 00 Adjustment

(1) Make this adjustment after the CE is adjusted.
(2) Point to which Probes are connected:
Connect CH-2 to pin 1 of TP-2, and CH-1 to pin 2 of TP-2.
Pin 4 of TP-1 is connected to GND. The rise of the STEP signal emitted from pin 1 of TP-2 is synchronized.
(3) Set the oscilloscope as following condition:
Mode set to chop
Volts set to 2V/div.
Time set to 1 mS/div.
(4) Connect an exerciser to the FDD unit.
Set the exerciser to generate STEP pulses at 6 mS rate to allow the carrier to continuously move between track 0 and track 2. (The timer for ST motor reverse should be 21 mS minimum.)

(5) Loosen the Interrupter AK fixing Screw Ⓔ, and position the interrupter until the below waveforms are obtained. After adjustment, tighten the fixing screw Ⓔ.

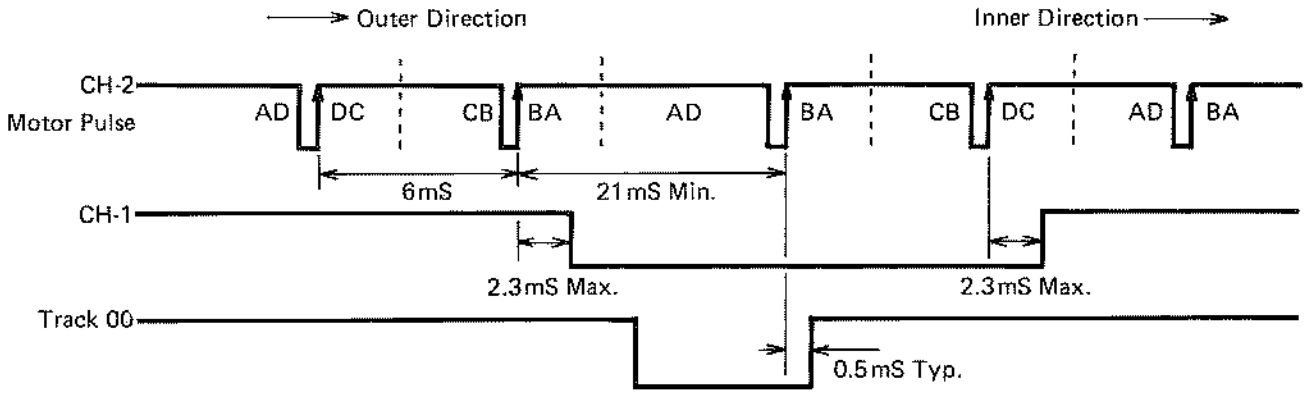


Figure C-18. Interrupter Timing Chart

1-3 Special Maintenance Tools

The following special tools are used for maintenance.

Name	
Oscilloscope	30 MHz
Simulator	(Example: BRIKON)
DC power supply	+12V, +5V
Alignment Diskette	
Flat-blade Screwdriver	
Exerciser	

1-4 Maintenance

1-4-1 Procedure for Cleaning the Read/Write Head

Only the floppy disk head cannot be replaced, since it is completely bonded to the carrier.
The had should be cleaned when dust and dirt particles are found.
Note that any other cleaning method than the one described below may cause damage to the head.

(1) Slightly dampen and cotton swab with isopropyl alcohol.
(2) Part the load arm from the head without touching the load button.
(3) Softly wipe the head with the dampened part of the cotton swab.
(4) After the alcohol has fully evaporated, softly polish the head with a clean cotton swab.
(5) Place the load arm on the head. At this time, extreme caution should be exercised to avoid shocks to the head.

1-4-2 Caution on Handling Disks

(1) Avoid directly touching the Mylar*.
(2) Avoid storing disks in locations with high temperature or high humidity.
(3) Always ensure that the disk is inserted properly.
(4) Avoid magnetic fields (i.e., AC motors, magnetics, etc.)
(5) Do not bend the disk.

* Mylar is a registered trademark of E.I. Du Pont de Nemours and Company.

Part 2 Electrical Section

2-1 General Description

This circuit uses two independent LSIs: the LSI that controls the signals from the pulse motor, DD motor, and the sensors: and the LSI for the read circuit — thus, realizing an increase in packaging density, compaction of the unit, powersaving and improved reliability.

2-2 Block Diagram

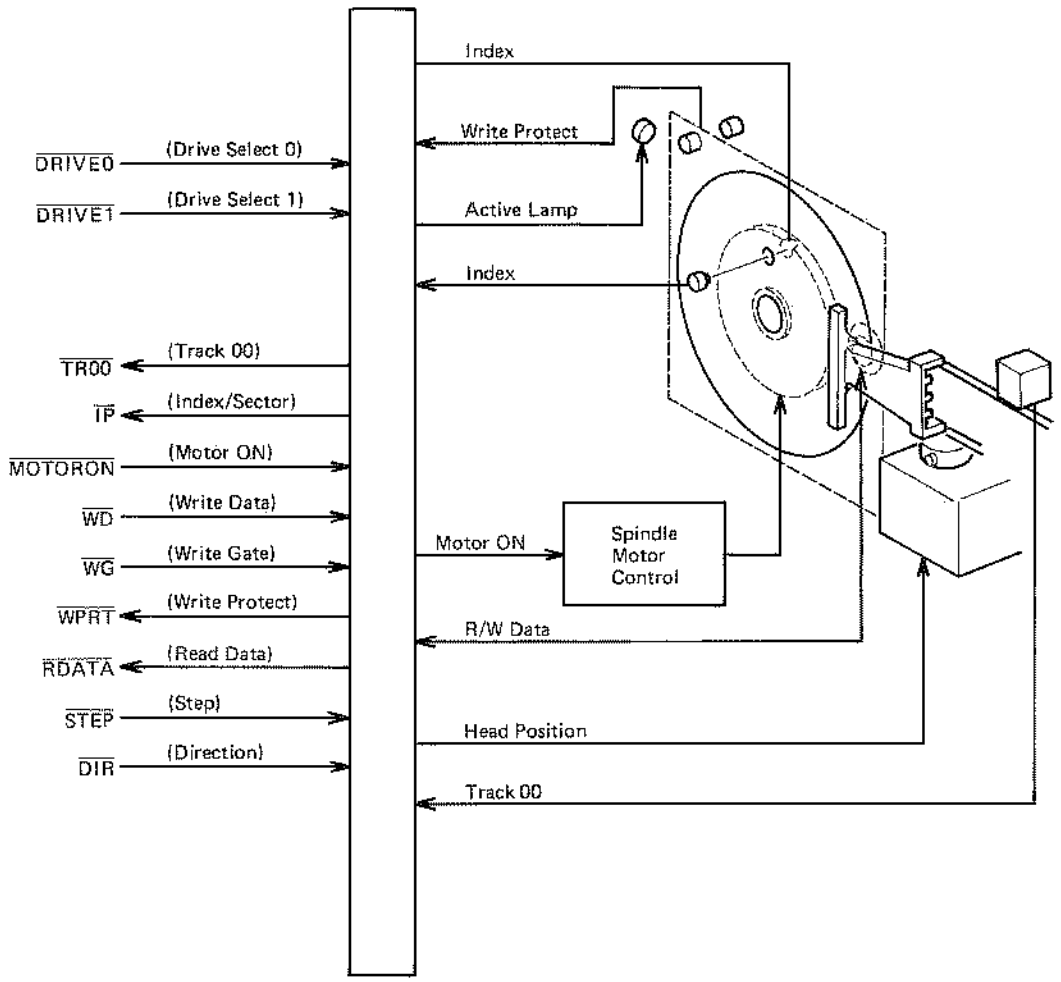


Figure C-19. Block Diagram

2-3 Electrical Diagram

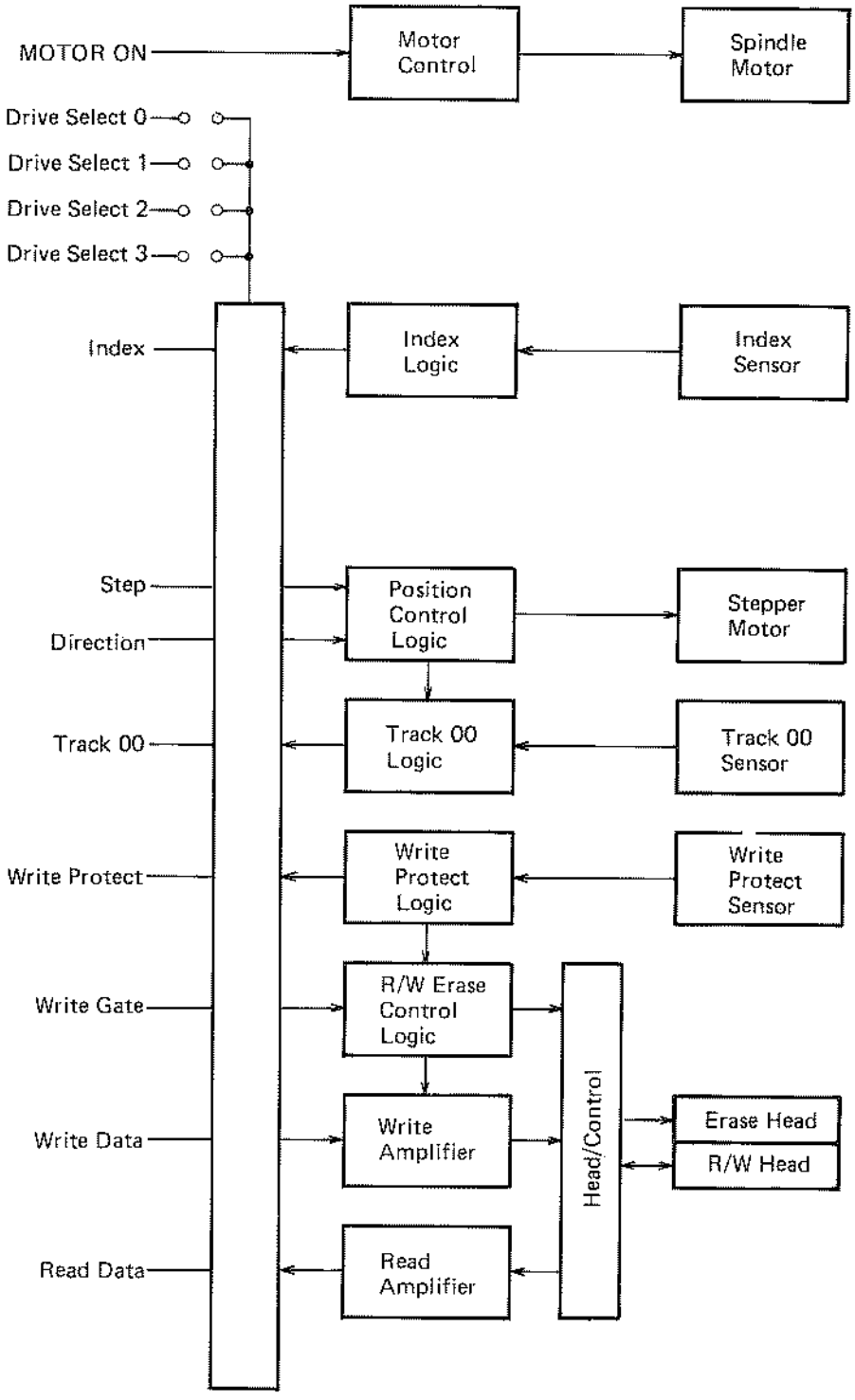


Figure C-20. Electrical Diagram

2-4 Independent LSI Configuration

2-4-1 Control LSI and Pin Names

Provided with the same functions as a custom one-chip LSI, this independent LSI is designed considering the hard timing required by the flexible disk drive (hereinafter referred to as FDD).
The package is compact and operated from a single +5V supply. All the pins are TTL-compatible. This LSI mainly controls the logic system.

Pin Configuration

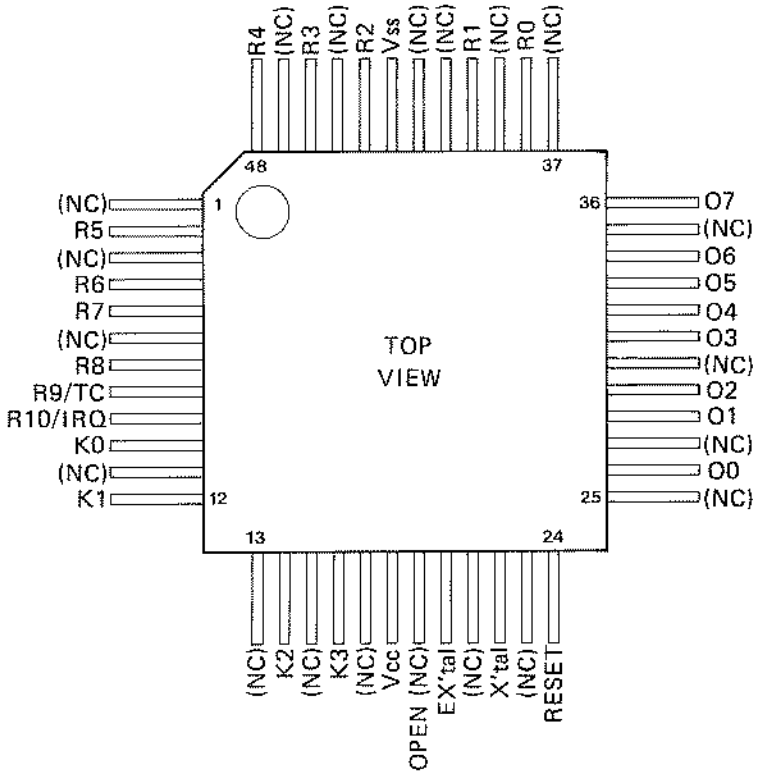


Figure C-21. Pin Configration of Control LSI

Block Diagram (EC-877)

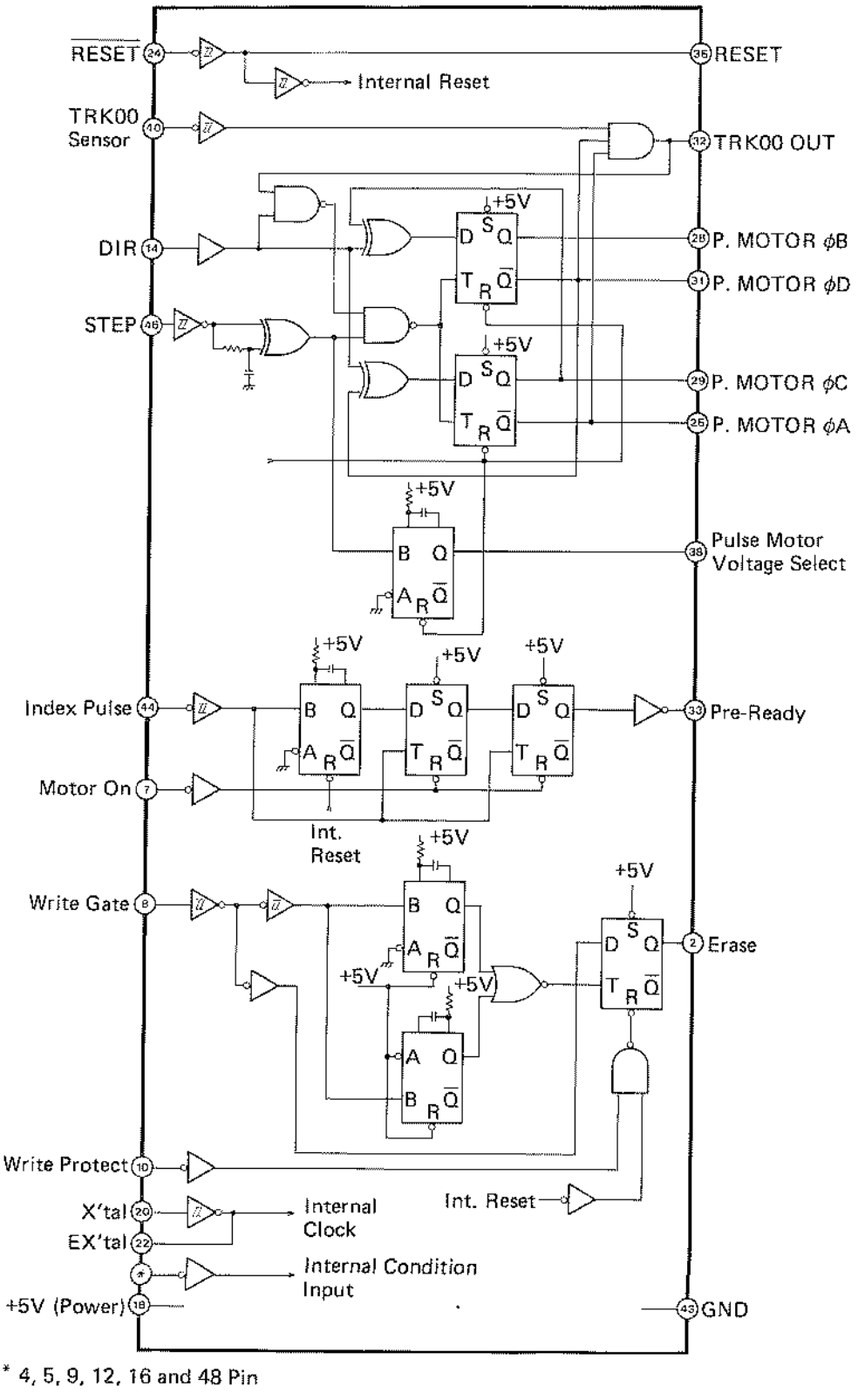


Figure C-22. Block Diagram of Control LSI

Pin Names

Pin Number	Pin Name	Pin Function
2	R5	Erase Gate
5	R7	Write Gate Signal Start and End Judgement
7	R8	External Motor Rotation
8	R9	Write Gate
9	R10	Write Gate Edge
10	K0	Write Protect
14	K2	Direction
16	K3	Side One Select
18	VCC	+5V
20	EX'tal	Terminals for External Crystal
22	X'tal	Terminals for External Crystal
24	$\overline{\text{RESET}}$	$\overline{\text{Reset}}$
26	00	Pulse Motor Phase A
28	01	Pulse Motor Phase B
29	02	Pulse Motor Phase C
31	03	Pulse Motor Phase D
32	04	Track 00 External Output
33	05	Ready
36	07	Soft Reset
38	R0	Pulse Motor Voltage Select
40	R1	Track 00 Position
43	VSS	GND
44	R2	Index
46	R3	Step

Table C-1. Pin Assignments of Control LSI

2-4-2 Read LSI Configuration and Pin Names

This LSI is a monolithic read amplifier that outputs signals recorded on the floppy disk in the form of digital signals. The LSI amplifies signals from the magnetic head and passes them through the filter. Then, it passes them through the differentiator, zero volt comparator and waveform shaper to obtain pulse outputs.

Floppy Disk read processing is performed by one IC. The output can be directly connected to a TTL device.

Pin Configuration

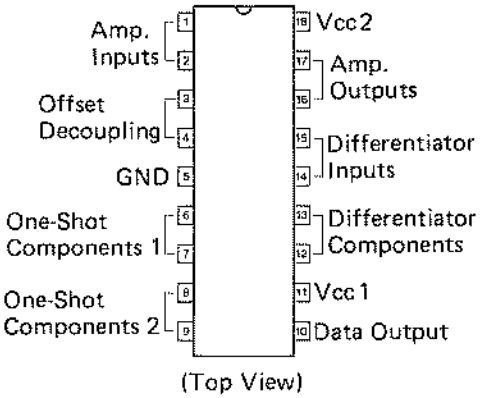


Figure C-23. Pin Configuration of Read LSI

Block Diagram

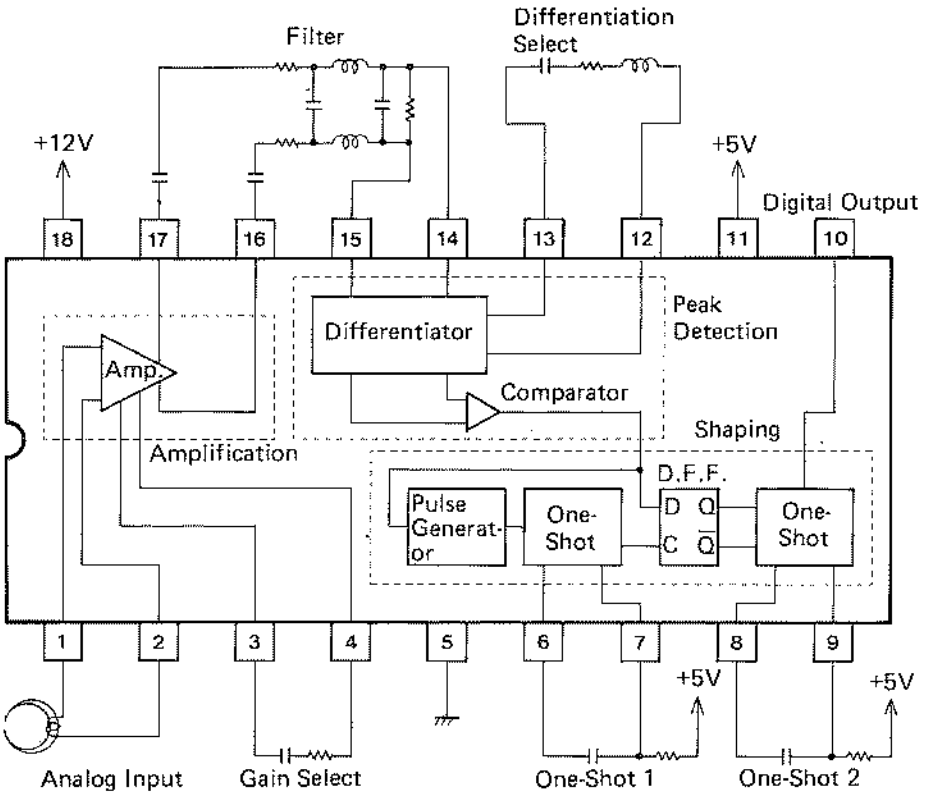


Figure C-24. Block Diagram of Read LSI

2-5 Input Signal Lines (CPU to FDD)

2-5-1 Drive Select Circuit and Indicator LED on Circuit

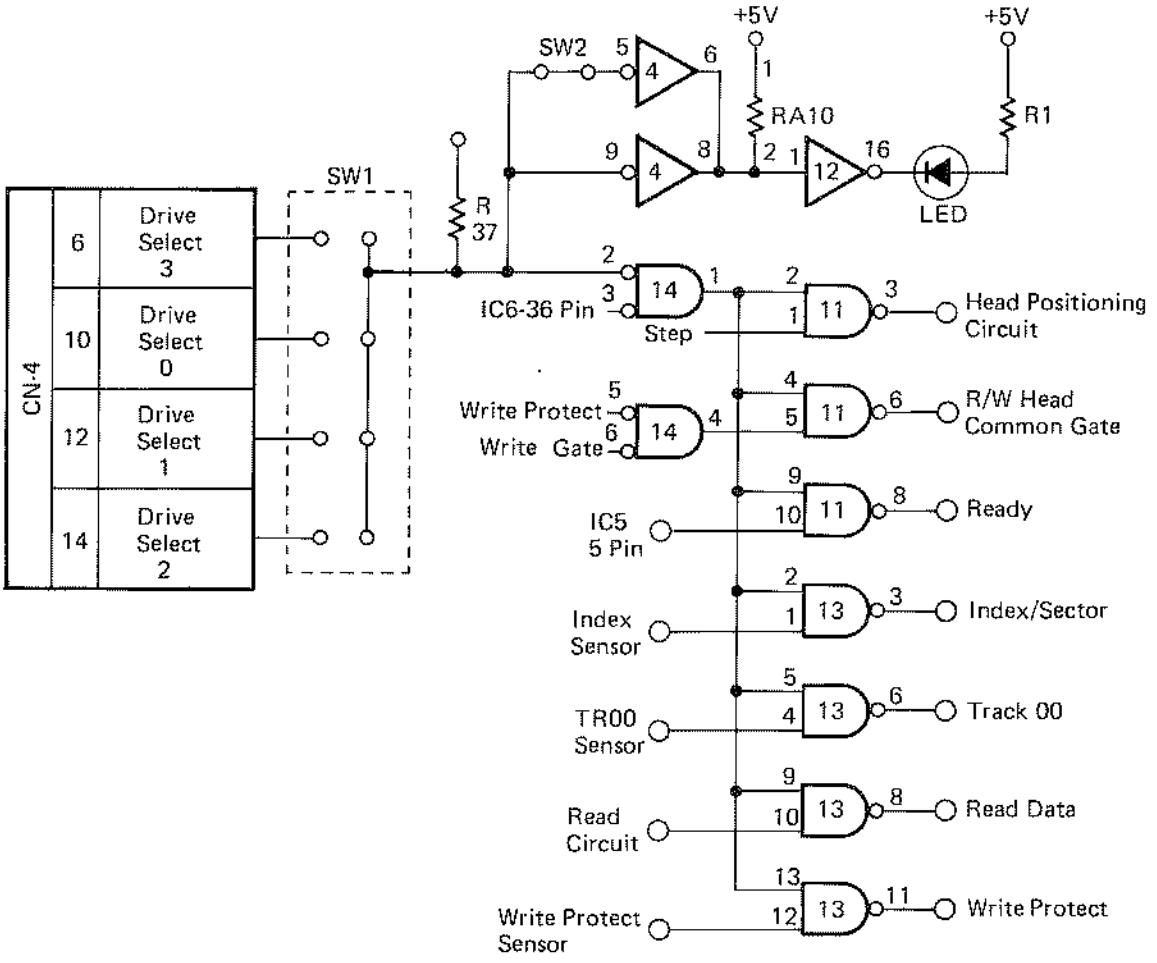


Figure C-25. Block Diagram of Drive Select Circuit

The drive select circuit and indicator LED on circuit are configured as shown above.

When one of these four signal lines, drive selects 0 to 3, is at "low" level, the drive corresponding to the low signal line responds to other input lines and the gates of the output signal lines of the drive open. Which one of the drive selects, 0 to 3, the drive corresponds to is selected by inserting a shorting pin of SW1. Up to four drives are controllable. When the drive select signal is low, the LED will turn on.

2-5-2 Side Select Circuit

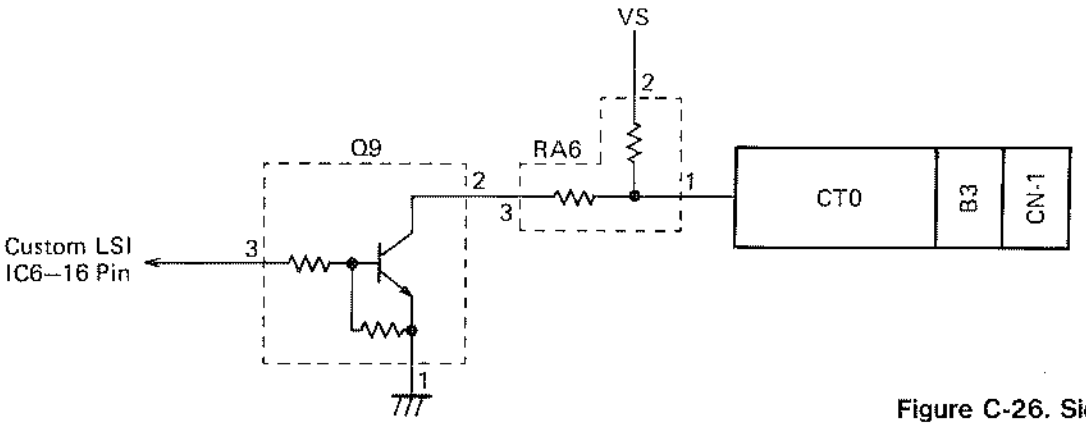


Figure C-26. Side Select Circuit

This circuit is used to select the head, but actually not used on 26-3806/3807 since the unit uses single side head and side 0 is automatically selected.

2-5-3 Head Positioning Circuit

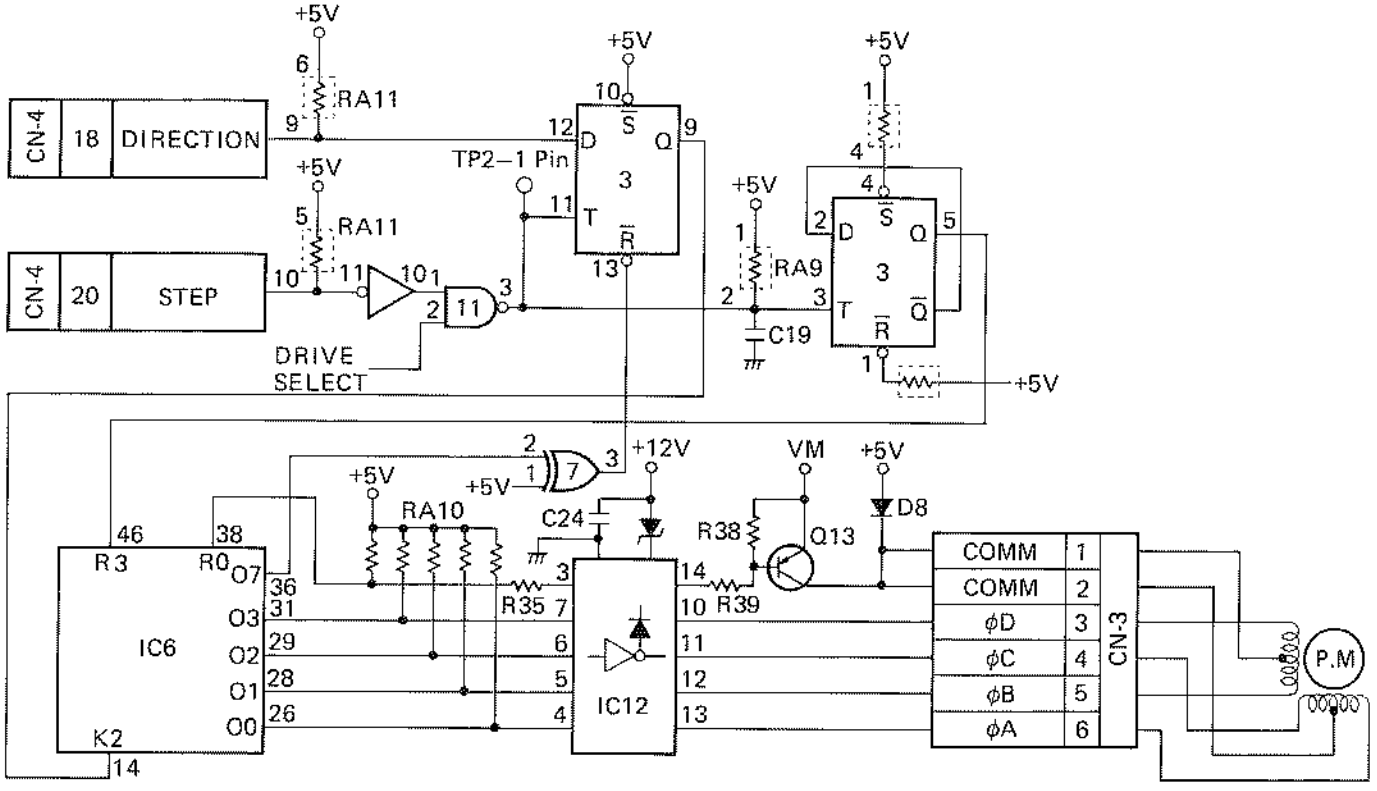


Figure C-27. Head Positioning Circuit

The head positioning circuit is configured as shown above. This circuit is used to move the head using step pulses, after the head stepping direction (inner or outer direction) is determined by the Direction signal. When the Direction signal from the host computer goes low and a step pulse signal is input, the head steps one track in the inner direction. When the Direction signal goes high, the head steps in the outer direction.

R38, R39 and Q13 in the circuit are used to drop the power when the stepping motor is on standby. To drive the stepping motor, Q13 is turned on by turning pin 38 of IC6 to "high" level and a voltage of 12V is applied to the stepping motor. To leave the motor on standby, Q13 is turned off and about 5V is applied to the stepping motor through D8 to hold the motor.

The timing chart for the Direction signal and Step signal is shown below.

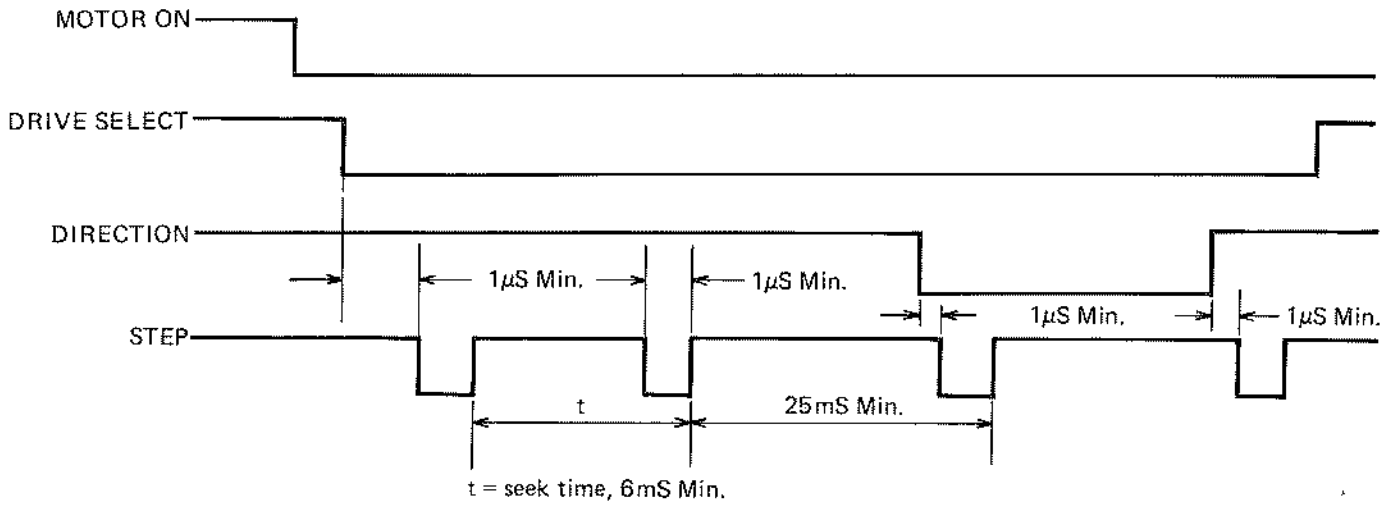


Figure C-28. Timing Chart for the Direction and Step Signal

In writing or reading data, it is necessary to wait for seek + settling time after the final step signal to stabilize the head.

2-5-4 WRITE GATE Signal

When the WRITE GATE input signal line of this circuit is low, the write circuit is made operable. However, writing will not occur, when the WRITE PROTECT output signal line is low (in a write disable state) or the corresponding FDD is not selected by the DRIVE SELECT signal line. When this input signal line is high, the FDD is in the read mode.

2-5-5 WRITE DATA Signal

This input signal line is used to transfer data to be written on the disk. When the FM- or MFM-modulated signal turns from "high" to "low" level, reverse current flows through the head to generate magnetic flux changes in it to write data on the disk. This input signal line is valid only when the WRITE GATE and DRIVE SELECT input signal lines are low and the WRITE PROTECT output signal line is high.

2-5-6 Write Circuit and Erase Circuit

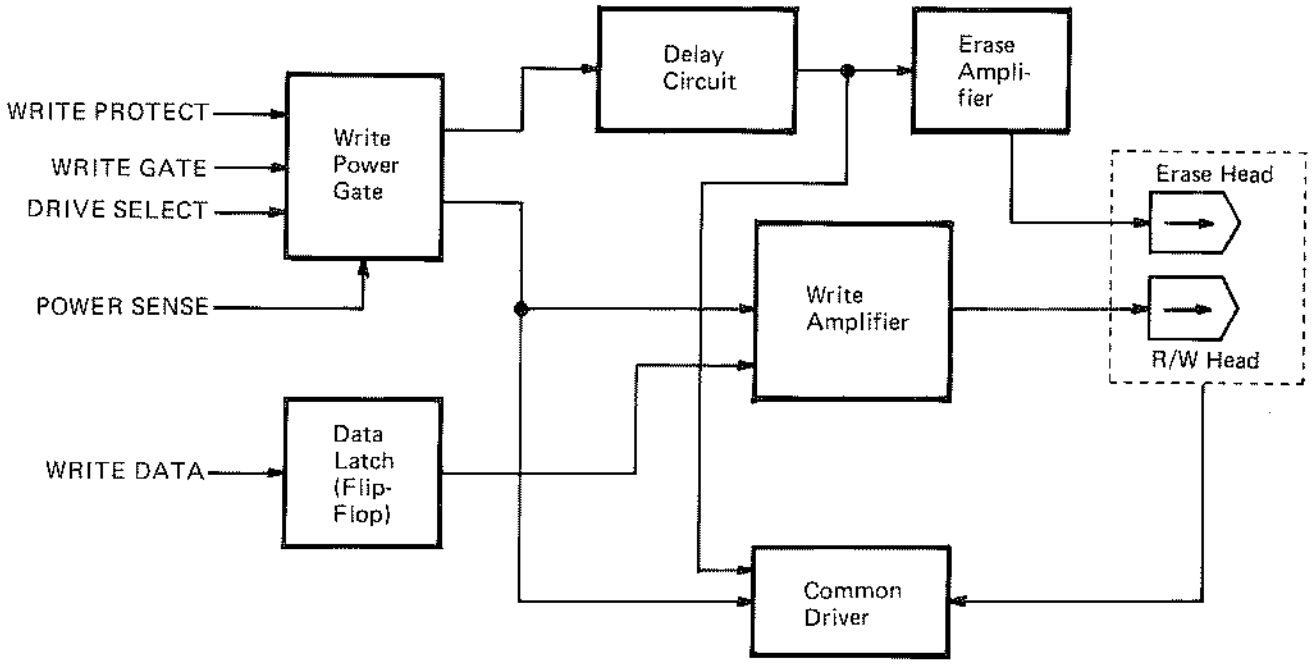


Figure C-29. Write Circuit and Erase Circuit

The block diagram for the write circuit and erase circuit is shown above.

1. Write Circuit

The write data modulated in the FM or MFM system is divided by the data latch (flip-flop) to become a WRITE DATA pulse. The write amplifier output signal becomes a rectangular signal that is inverted by this WRITE DATA pulse.
In other words, the write amplifier inverts the polarity of the head current through this signal to cause the magnetic flux synchronized with the WRITE DATA pulse to be generated in the gap of the read/write head and the media is saturation-magnetized and recorded.
The write power gate opens only when the WRITE PROTECT output signal line is high and the WRITE GATE and DRIVE SELECT input signal lines are low, enabling writing and erasing.
The timing chart for the write circuit is shown below.

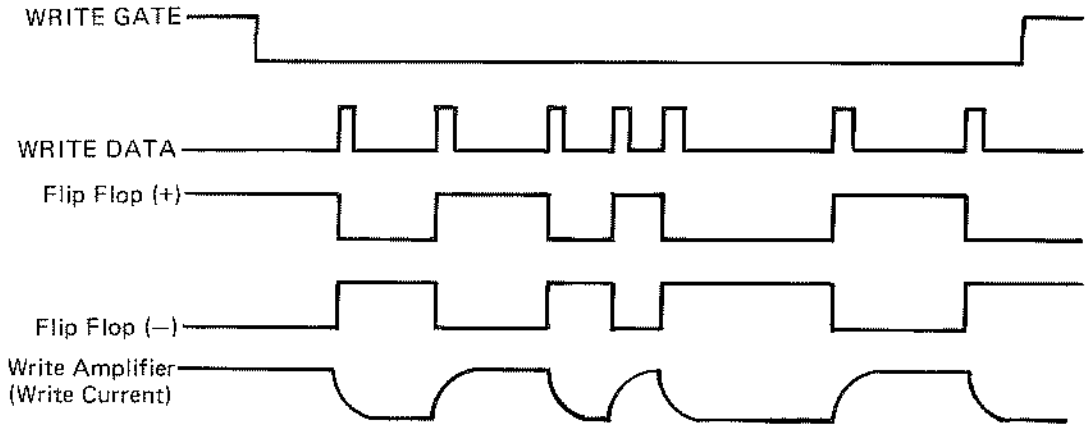


Figure C-30. Timing Chart for Write Circuit

2. **Erase Circuit**

The timing chart for the erase circuit is shown below.

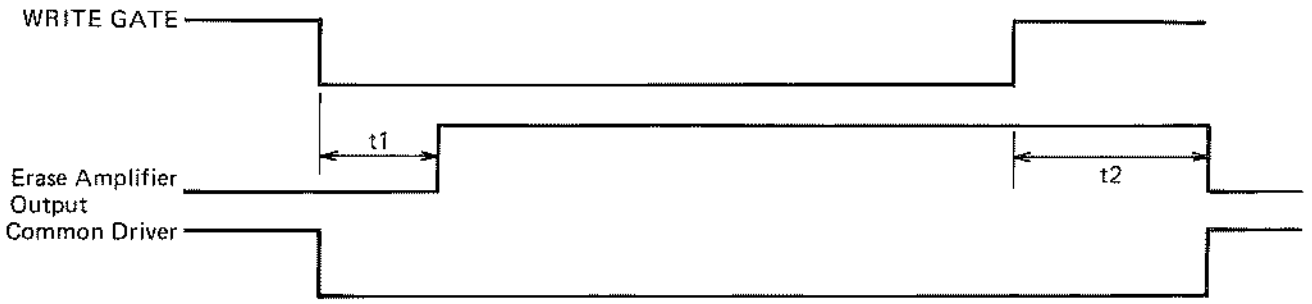


Figure C-31. Timing Chart for Erase Circuit

The tunnel erase system is adopted for this FDD. It consists of a broad-width read/write head followed by a tunnel erase head designed to allow the inner dimension to have the recording information track width. The information once recorded through the read/write head is trimmed at both edges by the tunnel erase head to be shaped to the desired track width. By doing this, even if track divergence occurs, it will not interfere with the adjacent track because the signals for the information track width are efficiently secured by the broad-width read/write head, thus securing the S/N ratio and improving the track density.

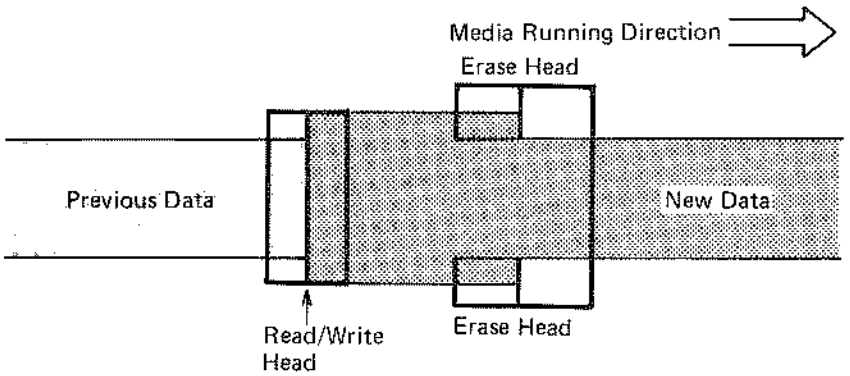


Figure C-32. Data Recording Procedure

For this reason, the erase amplifier output signal rises t1 milliseconds (minimum time required for the location written on the disk by the read/write head to reach the erase head) after the WRITE gate signal turns from "high" to "low" level, causing current to flow through the erase head to perform DC erasing. Then, the erase amplifier output signal falls t2 seconds (maximum value of time difference of above t1) after the completion of writing on the media (when the WRITE GATE signal rises), thereby completing the DC erasing. t1 and t2 seconds are previously-determined by the delay circuit.

2-5-7 MOTOR ON Signal

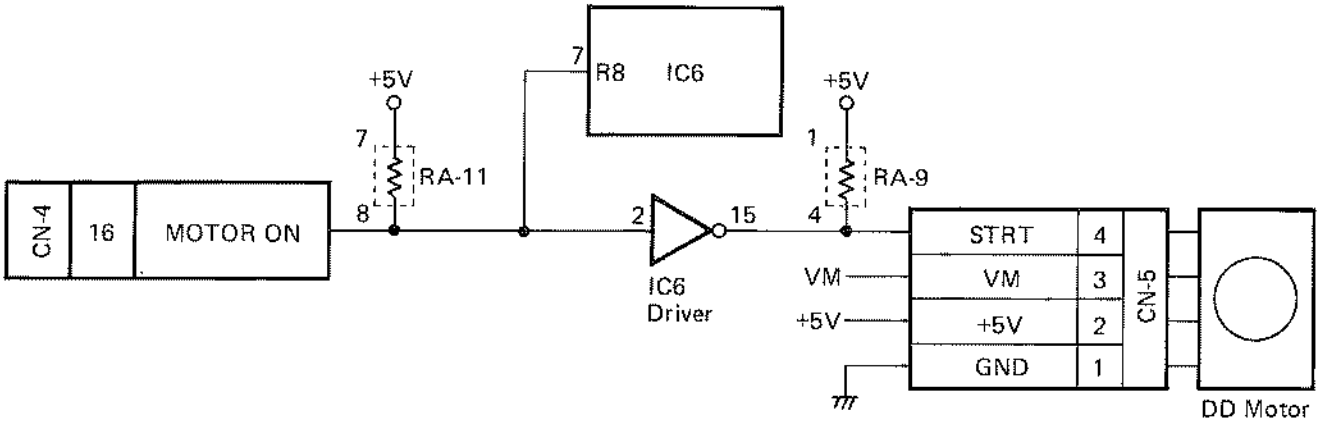


Figure C-33. Motor ON Circuit

A spindle motor drive signal appears on this input signal line.
When the input signal is low, the spindle motor turns. Conversely, when the signal is high, the motor stops.
This signal line responds regardless of the DRIVE SELECT signal. The start-up time for the spindle motor requires 0.5 seconds.

2-6 Output Signal Lines (FDD to CPU)

2-6-1 Index Circuit

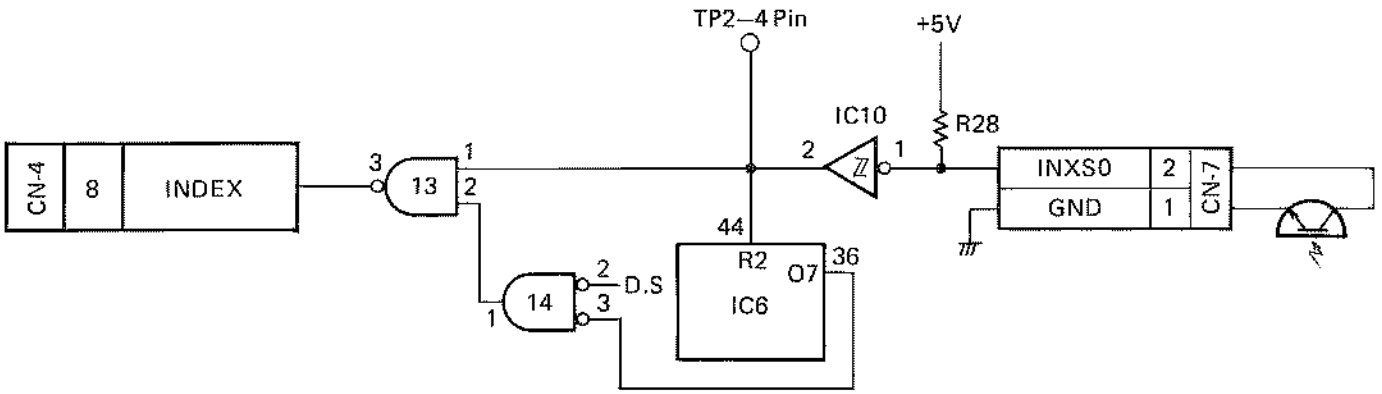


Figure C-34. Index Circuit

The index circuit is configured as shown above.
When the index sensor detects the index hole in the disk, this output signal line goes low indicating the beginning of a track.
The waveform of TP2-4 pin, while the media is turning, is shown below.

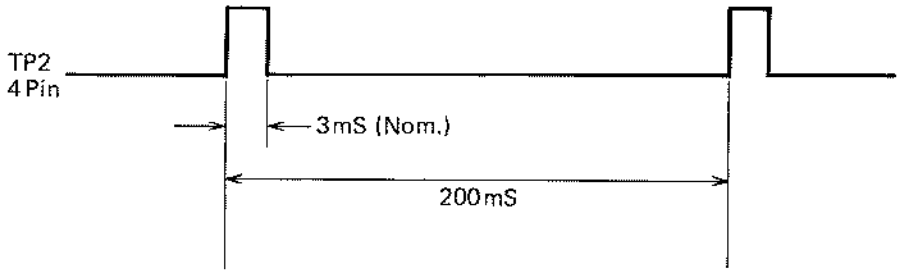


Figure C-35. Waveform of TP2-4Pin

2-6-2 Track 00 Detection Circuit

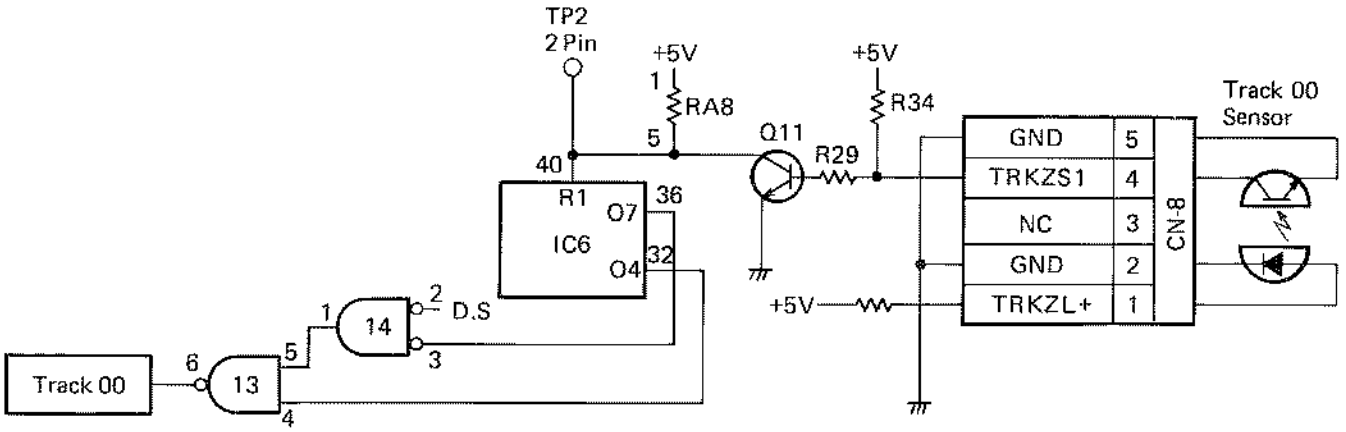


Figure C-36. Track 00 Detection Circuit

The track 00 detection circuit is configured as shown in Figure C-36.
This circuit detects track 00, the outermost track of the disk, through the track 00 sensor, and sends a Track 00 signal to the host computer.
With the stepping motor turning to move the head toward Track 00 (outer side of the disk), the light of the track 00 sensor LED is cut off when the head comes near Track 00, causing the photo-transistor to turn off and pin 40 of IC6 to go low. When the stepping motor reaches phase AD within the range of Track 00, IC6 outputs a "low" level on pin 32 and the external output pin goes low.
07 of IC6 is a Soft Reset pin, and is independent of this circuit. The soft Reset line goes low upon initially resetting the IC6 after power is turned on.

The waveform on test pin TP2-2 pin is shown below.

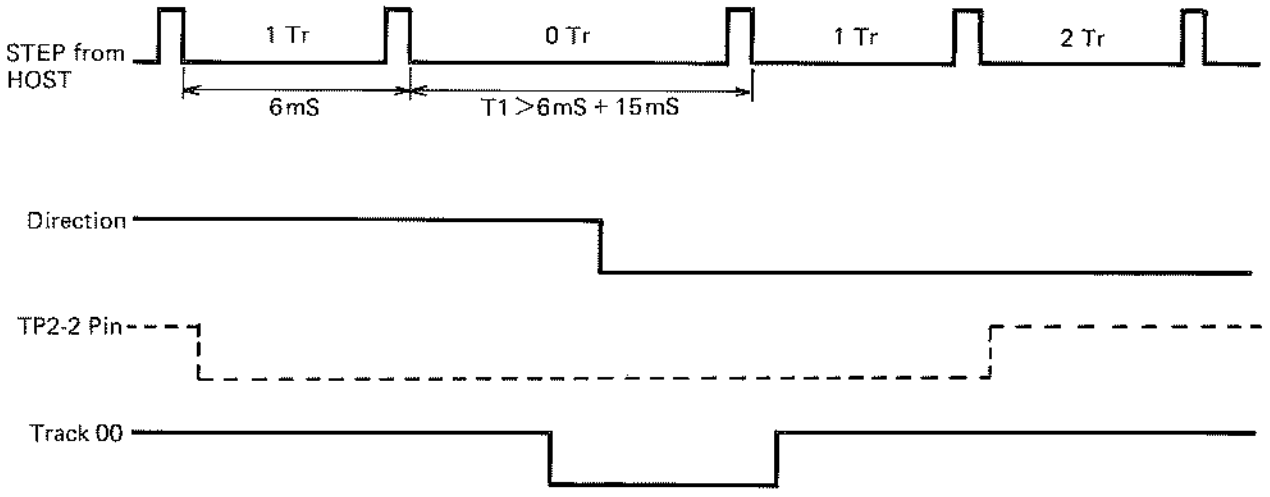


Figure C-37. Waveform on TP2-2 Pin

2-6-3 Write Protect Circuit

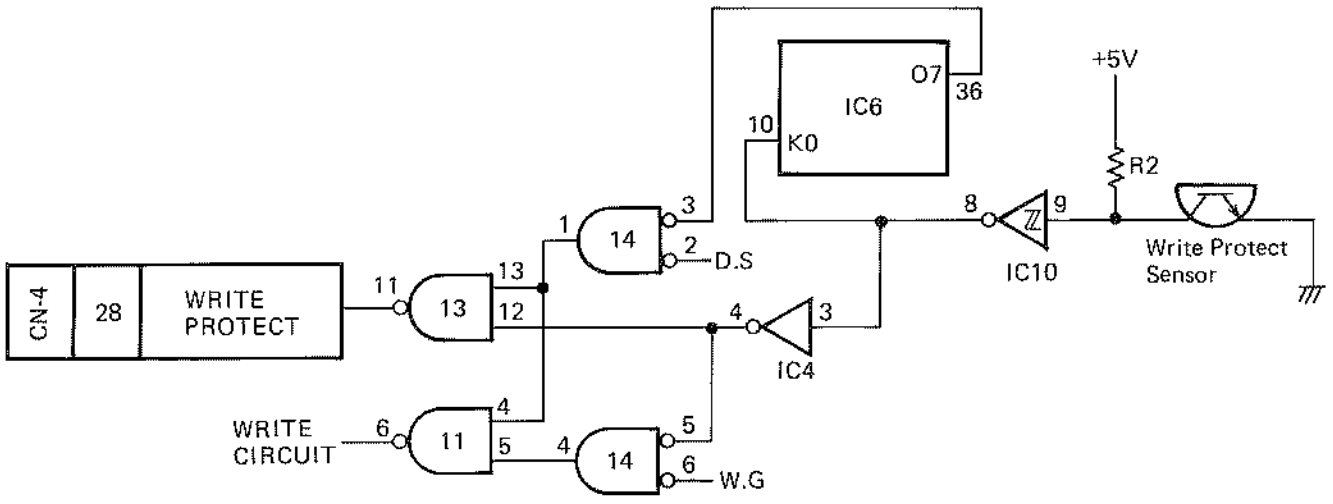


Figure C-38. Write Protect Circuit

This circuit is provided to prevent erroneous erasing of protected data recorded on the disk. The "low" level signal is output when the write enable notch of the disk, inserted into the FDD, is covered with a label, thus disabling writing to the disk. Conversely, when the "high" signal is output, the write enable state is assumed.

2-6-4 Read Amplifier Circuit

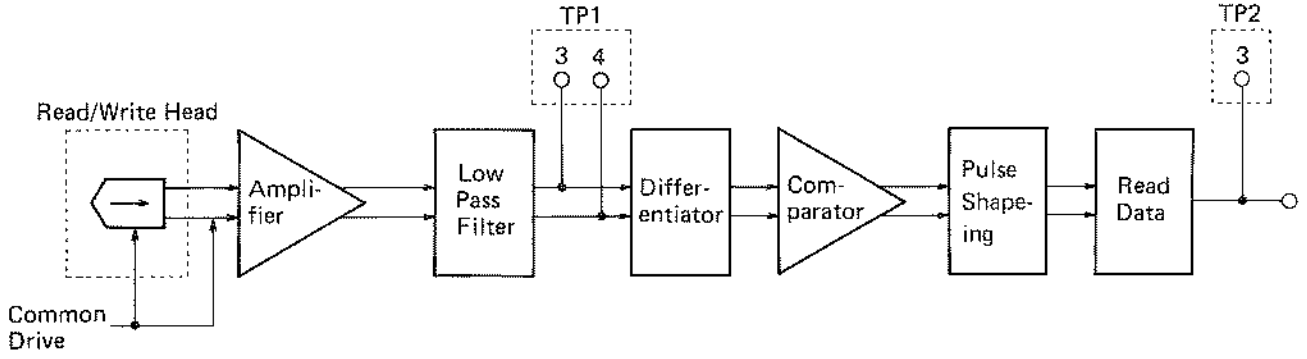


Figure C-39. Read Amplifier Circuit

The block diagram for the read amplifier is shown above.
This circuit picks up data recorded on the media through the magnetic head, and outputs read data close to the recorded signals by amplifying, although it slightly deviates time-wise, identifying, and pulse-shaping the data.
The timing chart for the read amplifier circuit is shown in Figure C-39.

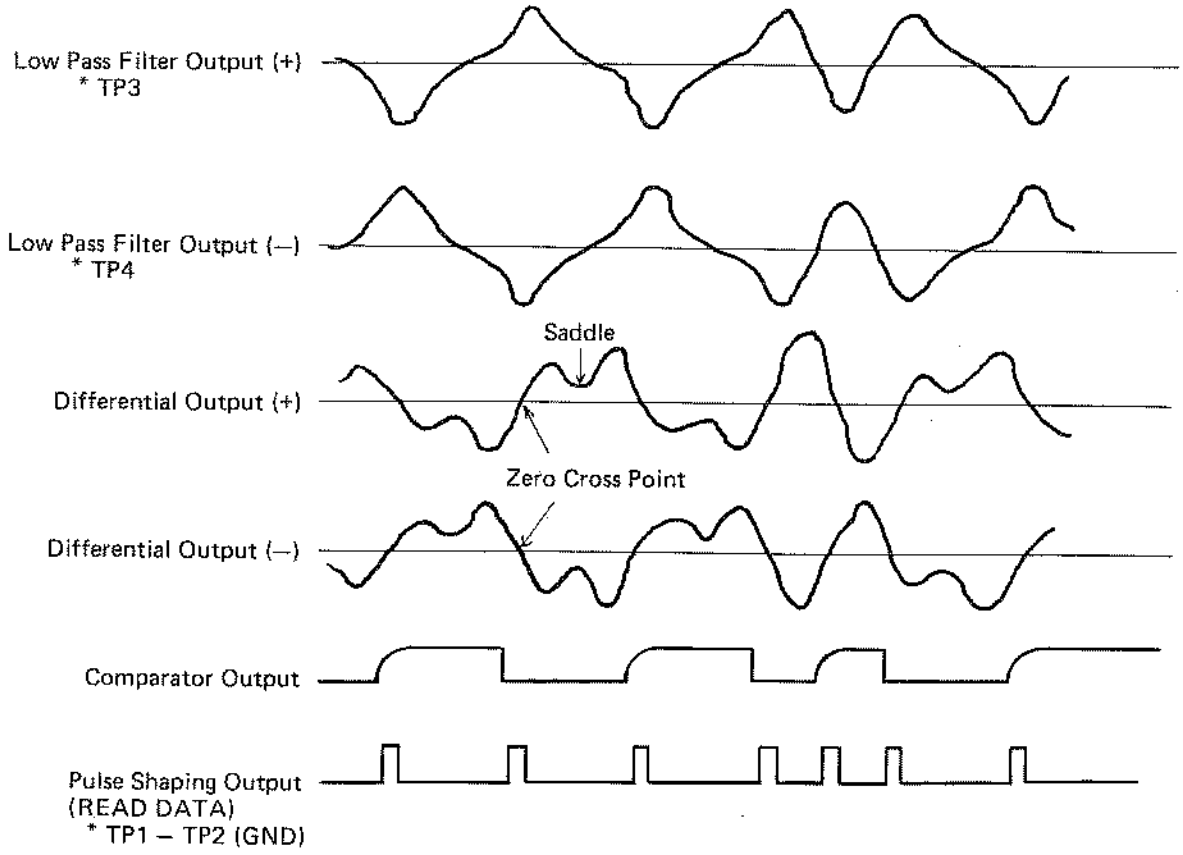
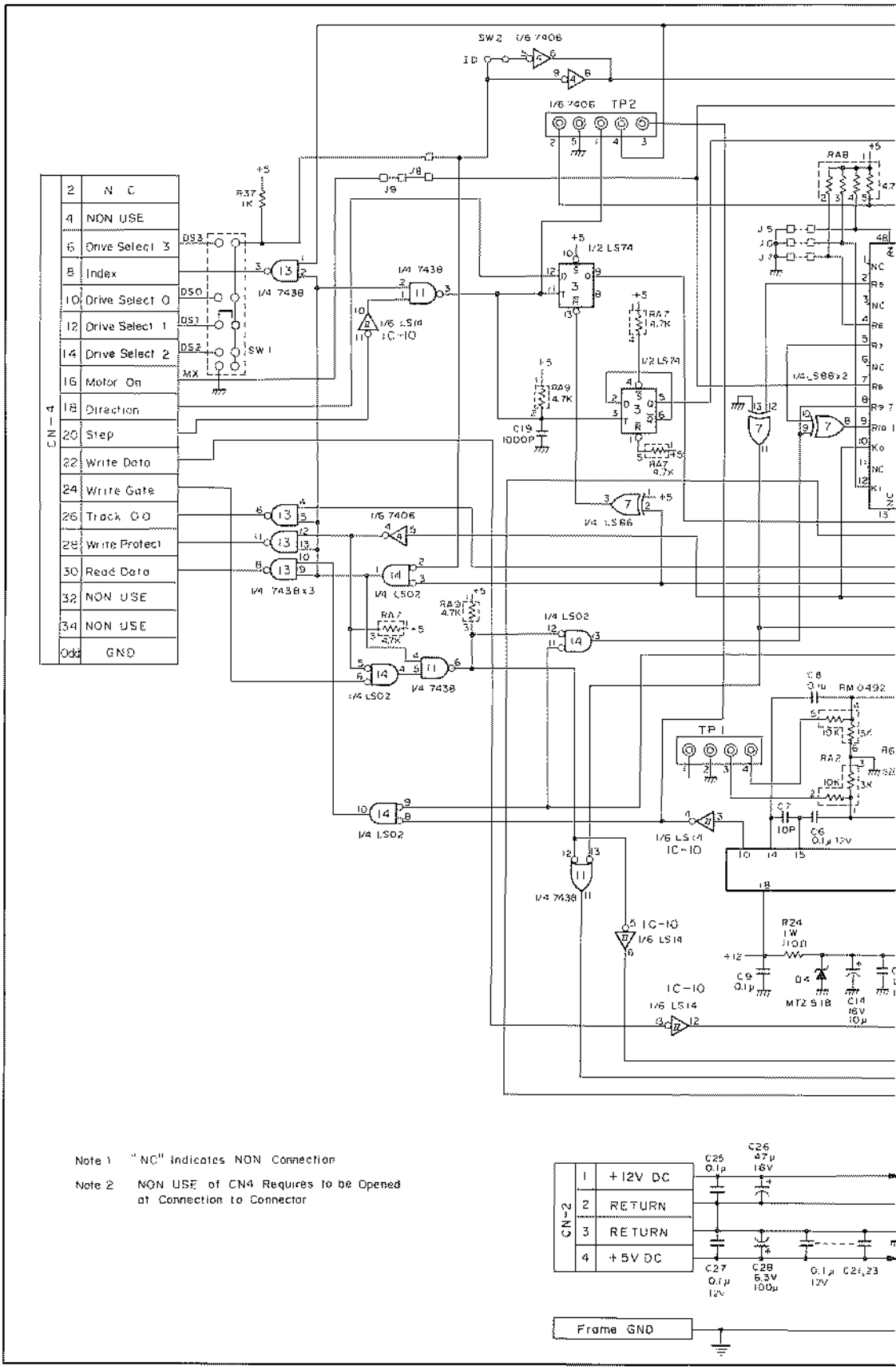


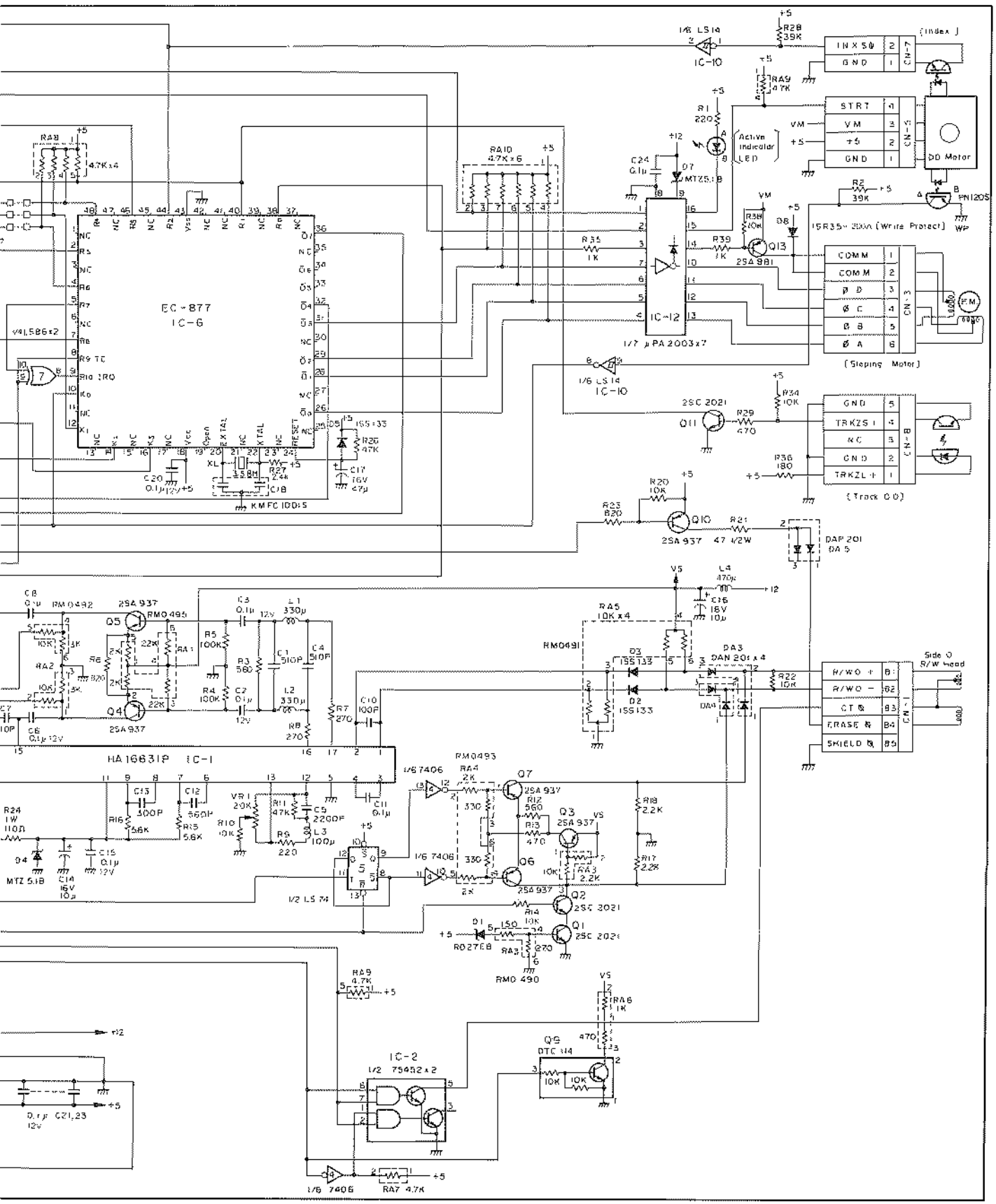
Figure C-40. Timing Chart for Read Amplifier Circuit

Part 3 Circuit Drawing



Note 1 "NC" Indicates NON Connection

Note 2 NON USE of CN4 Requires to be Opened at Connection to Connector


IC-10
1/6 LS14
INDEX
GND
STRT
VM
+5
DD Motor
Active Indicator LED
MTZ5.1B
IC-12
1/7 μPA2003x7
2SA 981
Q13
PN120S
WP
Write Protect
COMM
ØD
ØC
ØB
ØA
Stepping Motor
2SC 2021
Q11
TRKZS1
TRKZL+
Track 00
Q10
2SA 937
DAP 201
DA5
EC-877
IC-6
HA 16631P
IC-1
RM0492
RM0495
RM0491
RM0493
RM0490
Q5
Q4
Q7
Q3
Q6
Q2
Q1
DTC 114
IC-2
1/2 75452x2
1/6 7406
1/2 LS74
R027EB
DA3
DAN 201x4
D3
D2
1SS133
R/W0 +
R/W0 −
CT
ERASE
SHIELD
Side 0 R/W Head

Part 4 Troubleshooting

4-1 Processing Softerrors

4-1-1 General

The following soft errors are often mistaken for errors caused by troubles or misadjustments of the disk drive.

- Errors caused by improper operational procedure, incorrect programming or damaged disk.
- Software error caused by dust in the air, random electric interference or other external cause.

Unless a defective assembly point or damage point is clearly found in visual inspection, check to see whether the error repeats with the current diskette and also whether the same error is caused with other diskettes.

4-1-2 Detection and Correction and Read Error

Read errors are usually caused by the following conditions:

(1) Dust between the read/write head and disk; usually dirt resulting from dust is eliminated by the self-cleaning wiper in the diskette.
(2) Fine track divergence which is not detected during writing.
(3) Wear of damaged load pad or wear of disk caused by the head.
(4) Improper grounding of the power supply of the disk drive in the host computer.
(5) Improper motor speed.

To correct soft errors (1) to (5) above, follow the steps below.

(1) Re-read the error-occurred track about 10 times.
(2) If the data is not restored in step 1, allow the head to move to track 00 and make sure that the head is at track 00.
(3) Move the head to the error-occurred track.
(4) Repeat step (1).
(5) Errors which cannot be corrected by repeating the above steps are unrecoverable errors.

4-1-3 Write Error

An error which has occurred during writing is detected during a subsequent reading of the data written.

(1) To eliminate the error, write and read again.
(2) If the error still occurs after the above procedure is repeated a few times, perform reading using another track to determine whether the disk or drive is malfunctioning.
(3) If the error persists, change the disk and perform the above procedure.
If the error still persists, the drive is defective.

4-1-4 Seek Error

Possible Cause.

(1) The pulse motor or pulse motor drive circuit is defective.
(2) The carriage is defective.

There are two procedures to correct seek errors.

(1) Readjust the belt tension . . . . . Refer to page C-8.
(2) Readjust track 00 . . . . . Refer to page C-13.

4-1-5 Interchange Error

Sometimes data written by a disk drive cannot be read by another drive. This phenomenon is called "interchange error".
The points to be checked are:

(1) Head alignment is defective . . . . . Refer to Head/Radial Adjustment on page C-11.
(2) Head output is not enough . . . . . Refer to Head Output Adjustment on page C-11.
(3) The motor speed is incorrect . . . . . Refer to Motor Speed Adjustment on page C-12.
(4) Check the center hole of the disk.
If the center hole of the disk is damaged, check the clamp mechanism.

4-2 Floppy Disk Drive for Repair

4-2-1 Have the user send you the defective floppy disk drive together with the diskette which was used when the user found it defective.

Without this diskette, you may fail to locate the trouble.

4-2-2 Be sure to get information from the user about the operating conditions at the time the user found the floppy disk drive defective. This will help in troubleshooting later.

(1) If the Active lamp will not light and the unit does not operate at all, check the DC Power Supply.
(2) If the Active lamp lights but an operating sound is not heard inside the unit, proceed to Media Rotation check.
(3) If stepper motor turns without causing carriage movement, proceed to Tracking Mechanism.
(4) If the drive executes continuously but fails to read and write, proceed Write Circuit Check and Read Circuit malfunction.

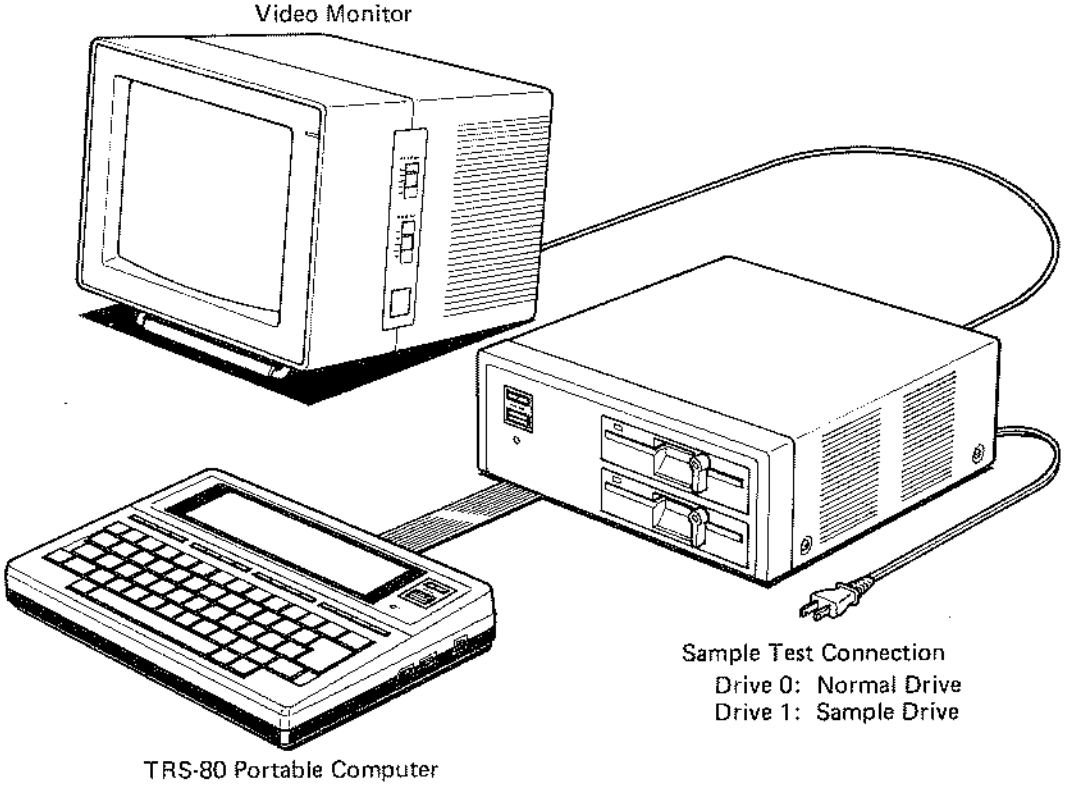
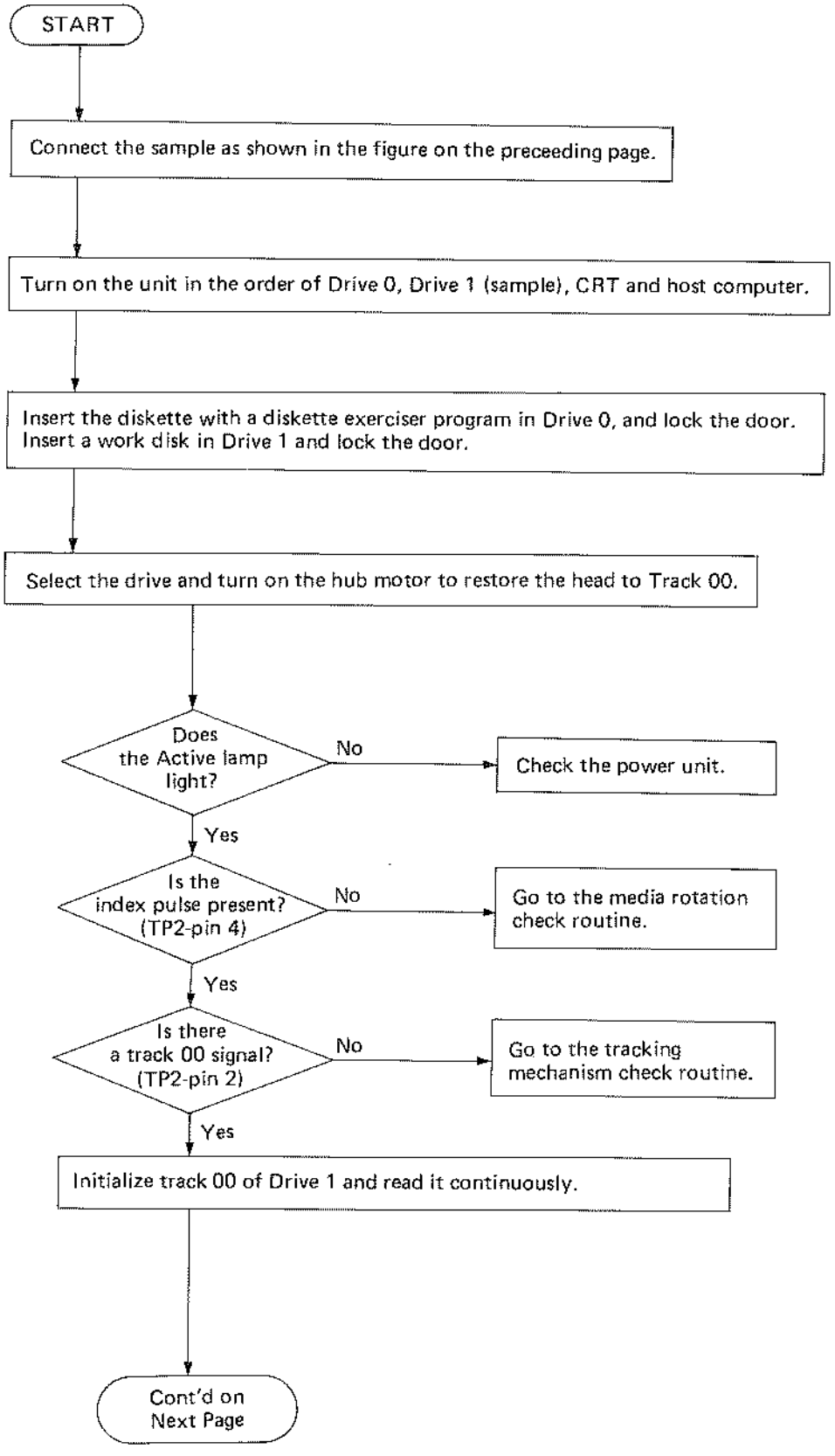
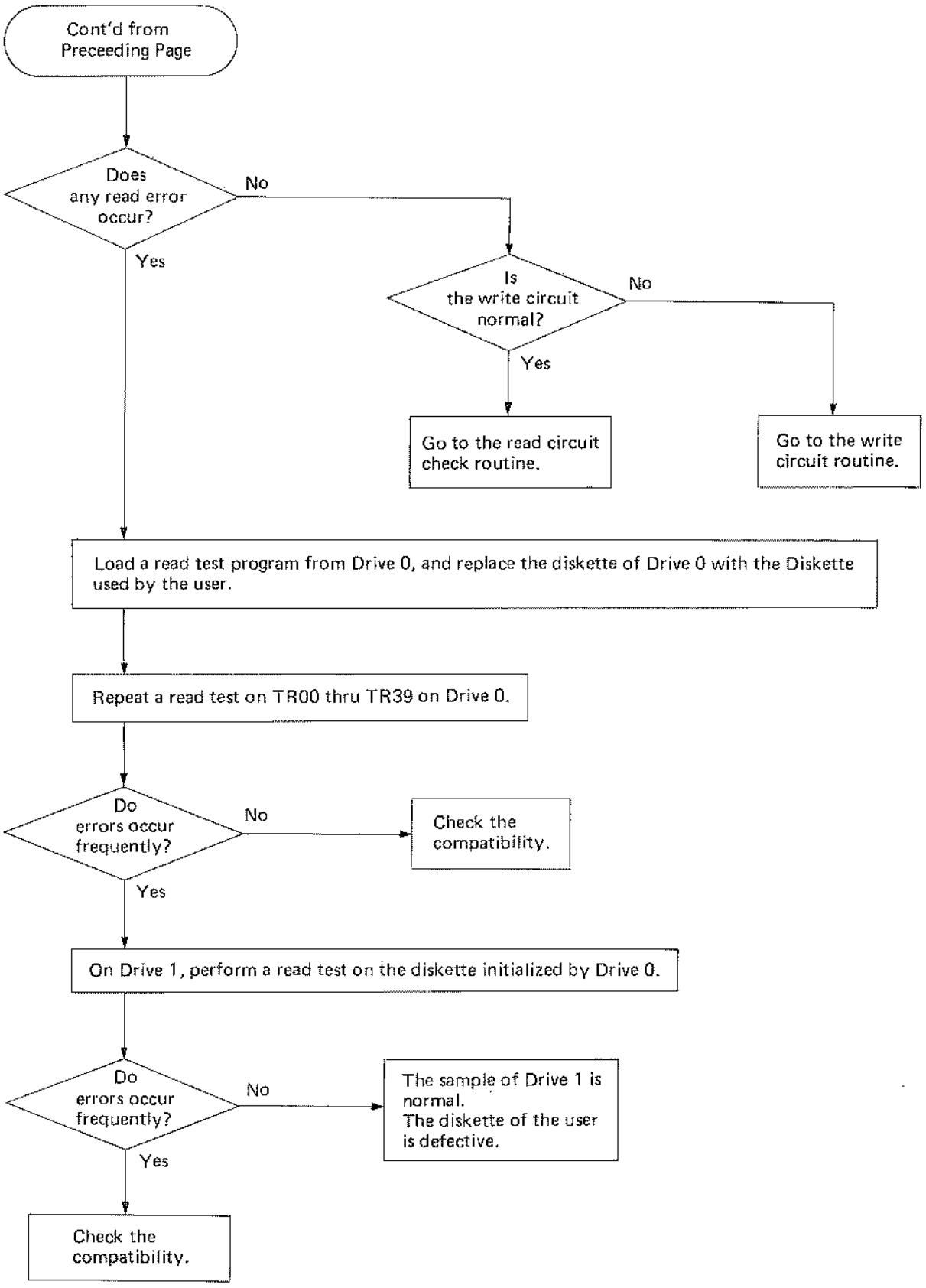


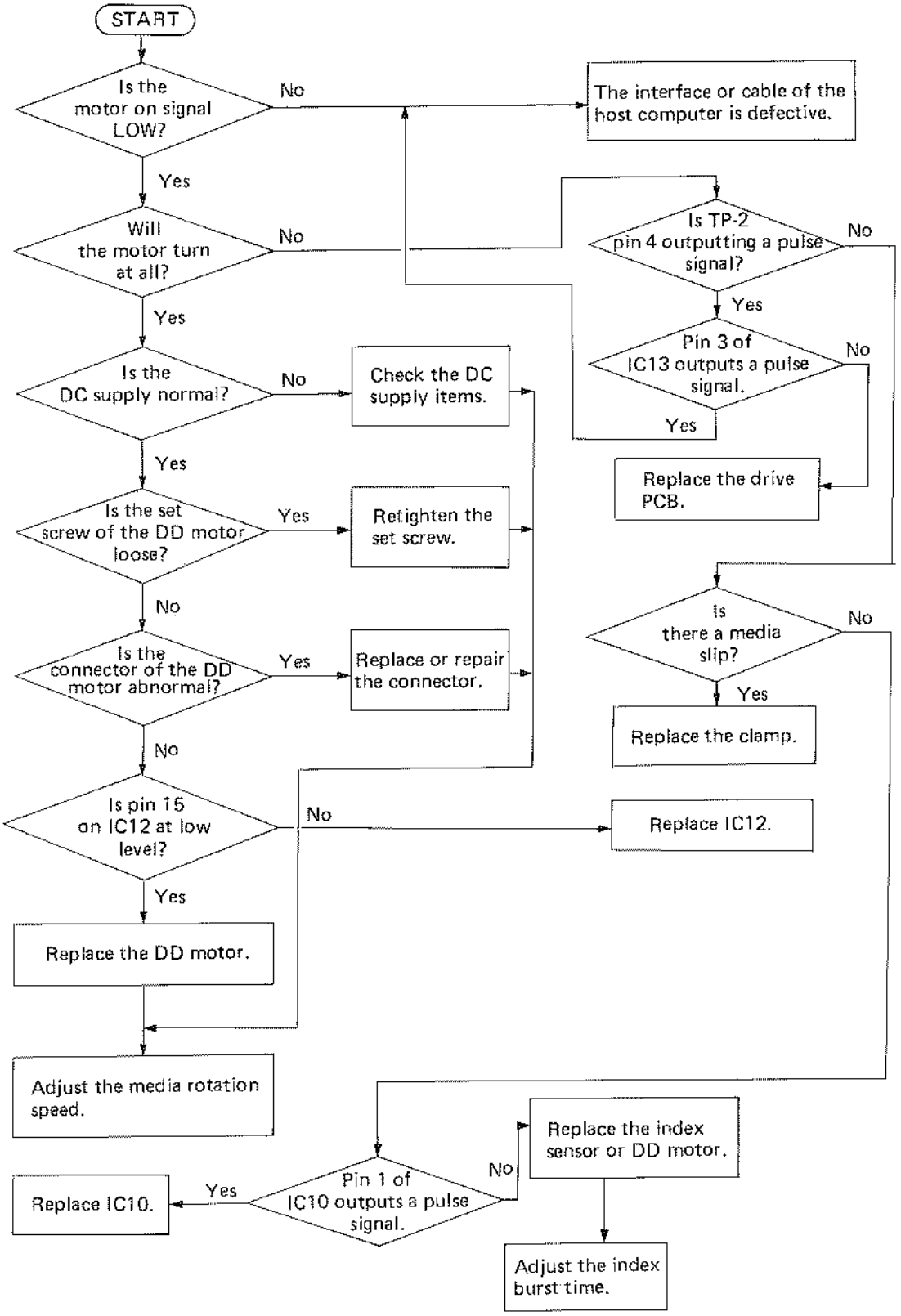
Figure C-42. Test System Hook-up

4-3 Troubleshooting Procedures

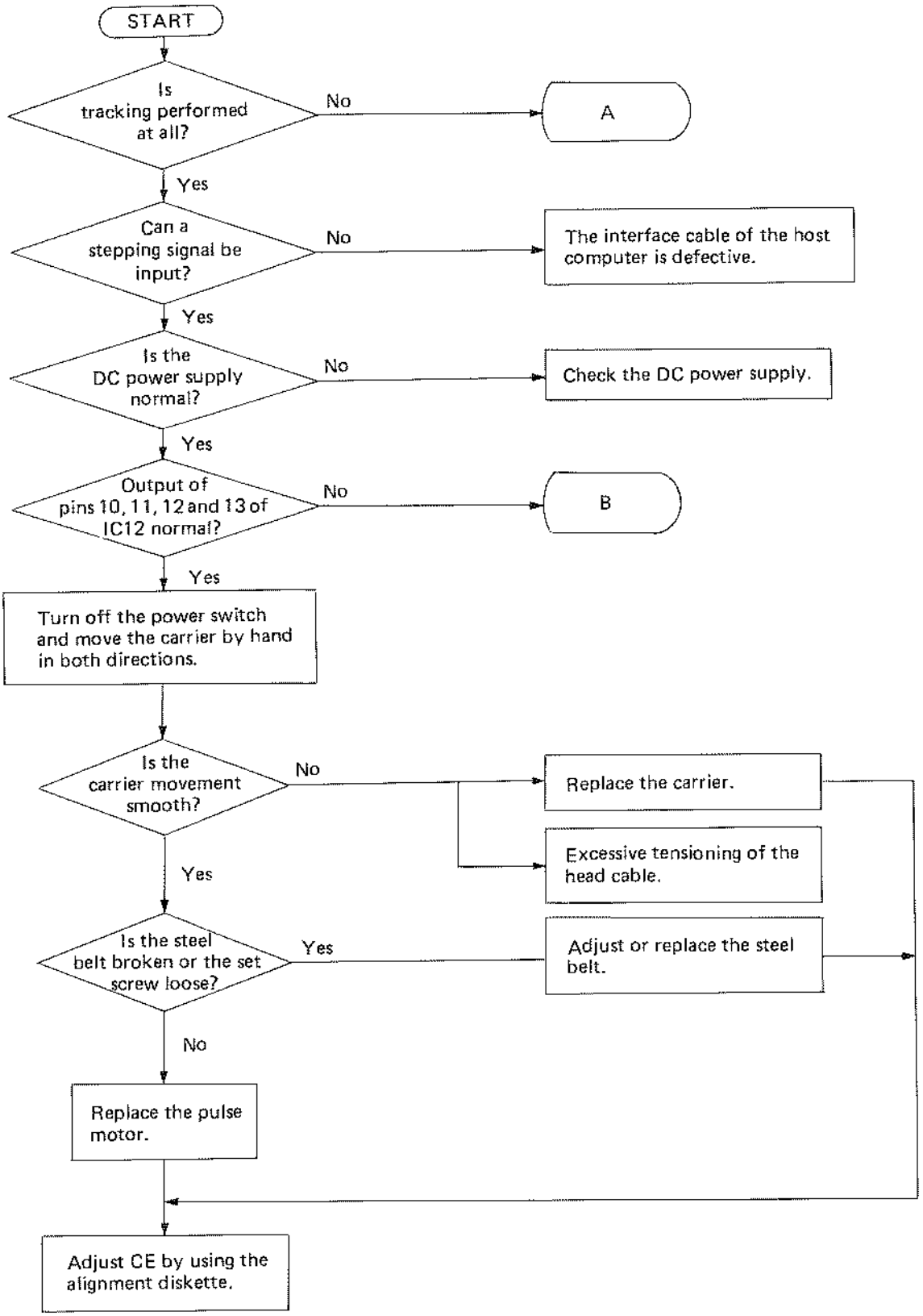


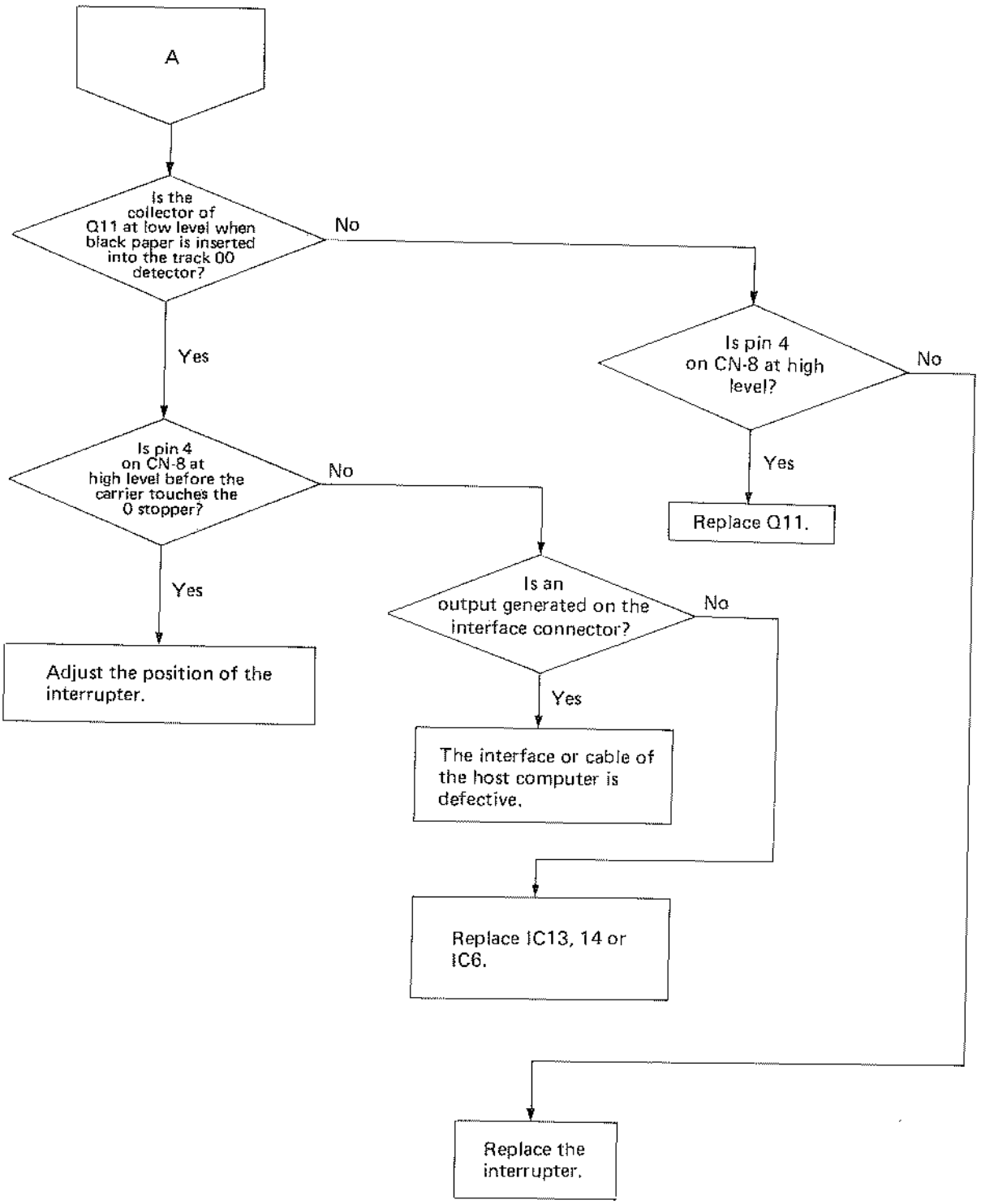

Cont'd from Preceeding Page
Does any read error occur?
No
Yes
Is the write circuit normal?
No
Yes
Go to the read circuit check routine.
Go to the write circuit routine.
Load a read test program from Drive 0, and replace the diskette of Drive 0 with the Diskette used by the user.
Repeat a read test on TR00 thru TR39 on Drive 0.
Do errors occur frequently?
No
Check the compatibility.
Yes
On Drive 1, perform a read test on the diskette initialized by Drive 0.
Do errors occur frequently?
No
The sample of Drive 1 is normal.
The diskette of the user is defective.
Yes
Check the compatibility.

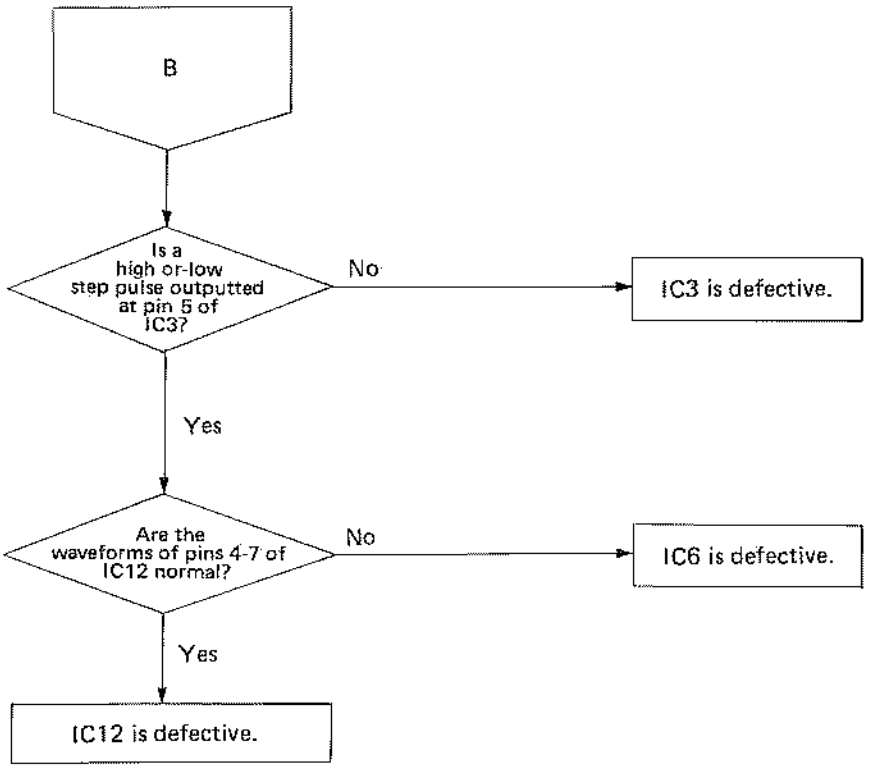
4-3-1 Media Rotation Check



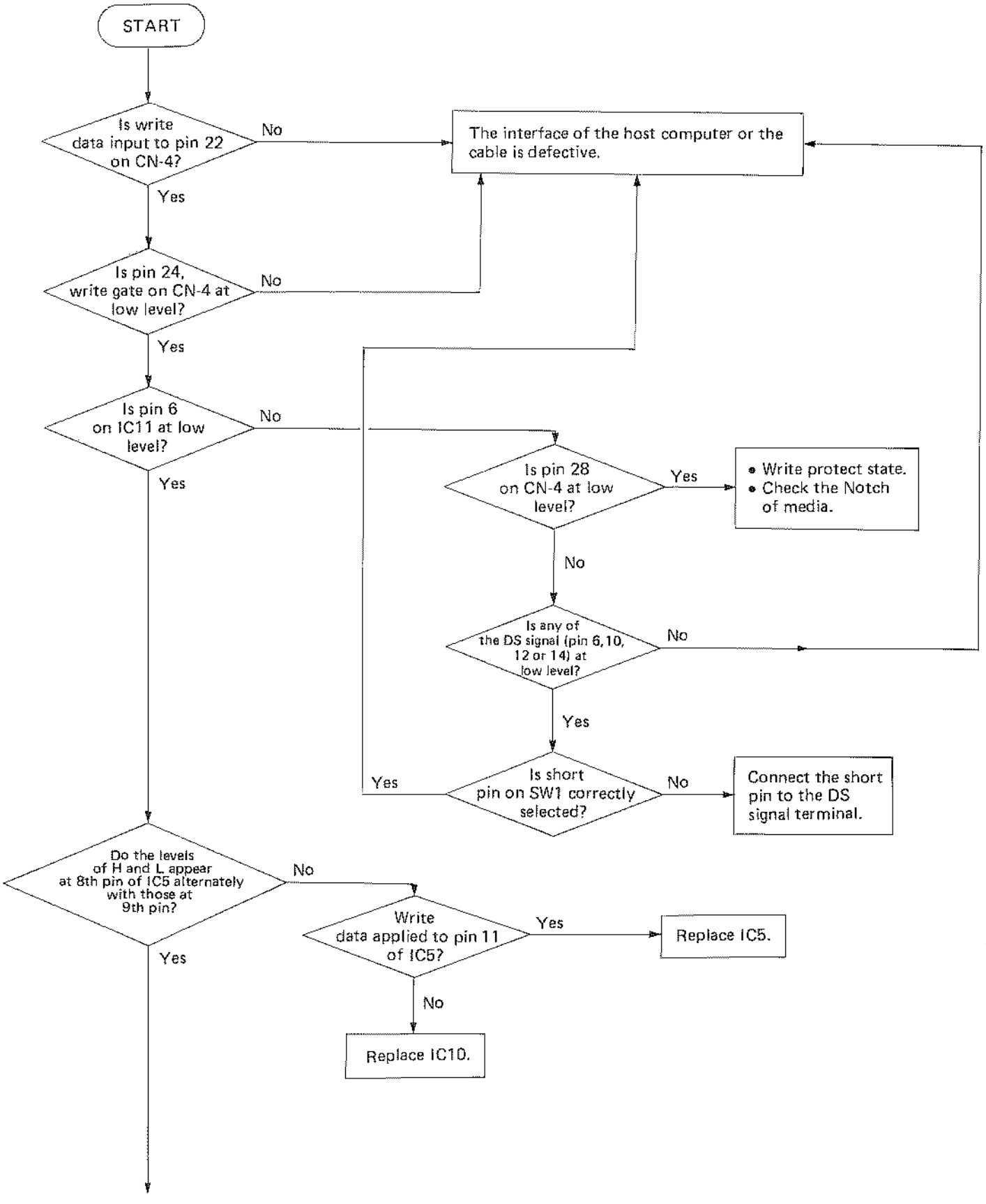
4-3-2 Tracking Mechanism (Track 00 signal won't be generated)

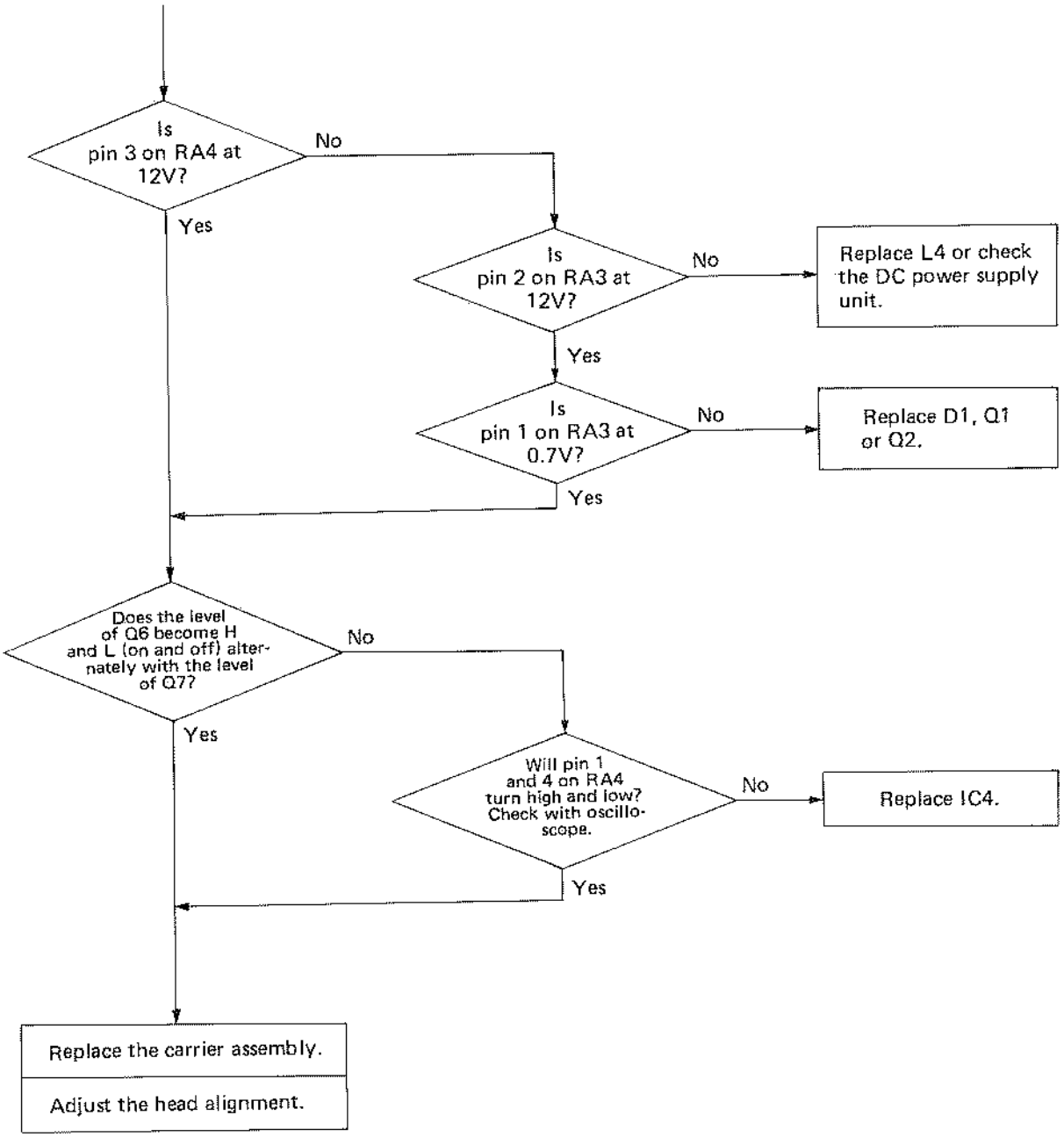



A
Is the collector of Q11 at low level when black paper is inserted into the track 00 detector?
No
Yes
Is pin 4 on CN-8 at high level?
No
Yes
Replace Q11.
Is pin 4 on CN-8 at high level before the carrier touches the 0 stopper?
No
Yes
Adjust the position of the interrupter.
Is an output generated on the interface connector?
No
Yes
The interface or cable of the host computer is defective.
Replace IC13, 14 or IC6.
Replace the interrupter.

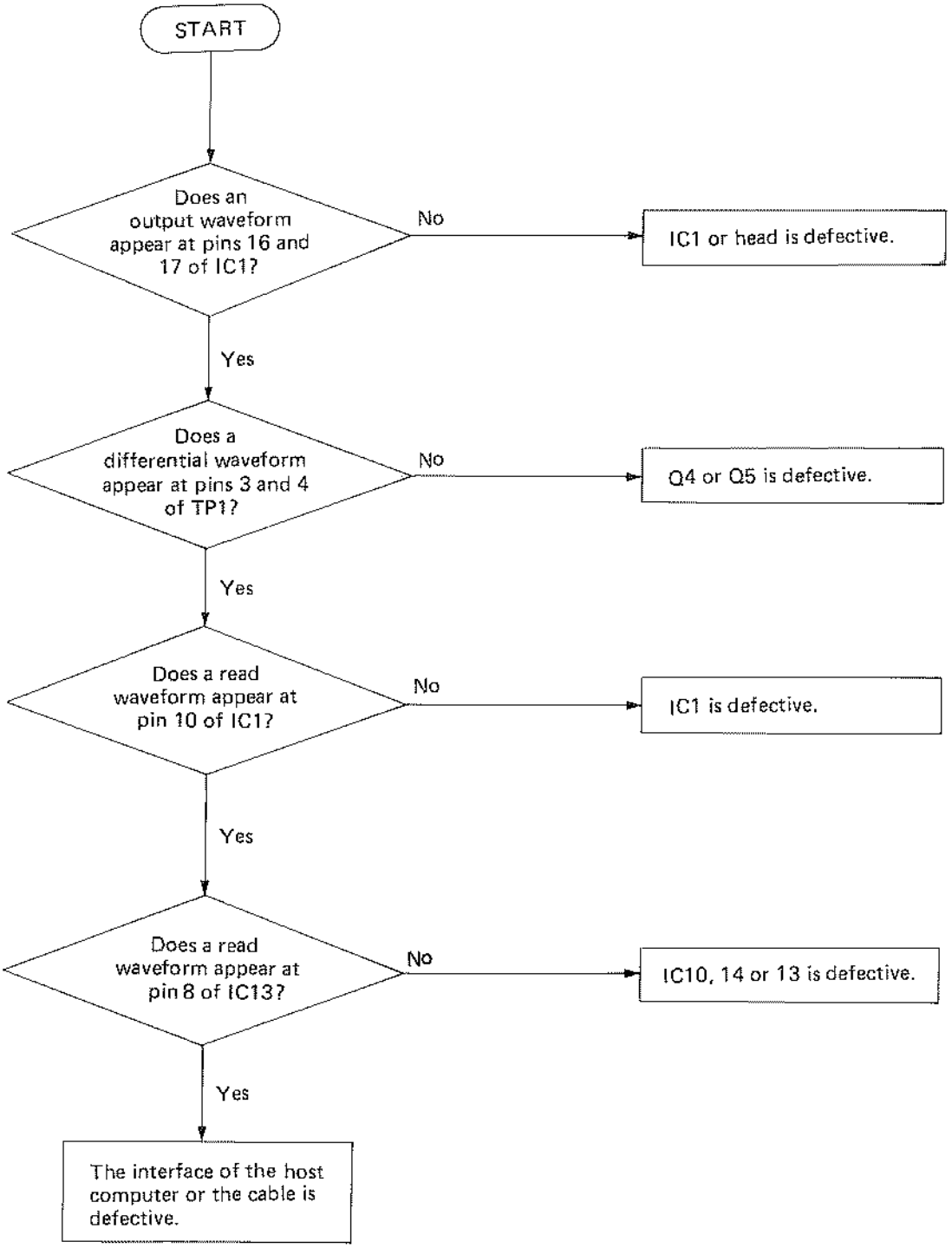

B
Is a high or low step pulse outputted at pin 5 of IC3?
No
IC3 is defective.
Yes
Are the waveforms of pins 4-7 of IC12 normal?
No
IC6 is defective.
Yes
IC12 is defective.

4-3-3 Write Circuit Check




Is pin 3 on RA4 at 12V?
No
Yes
Is pin 2 on RA3 at 12V?
No
Replace L4 or check the DC power supply unit.
Yes
Is pin 1 on RA3 at 0.7V?
No
Replace D1, Q1 or Q2.
Yes
Does the level of Q6 become H and L (on and off) alternately with the level of Q7?
No
Yes
Will pin 1 and 4 on RA4 turn high and low? Check with oscilloscope.
No
Replace IC4.
Yes
Replace the carrier assembly.
Adjust the head alignment.

4-3-4 Read Circuit Malfunction



Part 5 Parts List

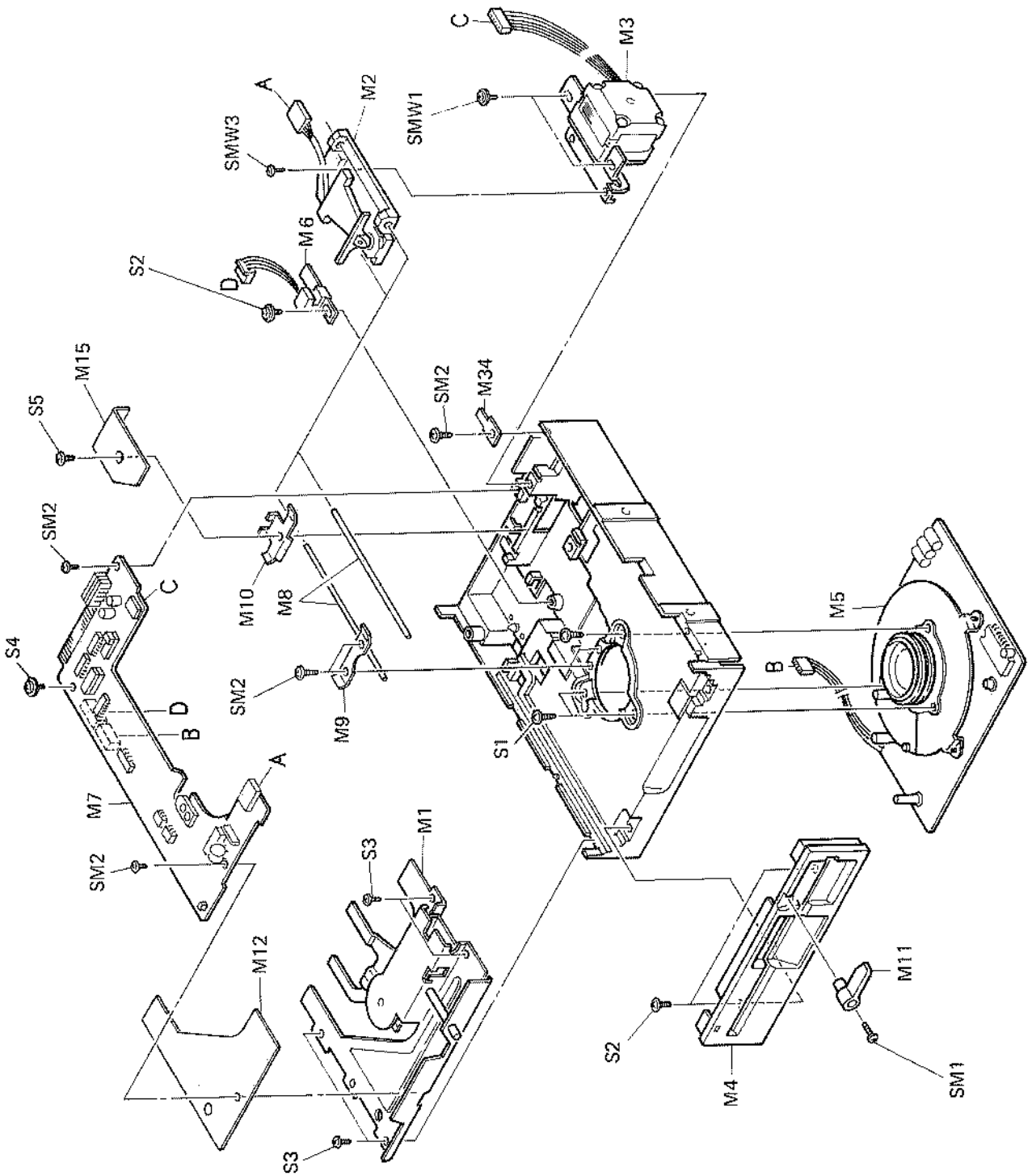


Figure C-43. Exploded View of Main Unit

MAIN UNIT

CLAMP BASE BK

CARRIER A BK

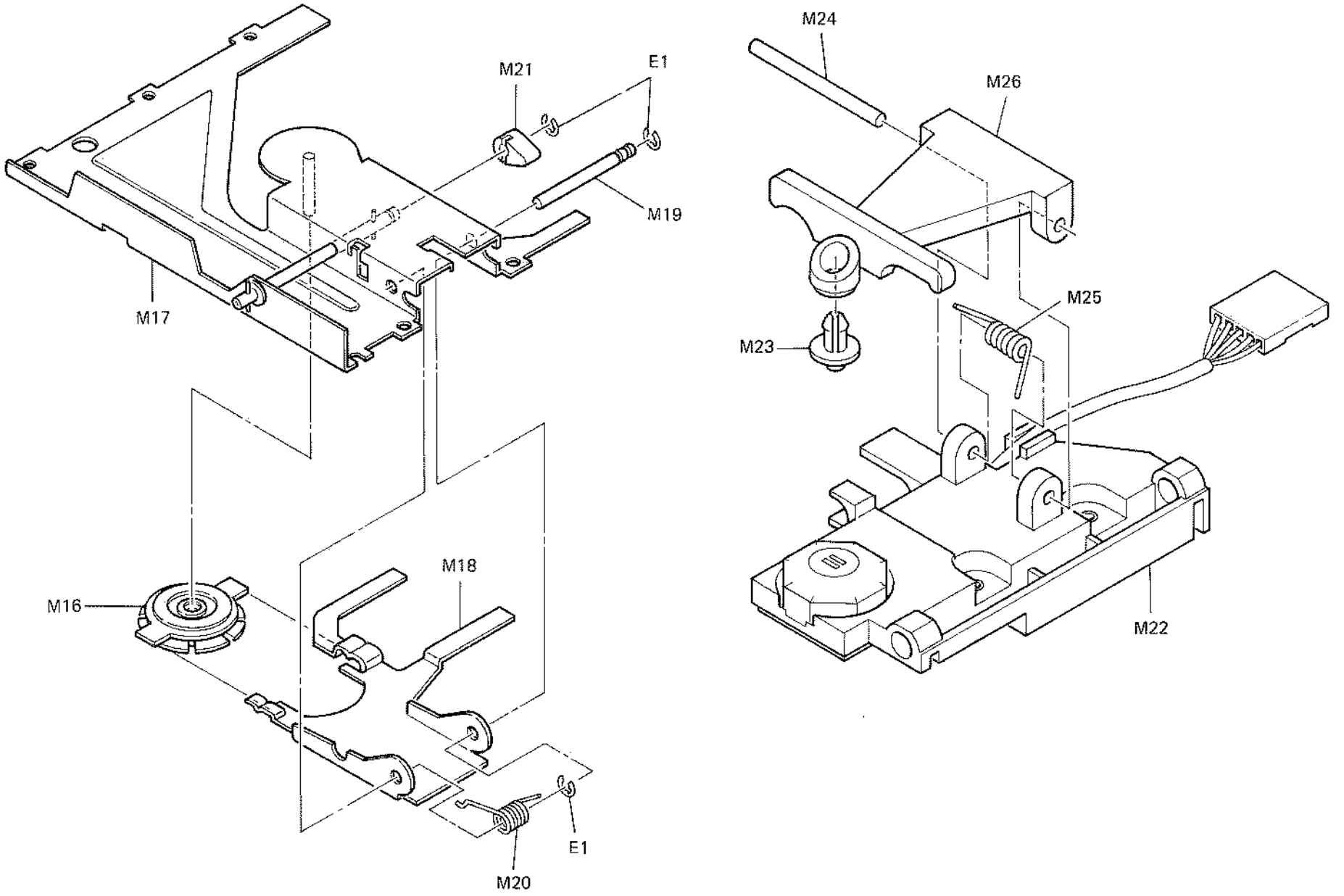


Figure C-44. Exploded View of Clamp Base BK and Carrier A BK

PULSE MOTOR BK

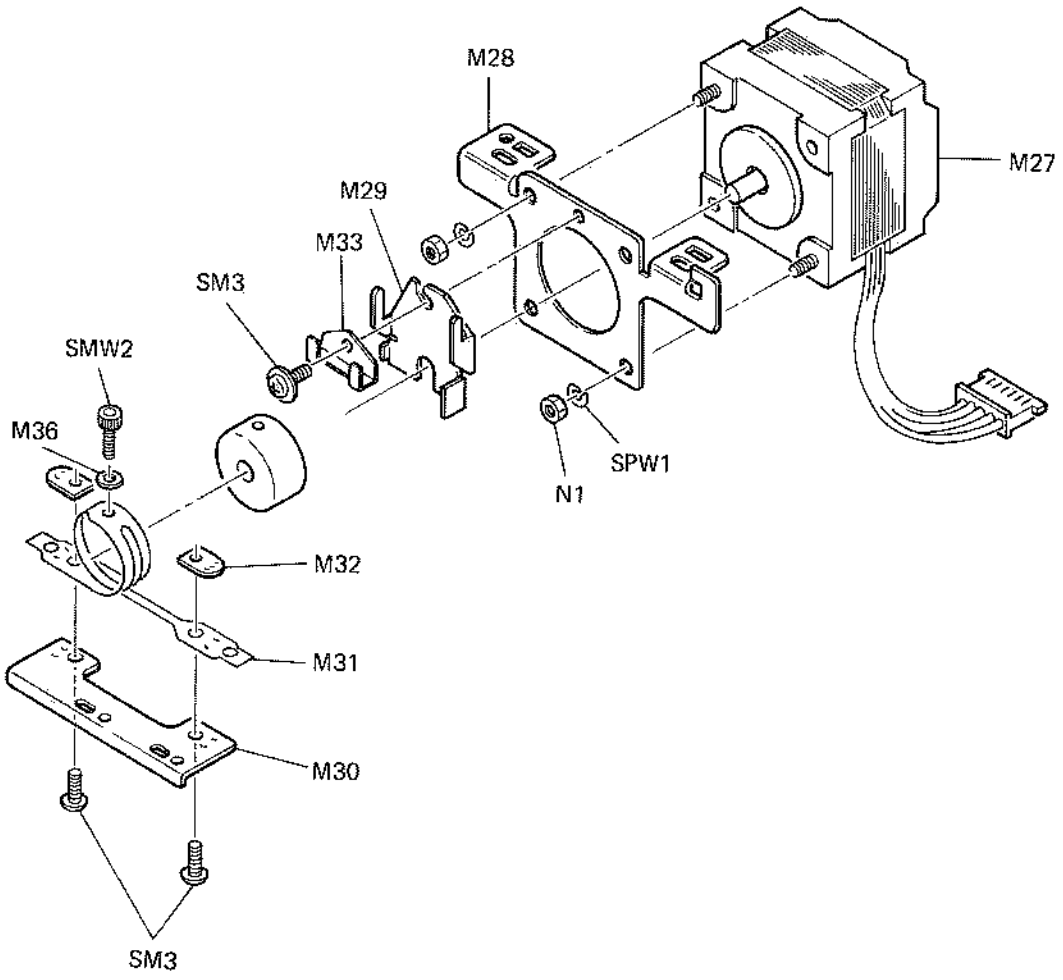


Figure C-45. Exploded View of Pulse Motor BK.

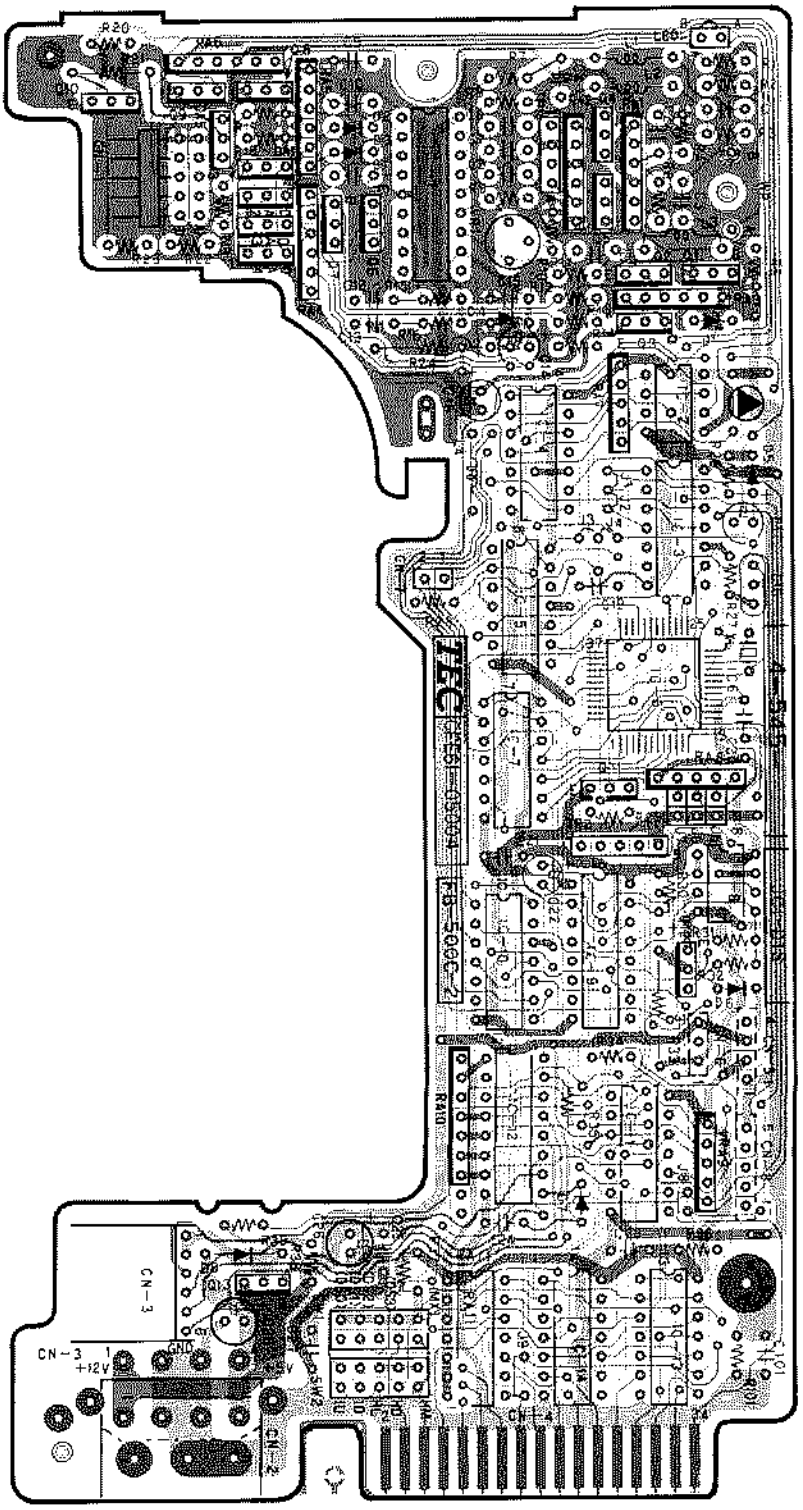


Figure C-46. P.C. Board

P.C.B. ASSEMBLY

Ref. No.	Description		RS Part No.	Mfr's Part No.
CAPACITORS				
C1	Capacitor, Ceramic	510pF/50V/±5%		EBJT0-11400
C2	Capacitor, Ceramic	0.1μF/12V/±5%		EBJT0-05200
C3	Capacitor, Ceramic	0.1μF/12V/±5%		EBJT0-05200
C4	Capacitor, Ceramic	510pF/50V/±5%		EBJT0-11400
C5	Capacitor, Ceramic	2200pF/50V/±10%		EBJT0-07200
C6	Capacitor, Ceramic	0.1μF/12V/±5%		EBJT0-05200
C7	Not used			
C8	Capacitor, Ceramic	0.1μF/12V/±5%		EBJT0-05200
C9	Capacitor, Ceramic	0.1μF/50V/+80 −20%		EBIT0-00900
C10	Capacitor, Ceramic	100pF/50V/±5%		EBJT0-07500
C11	Capacitor, Ceramic	0.1μF/50V/+80 −20%		EBIT0-00900
C12	Capacitor, Ceramic	560pF/50V/±5%		EBJT0-11500
C13	Capacitor, Ceramic	300pF/50V/±5%		EBJT0-13900
C14	Capacitor, Electrolytic	10μF/16V/+75 −10%		EBB00-53800
C15	Capacitor, Ceramic	0.1μF/12V/±5%		EBJT0-05200
C16	Capacitor, Electrolytic	10μF/16V/+75 −10%		EBB00-53800
C17	Capacitor, Electrolytic	47μF/16V/+75 −10%		EBB00-34800
C18, XL	Cerarock & Capacitor	KMFC1001S		EKH00-04600
C19	Capacitor, Ceramic	1000pF/50V/±10%		EBJT0-07100
C20	Capacitor, Ceramic	0.1μF/12V/±5%		EBJT0-05200
C21	Capacitor, Ceramic	0.1μF/12V/±5%		EBJT0-05200
C22	Not used			
C23	Capacitor, Ceramic	0.1μF/12V/±5%		EBJT0-05200
C24	Capacitor, Ceramic	0.1μF/50V/+80 −20%		EBIT0-00900
C25	Capacitor, Ceramic	0.1μF/50V/+80 −20%		EBIT0-00900
C26	Capacitor, Electrolytic	47μF/16V/+75 −10%		EBB00-34800
C27	Capacitor, Ceramic	0.1μF/12V/±5%		EBJT0-05200
C28	Capacitor, Electrolytic	100μF/6.3V/+75 −10%		EBB00-34900
C101	Not Used			
CONNECTORS				
CN1B	Jack, Junction to R/W Head			EEB00-54500
CN2	Jack, Junction to Power Supply			EEB00-61100
CN3	Jack, Junction to Pulse Motor			EEB00-52000
CN4	Jack, Junction to Interface			
CN5	Jack, Junction to Drive Motor			EEB00-50500
CN6	Not used			
CN7	Sensor, Index			CFA45-60301
CN8	Jack, Junction to Drive Motor			EEB00-51900

Ref. No.	Description		RS Part No.	Mfr's Part No.
DIODES				
D2	Diode, Silicon	1SS133		EACT0-09400
D3	Diode, Silicon	1SS133		EACT0-09400
D5	Diode, Silicon	1SS133		EACT0-09400
D6	Not used			
D8	Diode, Silicon	1SR35-200A		EACT0-09200
ZENER DIODES				
D1	Diode, Silicon, Zener	RD2.7EB		EADT0-08900
D4	Diode, Silicon, Zener	MTZ5.1B		EADT0-19900
D7	Diode, Silicon, Zener	MTZ5.1B		EADT0-19900
DIODE ARRAYS				
DA1	Not used			
DA2	Not used			
DA3	Diode Array	DAN201		EAC00-09300
DA4	Diode Array	DAN201		EAC00-09300
DA5	Diode Array	DAP201		EAC00-09900
INTEGRATED CIRCUITS				
IC1	I.C., Disk Read Amplifier	HA16631P		EAS00-12700
IC2	I.C., TTL, NAND Gate	SN75452 or		EAQ00-05000
		HD75452		EAQ00-05000
IC3	I.C., TTL, Flip-Flop	SN74LS74A or		EAQ00-12700
		HD74LS74A		EAQ00-12700
IC4	I.C., TTL, Inverter	SN7406 or		EAQ00-07500
		HD7406		EAQ00-07500
IC5	I.C., TTL, Flip-Flop	SN74LS74A or		EAQ00-12700
		HD74LS74A		EAQ00-12700
IC6	I.C., FDC	EC-877		EA006-40700
IC7	I.C., TTL, EX-OR Gate	SN74LS86 or		EAQ00-15900
		HD74LS86		EAQ00-15900
IC8	Not used			
IC9	Not used			
IC10	I.C., TTL, Schmitte-Trigger	SN74LS14 or		EAQ00-17200
		HD74LS14		EAQ00-17200
IC11	I.C., TTL, NAND Gate	SN7438 or		EAQ00-10000
		HD7438		EAQ00-10000
IC12	I.C., Transistor Array	μPA2003		EAS00-03000

Ref. No.	Description		RS Part No.	Mfr's Part No.
IC13	I.C., TTL, NAND Gate	SN7438 or HD7438		EAQ00-10000 EAQ00-10000
IC14	I.C., TTL, NOR Gate	SN74LS02 or HD74LS02		EAQ00-15800 EAQ00-15800
COILS				
L1	Coil, Choke	330μH/500mA		EDDT0-06800
L2	Coil, Choke	330μH/500mA		EDDT0-06800
L3	Coil, Choke	100μH/500mA		EDDT0-06900
L4	Coil, Choke	470μH/500mA		EDDT0-06700
LEDS				
LED A	Photo Diode			EAH00-06200
LED B	Photo Diode			EAH00-06200
RESISTORS				
R1	Resistor, Carbon	220 ohm/1/4W ±5%		ECC1GT221JB
R2	Resistor, Carbon	39K ohm/1/4W ±5%		ECC1GT393JB
R3	Resistor, Carbon	560 ohm/1/4W ±5%		ECC1GT561JB
R4	Resistor, Carbon	100K ohm/1/4W ±5%		ECC1GT104JB
R5	Resistor, Carbon	100K ohm/1/4W ±5%		ECC1GT104JB
R6	Resistor, Carbon	820 ohm/1/4W ±5%		ECC1GT821JB
R7	Resistor, Carbon	270 ohm/1/4W ±5%		ECC1GT271JB
R8	Resistor, Carbon	270 ohm/1/4W ±5%		ECC1GT271JB
R9	Resistor, Carbon	220 ohm/1/4W ±5%		ECC1GT221JB
R10	Resistor, Carbon	10K ohm/1/4W ±5%		ECC1GT103JB
R11	Resistor, Carbon	47K ohm/1/4W ±5%		ECC1GT473JB
R12	Resistor, Carbon	560 ohm/1/4W ±5%		ECC1GT561JB
R13	Resistor, Carbon	470 ohm/1/4W ±5%		ECC1GT471JB
R14	Resistor, Carbon	10K ohm/1/4W ±5%		ECC1GT103JB
R15	Resistor, Carbon	5.6K ohm/1/4W ±5%		ECC1GT562JB
R16	Resistor, Carbon	5.6K ohm/1/4W ±5%		ECC1GT562JB
R17	Resistor, Carbon	2.2K ohm/1/4W ±5%		ECC1GT222JB
R18	Resistor, Carbon	2.2K ohm/1/4W ±5%		ECC1GT222JB
R19	Not used			
R20	Resistor, Carbon	10K ohm/1/4W ±5%		ECC1GT103JB
R21	Resistor, Metal Oxide Film	47 ohm/1/2W ±5%		CFE61-05501
R22	Resistor, Carbon	10K ohm/1/4W ±5%		ECC1GT103JB
R23	Resistor, Carbon	820 ohm/1/4W ±5%		ECC1GT821JB
R24	Resistor, Metal Oxide Film	110 ohm/1W ±5%		CFE61-05301
R25	Not used			
R26	Resistor, Carbon	47K ohm/1/4W ±5%		ECC1GT473JB
R27	Resistor, Carbon	2.4K ohm/1/4W ±5%		ECC1GT242JB
R28	Resistor, Carbon	39K ohm/1/4W ±5%		ECC1GT393JB
R29	Resistor Carbon	470 ohm/1/4W ±5%		ECC1GT471JB
R30	Not used			
R31	Not used			
R32	Not used			
R33	Not used			

Ref. No.	Description		RS Part No.	Mfr's Part No.
R34	Resistor, Carbon	10K ohm/1/4W ±5%		ECC1GT103JB
R35	Resistor, Carbon	1K ohm/1/4W ±5%		ECC1GT102JB
R36	Resistor, Carbon	180 ohm/1/4W ±5%		ECC1GT181JB
R37	Resistor, Carbon	1K ohm/1/4W ±5%		ECC1GT102JB
R38	Resistor, Carbon	10K ohm/1/4W ±5%		ECC1GT103JB
R39	Resistor, Carbon	1K ohm/1/4W ±5%		ECC1GT102JB
R101	Not Used			
RESISTOR ARRAYS				
RA1	Resistor Array	2K x 2, 22K x 2 1/8W ±5%		ECM00-18300
RA2	Resistor Array	3K x 2, 10K x 2 1/8W ±5%		ECM00-18100
RA3	Resistor Array	2.2K, 10K, 150, 270 1/8W ±5%		ECM00-17900
RA4	Resistor Array	330 x 2, 2K x 2 1/8W ±5%		ECM00-18200
RA5	Resistor Array	10K x 4 1/8W ±5%		ECM00-18000
RA6	Resistor Array	470 x 2, 1K x 2 1/8W ±5%		ECM00-18400
RA7	Resistor Array	4.7K x 4 1/8W ±5%		ECM00-00300
RA8	↓			↓
RA9				
RA10	Resistor Array	4.7K x 6 1/8W ±5%		ECM00-09800
TRANSISTORS				
Q1	Transistor, NPN, 2SC2021, Silicon, NO-Rank			EAA00-18900
Q2	Transistor, NPN, 2SC2021, Silicon, NO-Rank			EAA00-18900
Q3	Transistor, PNP, 2SA937, Silicon, NO-Rank			EAB00-10300
Q4	↓			↓
Q5				
Q6				
Q7	Transistor, PNP, 2SA937, Silicon, NO-Rank			EAB00-10300
Q8	Not used			
Q9	Transistor, NPN, DTC114, Silicon, NO-Rank			EAA00-18800
Q10	Transistor, PNP, 2SA937, Silicon, NO-Rank			EAB00-10300
Q11	Transistor, NPN, 2SC2021, Silicon, NO-Rank			EAA00-18900
Q12	Not used			
Q13	Transistor, PNP, 2SA881, Silicon, NO-Rank			EAB00-10700
POTENTIOMETER				
VR1	Variable Registor			ECA00-14200
MISCELLANEOUS				
DS1	Short Pin, Female	DIC-S252		EEF00-20900
RA11	Socket, IC	DILP14P-8J		EED00-05600
SW1	Short Pin Plug	FFC-(10) BMEP2		EEF00-20800
SW2	Not Used			
TP1	Connector, 4 Pin Male	W-P5004#01		EEB00-51200
TP2	Connector, 5 Pin Male	W-P5005#01		EEB00-51300

MECHANICAL AND ASSEMBLY PARTS

Ref. No.	Description	RS Part No.	Mfr's Part No.
M1	Clamp Base BK Assembly		CFABK-60101
M16	Clamp, BK		CFABK-60601
M17	Base, Clamp K		CFAAK-60101
M18	Arm, Clamp K		CFAAK-60201
M19	Shaft, Clamp Lever		CFA10-60301
M20	Spring, Clamp Lever		CFA30-60301
M21	Cam, Clamp		CFA35-60501
E1	E-Ring M3		SRE030000E0
M2	Carrier A Assembly		CFABK-60205
M22	Carrier A-K		CFAAK-60405
M23	Pad K		CFAAK-02101
M24	Shaft, Load Arm		CFA10-00201
M25	Spring, Load Arm		CFA30-00201
M26	Arm III, Load		CFA35-02801
M3	Pulse Motor BK Assembly		CFABK-60403
M27	Motor K, Pulse		CFAAK-60703
M28	Frame 2, Motor		CFA20-62901
M29	Stopper, TR00		CFA20-63601
M30	Supporter, Belt		CFA20-61001
M31	Belt, Steel		CFA45-60701
M32	Plate, Belt Fastening		CFA20-60501
SMW2	Bolt, M2.6 x 4		CFA45-61001
M36	Stopper, Belt		CFA20-63301
M33	Clamp, Cable		CFA20-63401
SM3	Screw, Pan Head, Sems M2.6 x 4		CFA45-62301
N1	Nut, Hexagonal M3		SNC030018A2
SPW1	Washer 2.8 x 5 x 0.5		SWA028050A2
M4	Cover, Front, Black		CFAAK-60801
M5	DD Motor K Assembly		CFAAK-60301
M6	Interrupter AK Assembly		CFAAK-61201
M7	P.C.B. Assembly		CFEAK-06110
M8	Shaft, Carrier		CFA10-61201
M9	Support, Shaft, Inside		CFA20-60601
M10	Support, Shaft, Outside		CFA20-60701
M11	Lever, Clamp		CFA35-60601
M12	Insulator		CFA45-60901
S1	Screw, Bind Head, Machine, M3 x 6		CFA45-61401
S2	Screw with Washer M3 x 6		SST230060A2
S3	Screw, Bind Head, Machine, M3 x 8		CFA45-61402
S4	Screw with Washer M3 x 8		SST230080A2
S5	Screw, Dish Head M3 x 8		SSS230080A2
SM1	Screw, Pan Head, Sems M2.6 x 6		SSW226060A1
SM2	Screw, Pan Head, Sems M2.6 x 8		SSW226080A2
SMW1	Screw, Pan Head, Double Sems M4 x 10		SSX240100A2
M15	Guide, Cable K		CFA35-61401
M34	Terminal		EEH00-05600

Part 6 Special Maintenance Tools

1. Belt Tensioning Jig (CFABK-60801)

• Refer to Mechanical Explanation on Page C-8.

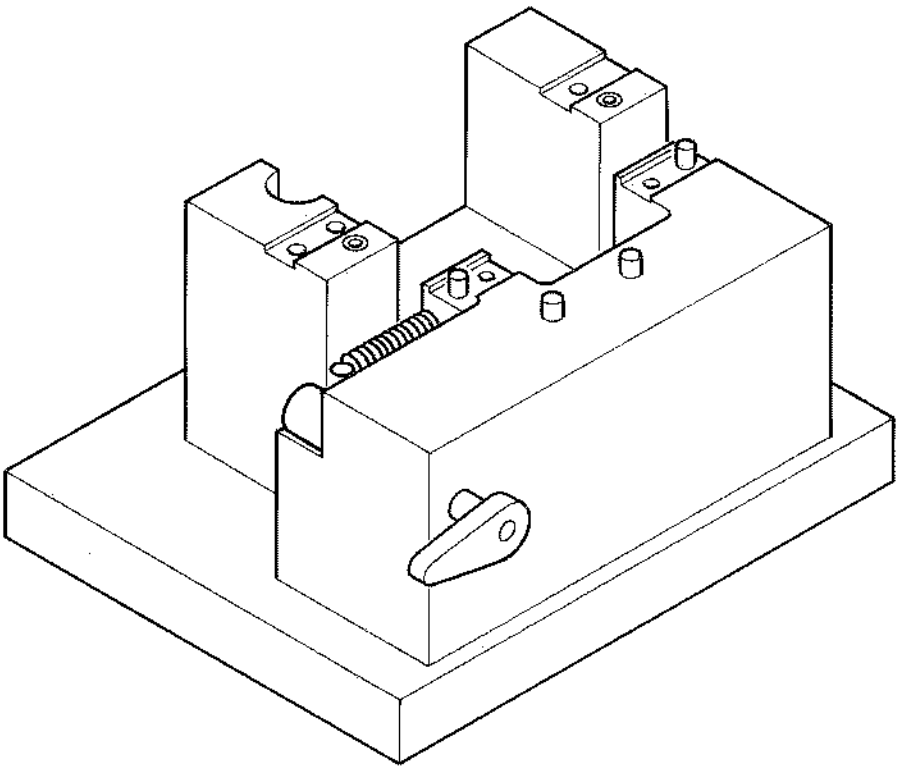


Figure C-47. Special Maintenance Tool

RADIO SHACK, A DIVISION OF TANDY CORPORATION

U.S.A.: FORT WORTH, TEXAS 76102
CANADA: BARRIE, ONTARIO L4M 4W5

TANDY CORPORATION

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