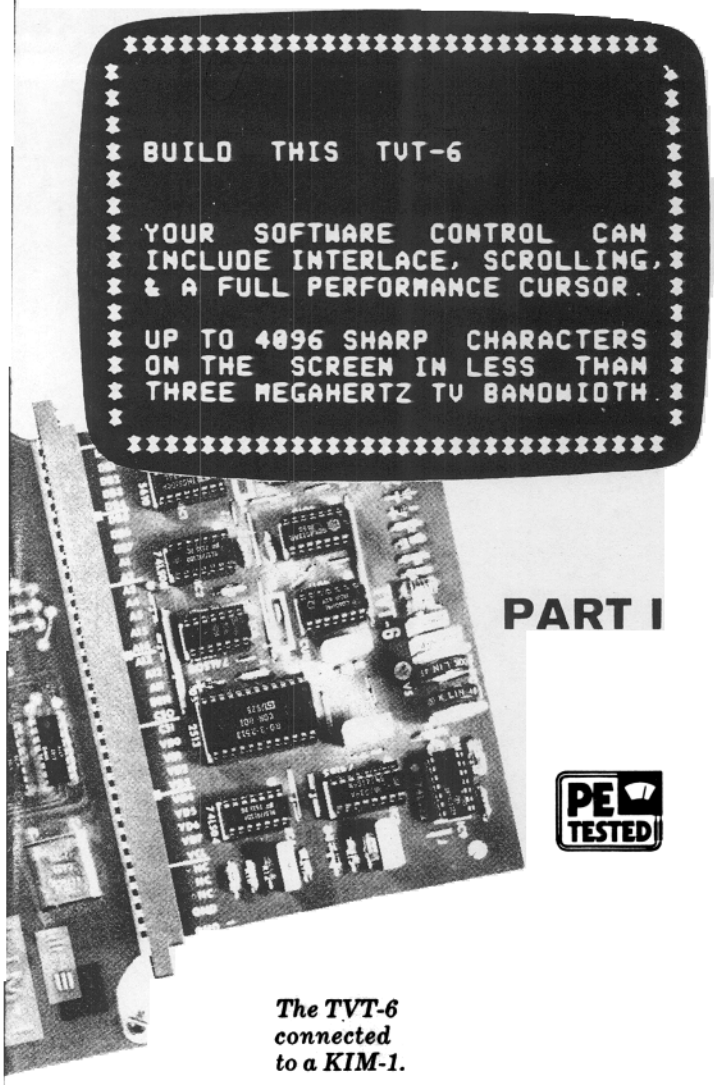


The TVT-6 connected to a KIM-1.

Build the TVT-6: A Low-Cost DIRECT VIDEO DISPLAY

PART I

PE TESTED

$35 microcomputer "add-on" provides:

- ***User-selectable line lengths***
- ***Scrolling***
- ***Up to 4k on-screen characters with only 3-MHz bandwidth***

BY DON LANCASTER

Thanks to some software tricks, a simple and low-cost add-on circuit, and a new way to speed up a microprocessor, you can now build a video interface for your microcomputer for an investment of only $20 to $35. The TVT-6 video system described here permits the choice of virtually any format including 16/32 (16 lines of 32 characters), 16/64, or 32/64. It also features full editing capability and full-performance cursor.

In spite of its simplicity (10 low-cost IC's), the circuit employs a new approach to video processing that permits up to 4000 characters to be displayed on-screen within a 3-MHz bandwidth. Although the TVT-6 was designed for the 6502 microprocessor based KIM-1, software can be used to easily map into the JOLT, EBKA, or Ohio Scientific microcomputers. In addition, the TVT-6 can be adapted to other microprocessors, including the popular 6800, 8080, and Z80. It is easiest to use with 16-address-line systems that operate on a single 5-volt supply and 1-μs cycle time.

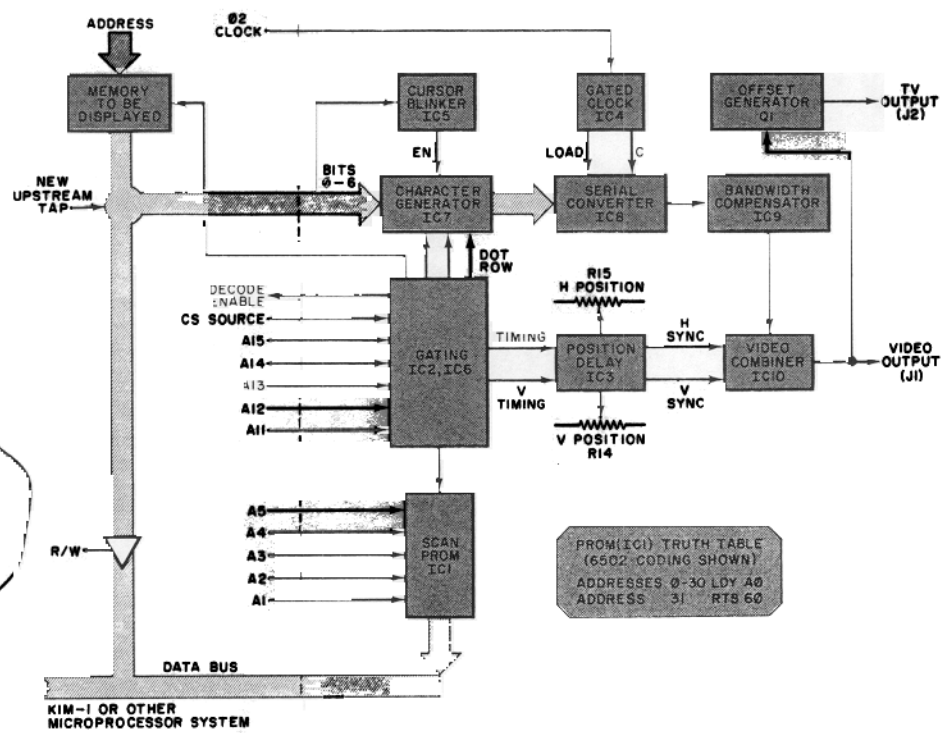


Fig. 1. TVT-6 block diagram and truth table for the PROM.

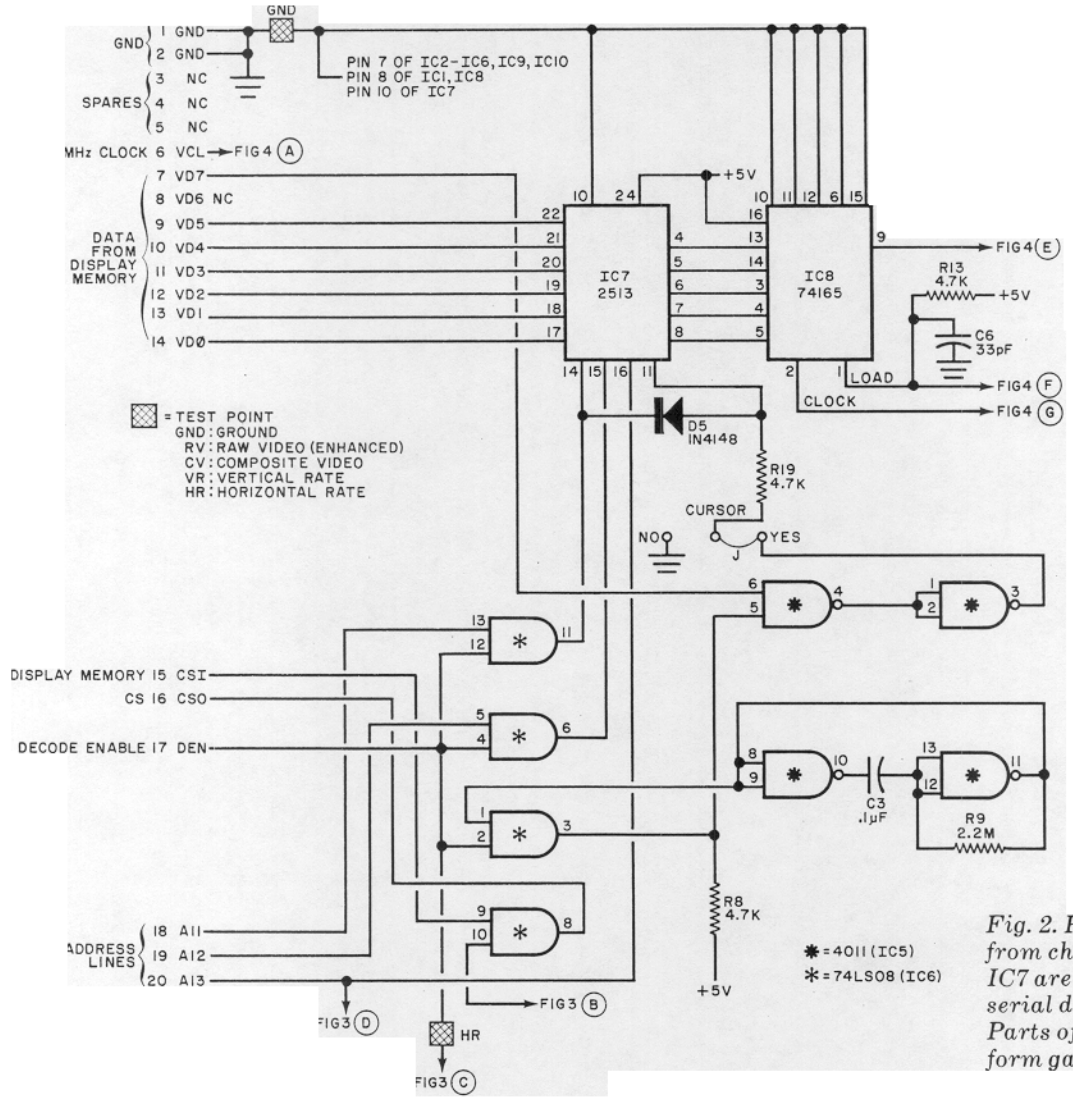


Fig. 2. Parallel outputs from character generator IC7 are converted into serial data in IC8. Parts of IC5 and IC6 form gating circuits.

Other systems will require software and microprogramming translation for their particular machine languages.

In this first of a two-part article, we will cover the hardware and construction details for the TVT-6. Next month, we will cover debugging, some useful software for the system, and provide instructions on how to couple the TVT-6 to other microprocessors.

Circuit Operation. A block diagram of the TVT-6, as used with the KIM-1 system, is shown in Fig. 1. The complete schematic diagram of the video system is shown in Figs. 2 through 4.

As shown in Fig. 1, bits ϕ through 6 from the "upstream tap" on the KIM display memory drive character generator *IC7* whose blanking and formatting are helped along by the AND gates in *IC6*. The cursor bit (bit 7) is stripped off the upstream tap and routed to cursor blinker *IC5*, which introduces a blinking cursor into the character generator's enable input.

The parallel outputs from *IC7* go to

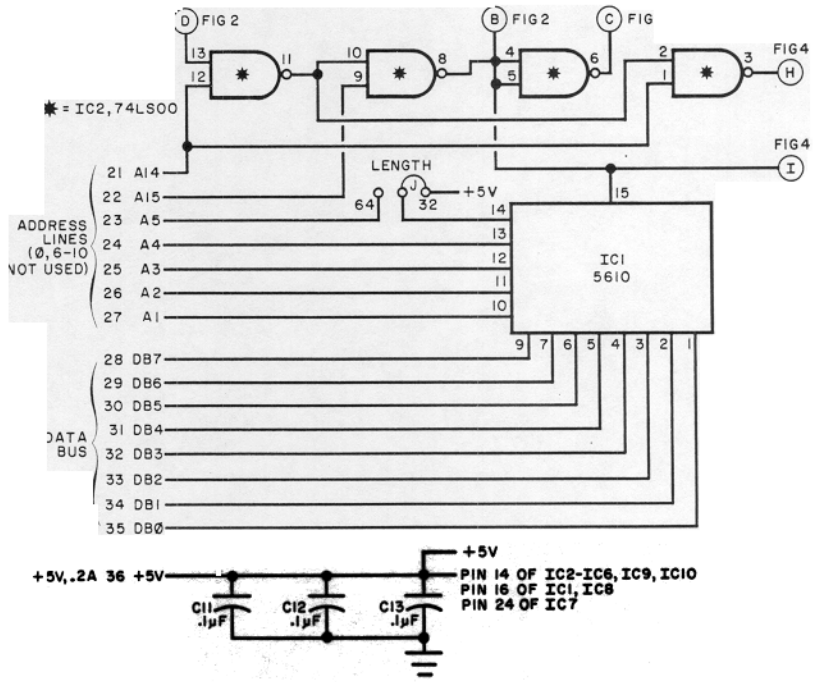


Fig. 3. New SCAN instruction uses PROM IC1, which also has the line length option in its circuit.

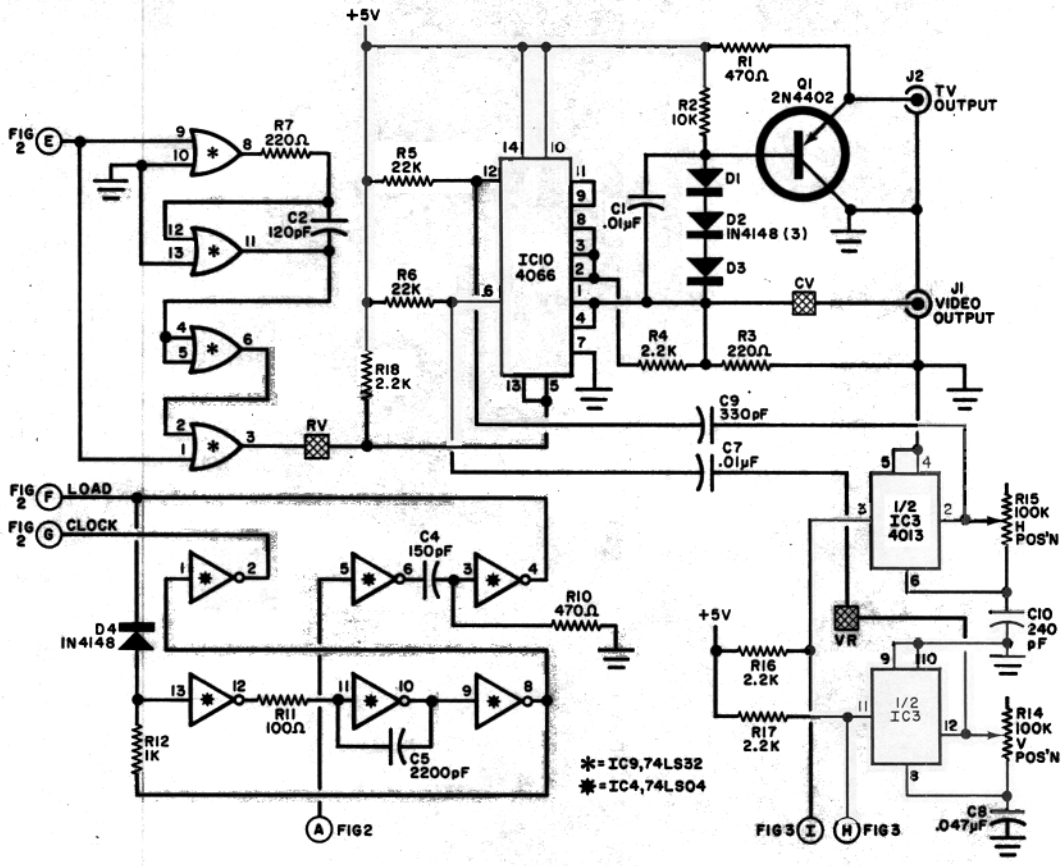


Fig. 4. Video combiner (IC10), offset generator (Q1) and sync delay circuits deliver video to TV. Gated clock (IC4) controls parallel-to-serial converter.

PARTS LIST

C1, C7—0.01-μF Mylar capacitor
C2—120-pF polystyrene capacitor
C3, C11, C12, C13—0.1-μF Mylar capacitor
C4—150-pF polystyrene capacitor
C5—2200-pF polystyrene or Mylar capacitor
C6—33-pF polystyrene capacitor
C8—0.047-μF Mylar capacitor
C9—330-pF polystyrene capacitor
C10—240-pF polystyrene capacitor
D1 through D5—IN4148 silicon diode
IC1—IM5610 32×8 PROM (or similar)
IC2—74LS00 quad tri-state NAND gate IC
IC3—4013 dual-D flip-flop IC
IC4—74LS04 hex inverter IC
IC5—4011 quad NAND gate IC
IC6—74LS08 quad AND gate IC
IC7—2513 character generator (must be single-supply type, such as General Instruments No. RO-3-2513)
IC8—74165 PISO shift register
IC9—74LS32 quad OR gate IC
IC10—4066 quad analog switch IC
J1, J2—Pc-mount phono jack (Molex No. 15-24-2181 or similar)
Q1—2N4402 or MPS6523 (Motorola) transistor

The following resistors are ¼ watt, 10% tolerance:

R1, R10—470 ohms
R2—10,000 ohms
R3,R7—220 ohms
R4,R16,R17,R18—2200 ohms
R5,R6—22,000 ohms
R8,R13,R19—4700 ohms
R9—2.2 megohms
R11—100 ohms
R12—1000 ohms
R14,R15—100,000-ohm pc-type (upright) potentiometer
Misc.—Sockets for IC's (seven 14-pin, two 16-pin, one 24-pin); 36-contact edge connector with 0.156" centers (Amphenol 225 or similar); solid hook-up wire for jumpers; insulated sleeving; test-point terminals (5); solder; etc.

Note: The following items are available from PAIA Electronics, Box 14359, Oklahoma City, OK 73114: No. PVI-1PC printed circuit board for $5.95; complete kit of all parts, No. PVI-1K, for $34.95 (specify blank or KIM-1 programmed *IC1*); KIM-1 coded cassette, with programs, No. PVI-1CC, for $5.00. All prices postpaid.

shift register *IC8*, where they are converted into a serial video signal. The clock and load commands for *IC8* come from gated oscillator *IC4*, which derives its signals from the microcomputer's clock. It is important that the correct clock phase be selected to permit the loading of *IC8* to occur when the output of the character generator is valid and settled. This is phase 2 in the KIM-1. (If you are using a different μP based computer, check this detail.)

The serial video from *IC8* goes to the TV Bandwidth Compensator in *IC9*, which predistorts the video by delaying the video output and OR'ing it against itself. This widens the vertical portions of all characters to generate clean and crisp characters that require minimum bandwidth. The amount of widening is determined by *C2* (Fig. 4). The optimum value of *C2* is obtained when the generated M or W in the video display just barely closes.

The vertical and horizontal timing signals from *IC2* in the gating circuit are delayed by *IC3*. The display positioning can be varied by potentiometers *R14* and *R15*. The vertical and horizontal sync signals are combined with the enhanced video from *IC9* into video combiner *IC10*. The output from *IC10*, available at *J1*, is composite video, with the sync tips at ground, black at 0.4 volt, and white at 1.6 volts. This output can be used to drive conventional video moni-

tors and converted TV receivers. The video output from *IC10* is also fed to *Q1*, which is offset to deliver a +4-volt output for the white level. This output, available at *J2*, can be connected directly to the first video amplifier of most transformer-powered solid-state TV receivers (see box for details) without requiring biasing, coupling, or translation circuits.

Two options are provided with the TVT-6, both of which are jumper selected. The LENGTH option allows a choice of either 32 or 64 characters/line. The CURSOR option gives the choice of either no cursor or allows the cursor to be displayed under software control.

Construction. The actual-size etching and drilling guide for the printed circuit board used in the TVT-6 is shown in Fig. 5, along with the component-installation diagram. Start assembly by installing and soldering into place the 21 jumpers and test points. (Note that insulated sleeving must be used on two of the long jumpers.) Install the IC sockets, resistors, capacitors, diodes, jacks, and position controls *R14* and *R15*. Do not install the IC's at this time. The correct IC installation sequence and the waveforms to be observed will be discussed in Part 2 next month.

Computer Interface. Detailed in Table I are the requirements of each of the edge connector contacts on the TVT-6 and how to use each contact. Table I also contains the KIM-1 interface connection instructions. The interface consists of adding a new connector and making some add-on connections. One circuit board trace is cut on the KIM-1's pc board to permit an optional changeover switch (or jumper) to be added to the microcomputers. This permits KIM-1 to be used with or without the TVT-6.

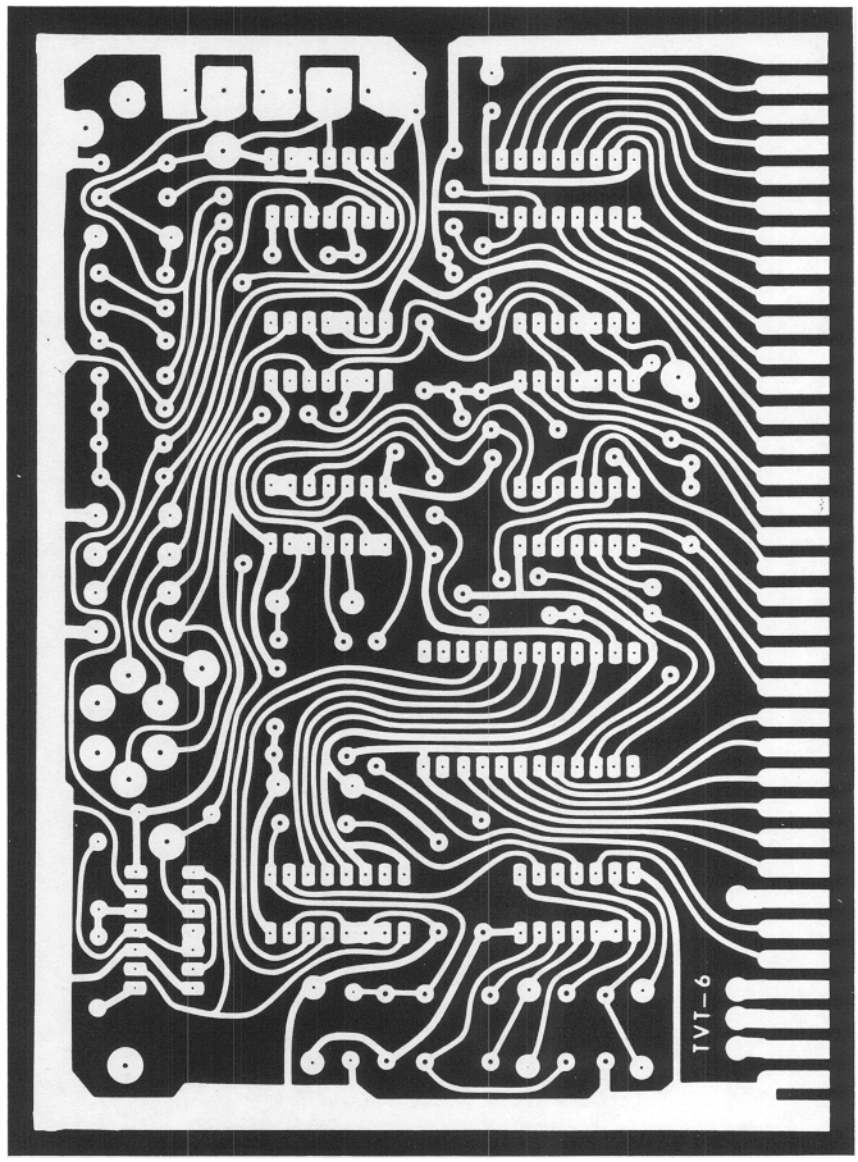
General Operation. Since most of today's TVT circuits are used with a microprocessor or microcomputer, it is best to do as much of the display control as possible with the microprocessor and some software. What may not be obvious is that almost all of the timing in the system can also be done using the microprocessor. All this takes is a few dozen words of code.

The four key secrets of operation for the TVT-6 are:

1. Carefully choose how the address lines are defined for TVT operation.

2. Add a new instruction, which we call SCAN, to rapidly address 32 or 64 sequential memory locations.

3. Permanently connect an upstream



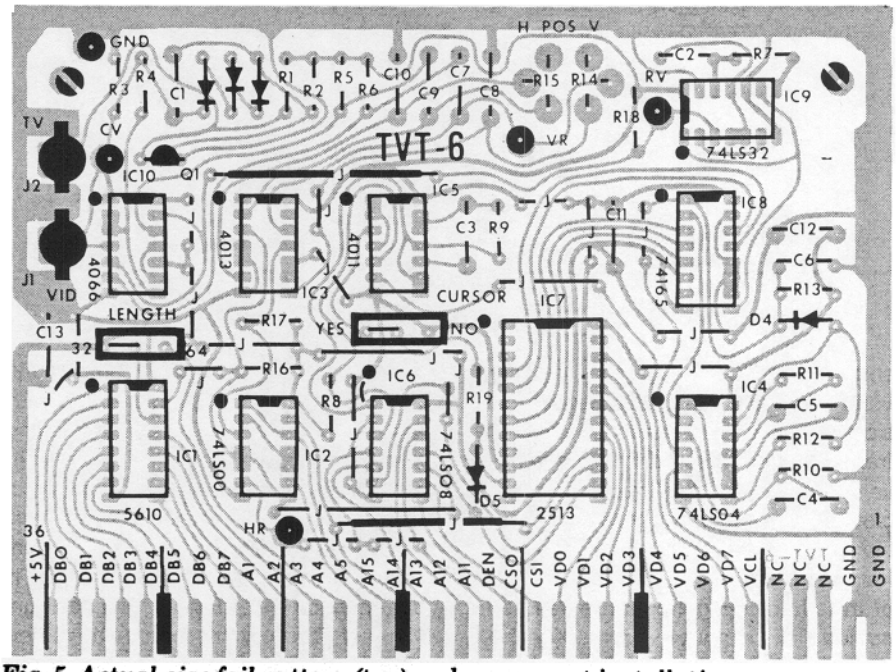


Fig. 5. Actual-size foil pattern (top) and component installation (below). Use sockets for all IC's. Edge connectors go to KIM-1.

TABLE I
TVT-6 PINOUT AND KIM-1 INTERFACE

TVT-6 CONTACT	NAME	REMARKS
1,2	GND	Heavy wire to expansion contact 22 or similar point in KIM-1
3, 4, 5	NC	Spares
6	VCL	1-MHz clock from expansion contact U(ϕ2). (In other systems clock phase must be selected so that load pulse arrives when CG is valid.)
7,8,9,10, 11,12,13, 14	VD7, VD6, VD5, VD4, VD3, VD2, VD1, VDϕ	Data output from memory display; drives character generator. For KIM-1 to display any part of pages 00 through 03, connections must be made as follows:

TVT-6 contact:	to pin 12 of KIM-1 IC:
7	U5
8	U6
9	U7
10	U8
11	U9
12	U10
13	U11
14	U12

15	CSI	Display memory chip select from μP; negative logic OR combined with TVT-6 chip select. From pin 1 of U4 on KIM-1.
16	CSO	Display memory chip select source; enables display memory when either TVT-6 is active or contact 15 is low. Goes to pin 13 of U5 through U12 in KIM-1 when displaying any part of pages 00 through 03. Existing Kϕ connection in KIM-1 must be broken.
17	DEN	Decode enable; goes low when μP is operated in normal mode, high when TVT-6 is doing an active scan. Goes to KIM-1 Applications contact K. Any external ground on applications contact K should be removed.
18,19,20, 21,22,23, 24, 25, 26, 27	A11, A12, A13, A14, A15, A5, A4, A3, A2, A1	Address inputs from μC, positive true. Addresses Aϕ, A6 through A10 not sent to TVT-6. Connections to KIM-1 expansion:

KIM-1 contact:	to TVT-6 contact:
N (A11)	18
P (A12)	19
R (A13)	20
S (A14)	21
T (A15)	22
F (A5)	23
E (A4)	24
D (A3)	25
C (A2)	26
B (A1)	27

28, 29, 30, 31,32,33, 34, 35	DB7, DB6, DB5, DB4, DB3, DB2, DB1, DBϕ	μP data bus; tri-state active high from IC1 during active scan, not used at other times. Connections to KIM-1 expansion:

KIM-1 contact:	to TVT-6 contact:
8 (BD7)	28
9 (DB6)	29
10 (DB5)	30
11 (BD4)	31
12 (DB3)	32
13 DB2)	33
14 (DB1)	34
15 (DBϕ)	35

36	+5V	Regulated +5-volt (200-mA) power bus; should be heavy wire. From KIM-1 expansion contact 21 or similar point to contact 36 in TVT-6.

Note: KIM-1 conversion consists of breaking one foil trace and adding a new 36-pin socket (Amphenol 127 or similar). Connection to be broken originates as Kϕ(pin 1 of U4). Routing of Kϕthat goes to memory chip select pin 13 of U5 through U12 should be broken. Other Kϕconnections, such as that to pin 1 of U16 should remain intact. Any external ground connections to Application connector contact K (decode-enable) must be removed. All wiring should be made with a wiring pencil.

When KIM-1 is used *without* displaying video, it will behave normally and transparently as long as TVT-6 is plugged in and addresses 8000 through DFFF are not used. To restore KIM-1 operation with TVT-6 out of socket, or to use available addresses for other programs, jumper pin 15 to pin 16 and separately jumper pin 1 to pin 17 in the KIM-1. Note that this jumpering is to be done only when TVT-6 is out of its connector. I you wish, a dpdt changeover switch can be added to perform the jumpering. Switch positions should be changed only when power is off.

memory tap to the character generator and display circuit.

4. Create special software that will allow TVT-6 scanning.

All 16 address lines are used, assigned as shown in Fig. 6A for a 32-character/line system or as shown in Fig. 6B for a 64-character/line system. Address A15 is the horizontal sync pulse and the key to jumping to the new SCAN instruction. This pulse is followed in descending address order by the vertical sync (A14) and three lines (L4, L2, L1) that produce the "what row of dots do we want?" information for the character generator. The lower address lines are used to select a page of display memory and to select the character that goes into any particular horizontal and vertical location on the display.

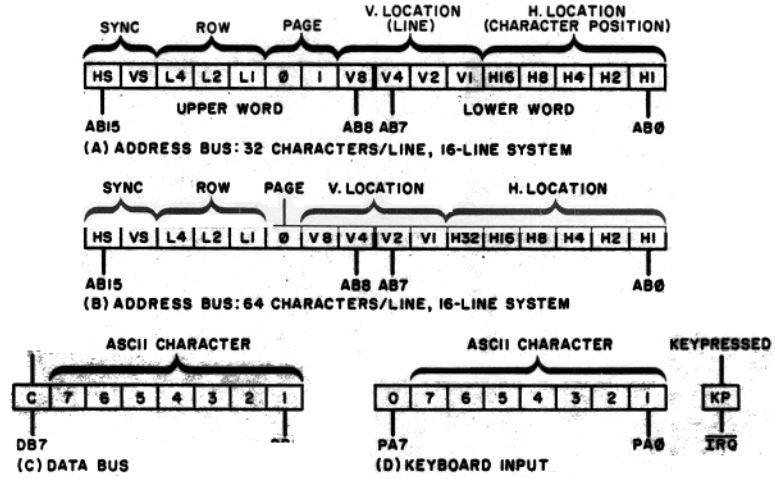
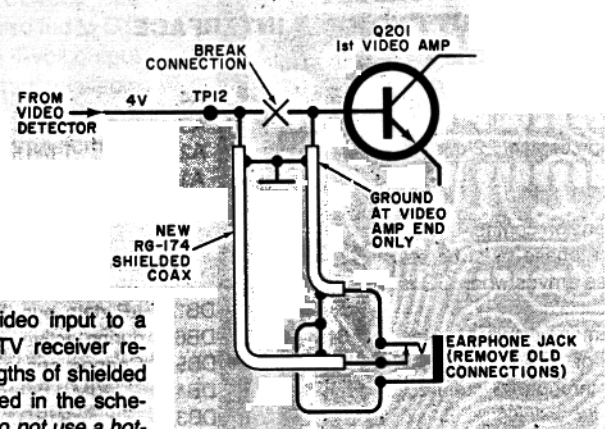


Fig. 6. Bus definitions as used with the TVT-6. All 16 address lines are used as described in text.

DIRECT-VIDEO INPUT CONVERSION



Adding a TVT-6 direct-video input to a small-screen solid-state TV receiver requires only two short lengths of shielded coaxial cable, as illustrated in the schematic. (Important Note: *Do not use a hot-chassis TV receiver!* Make absolutely certain that the TV receiver you use is transformer powered from the ac line.) The conversion circuit shown here is for the Sears No. 562-50260500 (Sams Photofact No. 1565-1). Other TV receivers can be modified in a similar manner.

The earphone jack in the circuit provides automatic changeover from normal receiver performance to video access. Correct bias is provided by TV output of the TVT-6. As an option, you can defeat the sound trap in the Sears TV receiver by lifting one end of capacitor *C201*.

interrupt and reset vectors on the KIM-1 so that the operating system will work compatibly and properly with the new SCAN instruction.

There are many possible codings for the SCAN program with the limitation that the last address is a return-to-subroutine (RTS) instruction. The obvious choice of NOP or EA runs at only half speed and can't be used. Of the three dozen instructions that operate at full speed, the choice of LDY is the one that does not disturb the accumulator or its flags. This adds flexibility to other programs. The Y register can be viewed as a write-only memory in the SCAN software and we can think of the whole SCAN instruction as a group of double-speed fetch-but-don't-execute instructions. Theoretically, a 64-word PROM would be required for a 64-character line, but this can be overcome by ignoring address Aϕ and changing the PROM's address every second cycle of the machine.

The data within the machine (see Fig. 6C) uses the lowest seven bits as ASCII character storage. This is arranged by putting the least-significant ASCII character bit in the least-significant data slot, and so on up through the more significant bits. The eighth data bit (DB7) is reserved for a cursor. If DB7 is a zero, a character is displayed, while if it is a one, a cursor box is optionally displayed.

The existing KIM-1 keypad can be used as an ASCII keyboard for many applications, particularly for setup and debugging. If you wish to add an external ASCII keyboard and encoder, connect it to the KIM-1's parallel interface A, following the assignments shown in Fig. 6D. The seven ASCII bits go to the seven low-order data lines, while PA7 is hard wired for a zero. The keypress, or strobe, signal from the keyboard must pull the IRQ (interrupt request line) to ground for 10 μs to enter a character or machine command.

The truth table for PROM *IC1* is shown in Fig. 1. This truth table stores the SCAN instruction, activated by addresses 8000 through DFFF. When *IC1* is enabled, it causes the microprocessor's program counter to appear on the address lines for 32 or 64 consecutive scans that advance one count per microsecond. This automatically and sequentially addresses the display memory and produces exactly the data needed for a horizontal scan of TVT characters. The scan instruction runs at least twice as fast as the microprocessor normally moves, which is the key to TVT timing with a microprocessor.

To use the SCAN instruction, jump to a subroutine whose starting address is within the 8000 to DFFF range. For example, if you call JRS 8200, the SCAN instruction will deliver a horizontal sync pulse and initiate operation on the top row of characters, starting with the first character on page 2. After a selected 32 or 64 characters, the SCAN instruction automatically jumps back to the main program.

The SCAN instruction can be viewed as a "portable subroutine" because it readily moves around to automatically output the correct page and character generator's row information, starting with an easily computed JSR address. Addresses above DFFF will not activate the SCAN instruction. This includes the

Upstream Tap. The SCAN instruction will sequentially address 32 or 64 memory slots per horizontal scan line at a rate of one-per-clock cycle (1 μs). These addresses are presented to the entire memory in the computer, including the memory to be displayed. However, during the display times, the SCAN instruction and its PROM have control of the data bus so that the display memory (or anything else) cannot output information to the data bus.

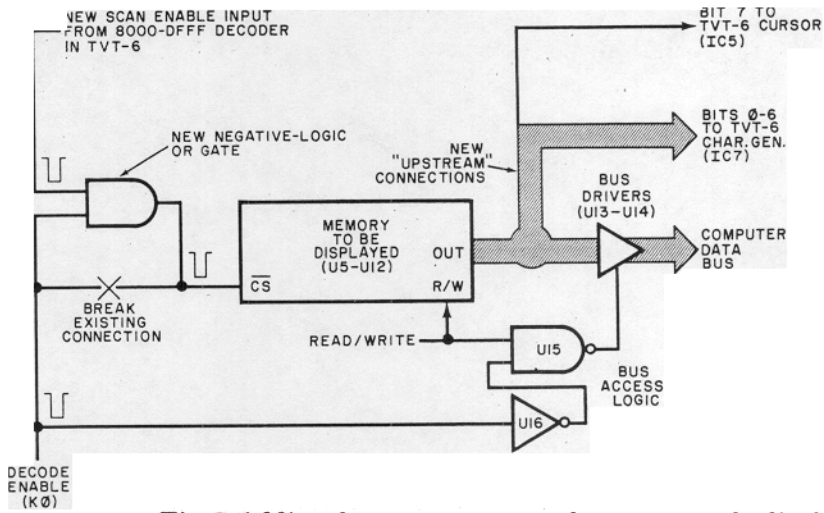


Fig. 7. Adding the upstream tap to the memory to be displayed.

The upstream tap is added as shown in Fig. 7. This tap is always outputting information to the character generator in the TVT-6. The output information is present even (and especially) when the display memory data bus drivers have been inactive. ◇