jection is 60 dB at 50/60 Hz, and the input is protected to 2000 volts dc plus peak on all ranges.

There are four ac voltage ranges that go up to 2, 20, 200, and 1000 volts full-scale. Accuracy on the three low ranges is 0.5%, while on the 1000-volt range, it is 0.75%. Measurements can be made down to 1 mV on the 2-volt range. The input impedance is rated at 1.5 megohms shunted by less than 100 pF. The frequency response is from 40 to 5000 Hz ±0.5 dB. The average-detecting measuring system provides rms readings. Input protection is to 2000 volts peak and dc or 1400 volts rms. The five ac and dc current ranges go to 200 μA, 2 mA, 20 mA, 200 mA, and 2 A full-scale. Measuring accuracy is 0.3% on dc and 1.0% of reading plus three digits on ac. Resolution is rated at 0.1 μA on the 200-μA range. The internal shunt resistance on the respective ranges is 1000, 100, 10, 1, and 0.1 ohms. The voltage drop is 200 mV on the three lower ranges, 250 mV on the 200-mA range, and 1 volt on the 2-A range. The input is protected up to 2000 volts dc and peak.

Resistance measurements can be made with either high or low power. The high-power ranges (to 2 k, 20 k, 200 k, 2 megohms, and 20 megohms full-scale) deliver a 1-volt maximum test potential to the test probes. The low-power ranges (200 ohms, 2 k, 20 k 200 k, and 2 megohms full-scale) deliver a 0.2-volt test potential to the probes. Accuracy is rated at 0.2% ±3 digits on all but the 20-megohm range, where it is 0.5% ± 3 digits. Resolution is 0.1 ohm on the 200-ohm range. Maximum current through the resistance being measured is 1 mA, 100 μA, 20 μA, 1 μA, and 0.1 μA on the low-power-ohms ranges and 500, 50, 5, and 0.05 μA for the high-power ranges. Input protection is provided to a maximum of 2000 volts dc and peak on all ranges.

The multimeter is made more useful by a permanently connected probe assembly, which consists of a flexible ground lead terminated in an insulated alligator clip and a signal lead terminated in the actual probe tip. Because these test leads are a permanent part of the DMM, they cannot be misplaced.

The special probe tip features two touch switches. The one labelled PUSH ON turns on power to the meter for as long as it is held down and instantly removes the power when released, which saves on battery power. Of course, the main power ON/OFF switch on the instrument's front panel can be used to turn on the power for continuous operation when desired. The second probe switch, labelled ISO DCV+2, provides an extra 15 megohms of isolation for critical circuits where loading presents problems, as in oscillators, very-high-impedance CMOS circuits, and the like. Operating this switch not only adds isolation resistance. It also doubles the measurement capability of the range on which it is used, as mentioned above.

User Comment. For our tests, we installed four C cells in the DMM. Then we used our usual laboratory voltage and current standards and high-tolerance resistors to check out the various functions and ranges. In each case, the instrument performed comfortably within its published specifications.

After completing our standard bench tests, we put the DMM to work under actual in-service conditions for a month, both on a service bench and in a field-service vehicle, taking no particular care to treat it gently. At the end of the test period, we could find not one fault in the instrument's performance or handling, based on combined bench and field experience. In fact, we feel it was among the most convenient multimeters we have ever used for the full range of different test and measuring conditions encountered.

At the end of the in-service test, we again examined the DMM, both physically and electrically. The DMM easily survived the rough environment of a service van. When we performed accuracy tests again, we noted no degradation from the results obtained in the original bench tests.

We like Sencore's new approach to test probes, particularly the switch that allows us to control the power to the instrument right at the probe body. The impedance and range doubling switch is a nice touch that adds practical utility to the instrument. It greatly simplified our measurements under some very trying conditions. The body of the probe itself is triangular in shape, making it comfortable to handle and easier to manipulate under actual measuring conditions than is usually the case.

In sum, the Model DVM37 combines all the utility, accuracy, and human engineering one could expect of a well-designed digital multimeter. Its high-impact case and recessed control knobs are particularly suitable for the rigors of actual servicing conditions.

CIRCLE NO. 105 ON FREE INFORMATION CARD

Computer Bits

By Hal Chamberlin

BUS SYSTEMS

ALL HOBBYIST computers have some kind of bus system for tying the various computer elements together. Component computers use a "motherboard" which contains only the bus connected to a number of pc board sockets. Each component of the system such as the CPU board or a memory board plugs into a socket and communicates with the rest of the system over the bus. Even an all-on-one-board system has a bus running around on the board to connect the CPU, memories, and input/output circuits together. For expansion purposes, the on-board bus is usually brought out to the edge of the main board.

Actually a bus sytem by itself is nothing more than a set of parallel wires. These wires can be conveniently broken down into four major groups. The most basic is the *power* group which supplies operating voltages to the circuits tied to the bus. On some systems this may consist of only two lines—one for +5 volts and the other for ground while others may have three separate power voltages, typically +15, +5, and −15 volts. Some systems may even distribute *unregulated* power voltages on the bus expecting the individual circuits to regulate the voltages as required. Often several of the bus wires are assigned as grounds in order to reduce the possibility of ground loops.

The next major group is the *data lines*. These lines carry binary data around to the various sytem components. In most systems, data either flows from a peripheral device or memory into the CPU during a *read cycle*, or flows from the CPU to a memory or peripheral during a *write cycle*. One widely used bus system has 8 lines for carrying data from the CPU *to* other system components and 8 more lines for carrying data into the CPU *from* other components. Most other systems use a single set of 8 lines for both purposes forming what is called a *bidirectional* data bus. This is allowable because none of the available microprocessor chips can simultaneously read and write.

Both schemes make use of integrated circuits having Tri-State® (National Semiconductor), sometimes called three-state, outputs which allow the outputs of several IC's on different boards to be tied onto the same bus lines. A three-state output can be in one of three conditions. Two of these are the familiar logic "0" and "1" states. The third is a *disabled* state in which the IC output essentially disconnects itself from the bus line. If only one of the three-state IC's connected to the bus line is enabled (in the "0" or "1" state) and all of the others are disabled, then the bus line assumes the logic state of the enabled IC output.

Another group is the *address lines*. Generally only the CPU supplies addresses, so frequently these are simply lines driven by the CPU and received by other system components.

The last major group is the *control signals*. These differ greatly in number and function among the various bus systems in common use; but in all cases they control the response of various system components. Many of the control signals are called *strobes*. Their purpose is to delay and qualify the response to an address or data change until the logic levels on the bus are stable. This prevents a response to erroneous address and data patterns caused by one bus line switching slightly faster than the others.

Occasionally the data lines and address lines are multiplexed onto the same physical bus wires. This is particularly advantageous in 16-bit systems since 16 bus lines and associated socket pins can be eliminated. In such a system, control lines indicate when an address or data appears on the bus. Flip-flop registers on the various system boards are used to remember the address while data transfer is taking place.

Often a bus system may have special features over and above what is required to read and write memory or I/O devices. One of these is called *direct memory access* or DMA. In a system with DMA capability, the CPU is not the only subsystem capable of generating addresses and reading or writing memory. DMA I/O devices are also allowed to do these operations. In a system with DMA capability, the address lines must also have three-state capability.

DMA is typically used by video display and floppy disk subsystems. Both of these require data transfer at such a high speed that conventional program-controled input/output techniques are not usable. In operation, a DMA device will temporarily stop the CPU and gain control of the bus for the duration of the data transfer. During this time, the full speed capability of the bus, which may easily reach 2-million bytes per second, can be utilized. When data transfer is complete, the CPU is allowed to resume normal operation. A couple of particularly sophisticated bus systems do not even stop the CPU during DMA operation. Instead, DMA transfers take place between the "cracks" when the CPU is not using the bus anyway.

The Altair Bus. By far the most popular bus system in use by hobbyists today is the original Altair bus. Although usually called the S-100 bus because of its 100 lines, its popularity approaches standardization. However, the fact re-

mains that MITS introduced it in early 1975 with its Altair 8800 computer.

Of the 100 lines, only 81 are actually assigned. Six lines are used to distribute +8, +16 and −16 volts, all rectified and filtered but unregulated. Separate data-in and data-out groups of 8 lines each constitute the data lines. Another 16 lines form the address bus. There is an unusually large complement of 43 control lines; but they are not necessarily an advantage since they are provided in their raw, undecoded state.

The bus timing and control functions are entirely dependent on the 8080 CPU for which the bus was designed.

However, when newer microprocessors such as the 8085 or the Z80 are interfaced to the S-100 bus, true compatibility with the original bus specification can only be attained by adding circuitry to "fake" the same timing and control sequences as used by the 8080. Actually most peripheral board designs, particularly static memories, can tolerate considerable variation in timing and control details and still operate satisfactorily. However, more complex boards such as floppy disk controllers and graphic display interfaces may depend heavily on standard 8080 control timing. Thus, these more complex boards may not operate correctly with a Z80 CPU board that does a poor job of faking the 8080 control sequences.

Control and timing is not the only source of potential incompatibilities among "standard" S-100 boards. Some manufacturers have assigned their own functions to the 19 unused bus lines. Of course, with only 19 to go around, not everyone has assigned them to the same functions. Nevertheless, the S-100 bus is the closest thing to a standard bus this industry has.

Benton Harbor (Heath) Bus. Another bus structure that has just been introduced with the announcement of the H8 microcomputer is the "Heath" bus. Unlike the S-100 bus, this one was carefully planned with the benefit of 2 years hindsight of the hobby computer market. Major differences are the much smaller number of lines, 50 instead of 100, and more generalized control signal assignments. The smaller number of bus lines and use of less expensive board-bus connectors greatly reduces the cost of a motherboard/bus system over the S-100 equivalent. Generalized control signals make the transition to newer processors more orderly.

Eight lines are used to distribute +18, +8, and −18 volts, all unregulated. Four of these are grounds scattered among the other signals to further reduce noise. Although separate address and data busses are used, the data bus is bidirectional in order to conserve bus lines. The control signals are already decoded on the bus into the basic 4 operations; memory read, memory write, I/O read, and I/O write.

KIM-1 Bus. Probably the most popular "one board" microcomputer is the KIM-1. Although it has most of the subsystems needed for a complete system already on-board, it also has a 44-pin edge connector which brings the CPU bus out for expansion. While the busses described earlier were all TTL busses, capable of driving dozens of subsystems boards simultaneously, the KIM-1 bus is a "MOS" bus having limited drive capability. Using the signals raw, a maximum of four expansion boards can be driven and then only if they use "L" or "LS" TTL to connect to the bus. For greater expansion capability, a "bus expansion motherboard" can be used. This contains the typical parallel lines and board connectors as well as TTL buffers to drive a large number of boards. One of these in effect converts the KIM-1 bus to an S-100 bus and allows all of the less sophisticated S-100 boards to be used with a KIM-1 system.

General Purpose Interface Bus (GPIB). All of the bus systems discussed so far have been *processor* busses. That is, they connect both memory and I/O boards to the CPU. Although they are very fast and relatively simple to interface to, operational speed restricts the overall length to two feet or less. Running the parallel lines over a longer distance than this produces intolerable noise and crosstalk as well as a general slowdown of all signals. What this means is that all interface boards *must* plug directly into the bus in the computer cabinet. Since input/output is usually done much more slowly than memory access, it would be nice to have a parallel I/O bus that can be run through a cable to a variety of peripheral devices.

One bus designed for just this purpose is the General Purpose Interface Bus (GPIB), developed by Hewlett-Packard and adopted as a standard by the IEEE. The bus consists of 16 lines, 8 of which are bidirectional data/address lines and 8 of which are control lines. Although slower than the typical processor bus, it is much faster than a serial interface and uses full "handshake" control signal exchange to prevent data loss in the event a peripheral device is unable to receive data. Data transfers over the bus are in the form of 8-bit bytes and the control signals insure that devices on the bus are ready to receive or send data. Maximum bus length is about 16 feet, long enough to interconnect a table full of microcomputer peripherals. A maximum of 14 different devices can be addressed.

The significance of the GPIB is that the recently announced PET computer from Commodore has a GPIB connector on the back. Their plans call for interfacing add-on peripherals through this connector rather than adding boards inside the computer itself. Because of the large market expected for the PET computer and the fact that it is a formal industry standard not dominated by a single manufacturer, it is likely that the GPIB will soon become the preferred standard method of interfacing peripheral devices to a microcomputer. The familiar motherboard bus may disappear as 16k and 64k RAM chips make their appearance.◇