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PE Compares Audio "Click & Pop" Suppressors

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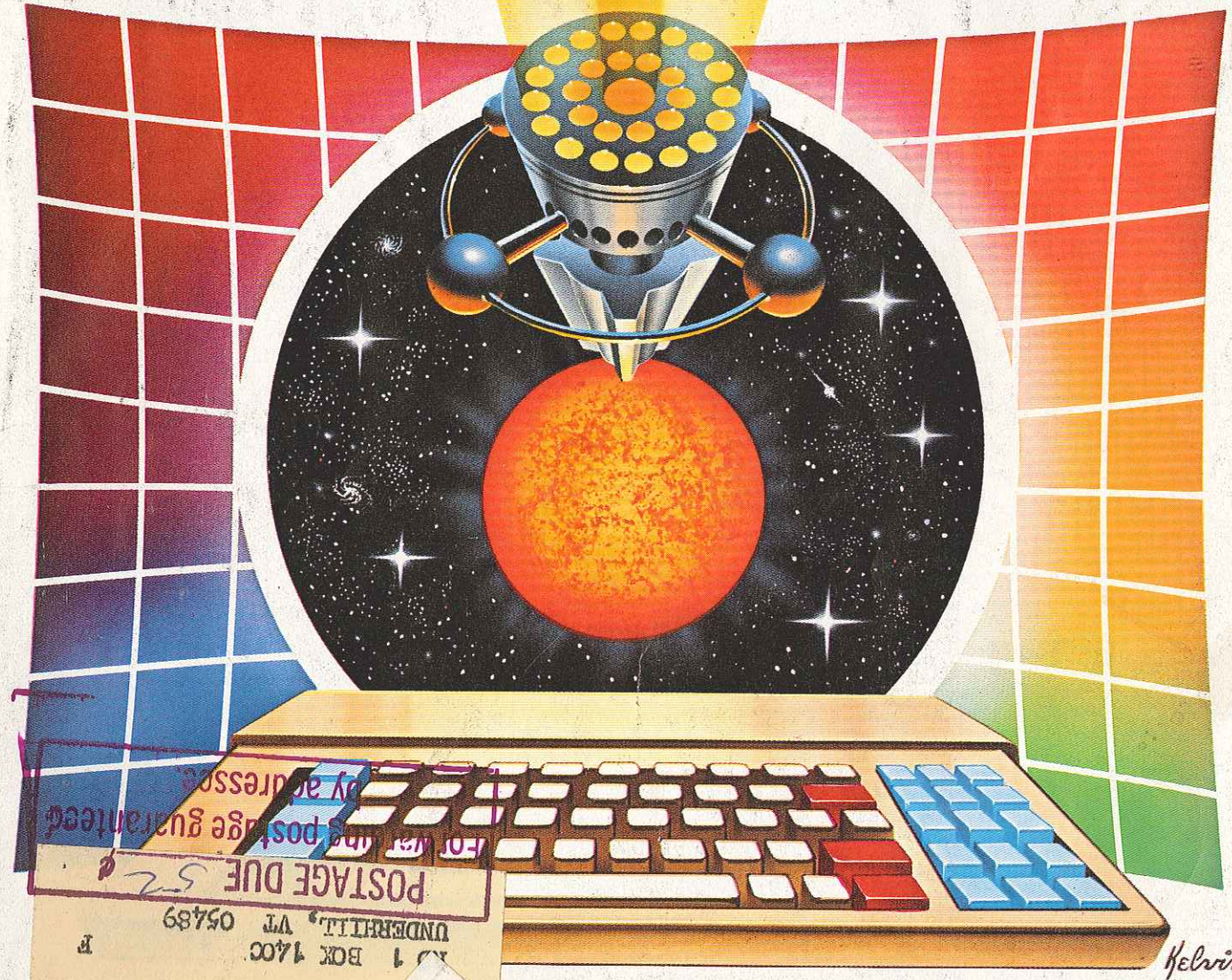
Special Focus On Personal Computers

"CORONA" 256-COLOR PERIPHERAL + TIC-TAC-TOE PROGRAM

8085 SINGLE-BOARD COMPUTER + 16 BIT Vs. 8 BIT CPUs



xman R-1120 AM/FM Stereo Receiver

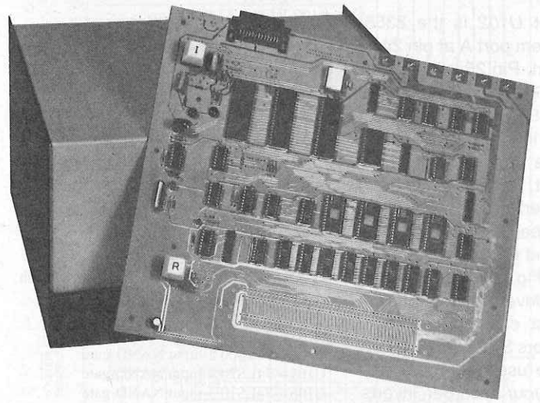
Pioneer CT-F900 Cassette Deck

Signet TK7E Stereo Phono Cartridge

POPULAR ELECTRONICS NOVEMBER 1978

SPECIAL FOCUS ON computers

This special editorial section crams into more than 18 pages a host of personal computer articles that illustrate the field's continued vigor. It includes a new low-cost microcomputer project that employs the advanced 8085 CPU, a look at an upcoming peripheral that will put all the colors of the rainbow—and then some—into the hands of computer users, an auxiliary-device project for the popular TRS-80 to make cassette program retrieval easier, a discussion about the new 16-bit CPUs and how they compare to the presently dominant 8 bitters, and how to care for and handle floppy diskettes.



CONSTRUCTION PROJECT

"EXPLORER" 8085-Based Microcomputer

Expandable, single-board $130 computer uses simplified hardware and is fully compatible with 8080 software

BY MARTIN MEYER

IT IS no secret that hundreds of thousands of programs have been written for 8080-based microcomputers. While the 8080 is an excellent microprocessor, it requires 30 support ICs and has a rather complicated system architecture. Consequently, users generally do not understand how the μP works and are, therefore, relegated to being "appliance" operators and slaves of packaged software. The new Intel 8085 μP, which is 100% software-compatible (though not pin-compatible) with the 8080A, simplifies hardware and software matters considerably because it requires only three support ICs. Without a maze of flip-flops to fight through and with eight fewer connections and bus lines for every chip added, you need no longer be confused about μP operation with the 8085.

In addition to using "canned" programs, one can learn the rudiments of machine language more easily with the 8085 than its 8080 predecessor. Hence, program debugging is simplified so that exchanged programs that are slightly askew from your BASIC can be corrected and modified. Also, programs published in magazines and other literature can be made to work with your computer. Once you learn machine language with the 8085, you will no longer be a prisoner of canned software. This means that you will not have to search out software to instruct your computer to do a myriad of simple dedicated tasks. You will be able to program it yourself to, say, turn on and off a light with a specified delay, act as an alarm system or telephone dialer, etc.—all without expensive RAM or ROM or any special expertise.

The minimum-system 8085-based "Explorer" microcomputer presented

here has a host of other welcome attributes, including: built-in ROM monitor; 50% faster speed than the 8080A; S-100 bus compatibility; single 5-volt supply requirement; four *built-in* hardware and seven software interrupts; and multiplexed data/address lines. A basic starter kit with full on-board expansion capabilities (see Minimum System Parts List) allows one to grow at his own pace. System peripherals designed to work directly with the 8085 already include interval timers, DMA and interrupt controls, programmable floppy-disk and CRT controllers.

The Minimum System. The basic Minimum Explorer T-8085 computer system described here is built around just eight ICs, the most important of which is the 8085 μP. Direct support of the 8085 is provided by an 8355 ROM and an 8155 RAM. The ROM contains a 2K monitor and two programmable 8-bit bidirectional parallel I/O ports (see table for commands contained in the ROM). The RAM contains two programmable 8-bit bidirectional and one programmable 6-bit bidirectional I/O ports and a programmable 14-bit binary counter/timer. The remaining five chips include operational amplifiers, inverters, and gates.

Bear in mind in the following circuit descriptions that all components with 100-series part numbers (*C101, R115, U101,* etc.) comprise the basic minimum system. Components labelled with 200-series numbers are required for S-100 bus expansion, 300-series components are for on-board RAM and ROM expansion, and 400-series components are for a hex keypad.

The 8085 (*U101* in Fig. 1) utilizes a multiplexed address/data bus (pins 12 through 19). The lower eight bits of the address output is followed by eight bits of data or I/O. ALE pin 30 synchronizes the accessory chips in the system, which latch in first the address and then the eight bits of data. This greatly simplifies the system and use of the I/O ports and is largely responsible for its compactness and the saving of up to eight pins per add-on chip. High-order bus pins 21 through 28 contain the high-order address signals.

Transistors *Q101, Q102,* and *Q103* are serial-output buffers and are selectable via *S9* and *S10* to be either a 20-mA TTY or an RS232-C interface. (A negative supply is required to drive an RS232-C device.) The collector circuit of *Q102* also includes light-emitting diode *L100* and an output for a speaker or a headphone. The LED is useful for signalling the end of a program or event. (For example, the last statement in a program could be an instruction to turn on the LED after the program has been successfully executed.) The headphone or speaker is useful for monitoring music and audio programs.

Integrated circuits *U104A, U104B, U105,* and *U106A* are address decoders that specify the address of the system's ROM at F800 and RAM at F000. IC's *U104C U104D,* and *U106B* are part of the auto-boot that automatically points the system to the monitor on turn-on and when pressing the monitor switch. IC *U106C* is a memory-ready control that is employed only when using memories that are slower than the speed of the 8085.

Integrated circuit *U102* is the 8355 system ROM. System port A at pin 24 is the tape-output port. Pin 25 is the tape-control port. Pin 26 is the cassette-tape output port. The 8155 *U103* RAM is used to take data in and pass it out of the computer to a variety of different types of equipment. The 8155 also contains a 14-bit counter/timer.

Cassette tape operation is controlled by *U108, Q104,* and reed relay *K1.* (For more details, see Fig. 2.) The tape output is designed to drive a microphone input on a low-cost cassette recorder. Tape phase selectors *S11A* and *S11B* in Fig. 2C permit the use of virtually any tape recorder. If your recorder inverts the signal during record, a condition that might cause loading errors, simply install a jumper for *S11B.*

Reed relay *K1* in Fig. 2B closes whenever you write or read a tape program and automatically turns off the tape recorder when the information being written or read is completed. ICs *U209* and *U210* are bidirectional data bus drivers, while *U214* is used for on-board memory acknowledge, which turns off the S-100 data bus when either the on-board RAM/PROM or monitor is in use. Jack *J2* is the hex keypad output jack. (The 200-series components mentioned here are *not* part of the basic system.)

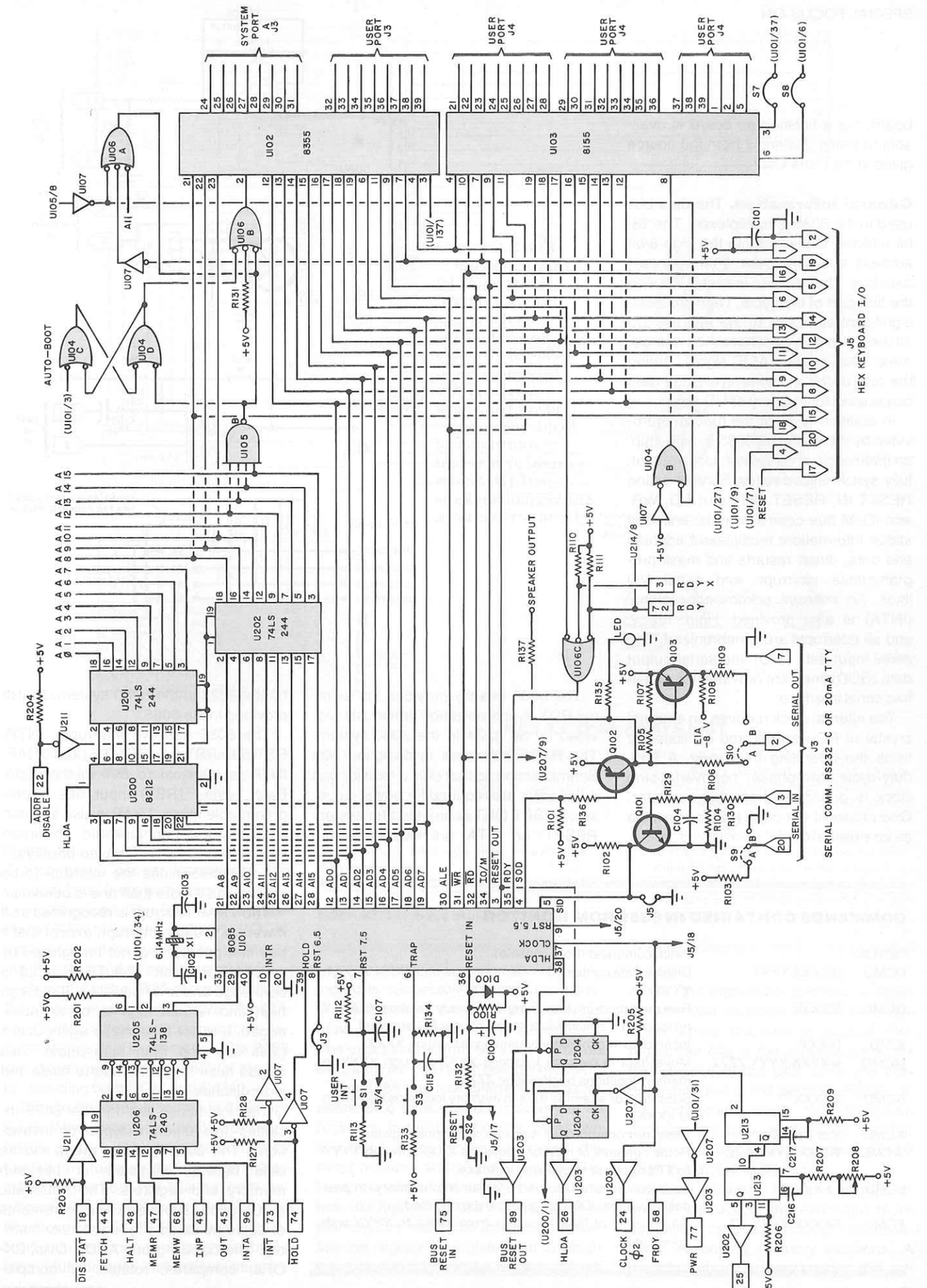
Due to the complexity of the double-sided pc board, which includes expansion provisions, its etching and drilling guide is not given here. Since the basic system actually consists of so few parts, they can be direct-wired on perforated

Fig. 1. Schematic of the basic Minimum Explorer T-8085 computer system is shown on the opposite page. The Parts List is below. The system is built around eight ICs, the most important of which is the 8085.

MINIMUM SYSTEM PARTS LIST

C100—1-μF, 35-volt tantalum capacitor
C101—25-μF, 25-volt upright electrolytic capacitor
C102,C103—18-pF disc capacitor
C104,C107,C115—0.1-μF disc capacitor
C105—0.0047-μF Mylar capacitor
C106—0.47-μF Mylar capacitor
C108 through C114—0.01-μF disc capacitor
D100,D101—1N4148 switching diode
K1—Spst reed relay
LED100—Red light-emitting diode
Q101,Q104—2N4384 transistor
Q102,Q103—2N4355 transistor
The following resistors are ¼-watt, 5% tolerance:
R100,R134—47,000 ohms
R101,R110,R111,R115,R119,R123,R124 through R128, R131—10,000 ohms
R102—2200 ohms
R103,R135—390 ohms
R104,R105,R107,R108,R109,R116,R118, R129,R132—1000 ohms
R106,R117,R133,R137—100 ohms
R112—39,000 ohms
R113—200 ohms
R114—100,000 ohms
R120,R121—1 megohm
R122—22,000 ohms
R130,R136—3900 ohms
S1,S2,S3—Spst momentary-action keyswitch
U101—8085A CPU
U102—8355 I/O ROM (see text)
U103—8155 RAM I/O-timer
U104—74LS00 2-input NAND-gate
U105—74LS20 4-input NAND-gate
U106—74LS10 3-input NAND-gate
U107—74LS04 hex-inverter
U108—LM3900 quad op-amp
X100—6.14-MHz crystal
Misc.—Printed-circuit board; sockets for IC's (three 40-pin, five 14-pin); rubber feet (8); solder; etc.

Note: The following items are available from Netronics R&D Ltd., 333 Litchfield Rd., New Milford, CT 06776: Complete 8085 minimum system Explorer microcomputer kit, including IC sockets (No. 8085EIA for EIA terminals or No. 8085HEX for hex keypad systems) for $129.95 plus $3.00 postage and handling. The double-sided, plated-through hole pc board No. 8085PC is also available separately for $49.95 plus $2.00 postage and handling. Additional equipment not part of minimum system includes: No. PS5VR 5-volt regulated power supply for $39.95 plus $2.00 postage and handling; Explorer case for $39.95 plus $3.00 postage and handling; hex keypad kit (see Hex Keypad Parts List) for $69.95 plus $2.00 postage and handling; Intel 8085 User's Manual for $7.50 ppd.



board; but a finished pc board is available to those desiring it from the source given in the Parts List.

General Information. The data bus used in the 8085 is multiplexed. The 16-bit address is divided into the high 8-bit address bus and lower 8-bit address/data bus. The address is sent out during the first part of the cycle. Then the least-significant eight bits of the address are latched into the peripherals by the address latch enable (ALE) signal. During the rest of the machine cycle, the data bus is used for memory or I/O data.

In addition to all of the functions provided by the 8080, the 8085 has on-chip: an internal clock generator; clock output; fully synchronized ready; Schmitt-action RESET IN; RESET OUT pin; RD, WR, and IO/M bus control signals; encoded status information; multiplexed address and data; direct restarts and mask-programmable interrupt; and serial I/O lines. An interrupt acknowledge signal (INTA) is also provided. Hold, ready, and all interrupts are synchronized. The serial input data (SID) and serial output data (SOD) lines are provided for simplified serial interface.

The internal clock requires an external crystal or RC network and oscillates at twice the operating frequency. A 50% duty-cycle, two-phase, nonoverlapping clock is generated from this oscillator. One phase of the clock ($\phi 2$) is available as an external clock.

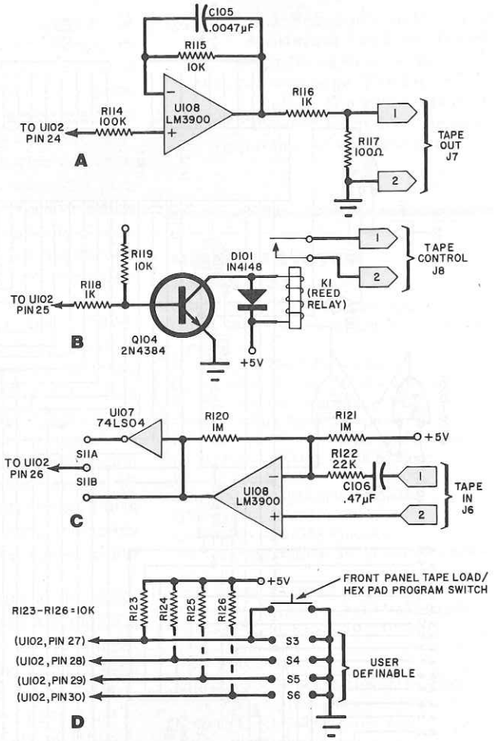


Fig. 2. Cassette tape operation is controlled by circuits shown. (A) Amplifies signal for tape deck. (B) Controls tape movement. (C) Amplifies output from deck to microcomputer and choice of normal or inverted signal. (D) Shows hex keypad hookups for tape functions.

The 8085 directly provides the external RDY synchronization previously provided by an 8224 in the 8080 system. The RESET IN input is designed with Schmitt action so that only a resistor and a capacitor are required for power-on reset. RESET OUT is provided for system RESET. An INTA, previously provided by the 8224 in the 8080 system, is also provided in the 8085.

The 8085 has five interrupts: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical to INT in the 8080. Each restart (RST) input has a programmable mask. TRAP is also a restart input, but it is nonmaskable. The interrupts are arranged in a fixed priority order that determines the interrupt to be recognized if more than one is pending.

The TRAP interrupt is recognized as if it were any other interrupt, except that it has first priority. It is not recognized by any flag or mask. The TRAP input is both edge and level sensitive. It must go high and remain high to be acknowledged. It is not recognized again until it goes low and then high again. This avoids false triggering due to noise and logic glitches.

The instruction set for the 8085 includes five different types of instructions. The Data Transfer group moves data between registers or between memory and registers. The Arithmetic group adds, subtracts, and increments or decrements data in registers or memory. The Logical group ANDs, ORs, EX-ORs, compares, rotates, or complements data in registers or memory. The Branch group permits conditional and unconditional jump instructions, and return instructions. The Stack I/O and Machine Control group includes I/O instructions and instructions for maintaining the stack and internal control flags.

COMMANDS CONTAINED IN 8355 ROM MONITOR

GETCM		Fetch command (from console).
DCMD	DXXXX,YYYY	Display data contained in memory locations XXXX through YYYY.
GCMD	GXXXX	Run user program beginning at memory location XXXX. If no location is specified, contents of user PC are used.
ICMD	IXXXX	Insert data into memory beginning at location XXXX.
MCMD	MXXXX,YYYY,ZZZZ	Move data in memory locations XXXX through YYYY to memory locations beginning at ZZZZ.
SCMD	SXXXX	Substitute or examine data in memory locations beginning at XXXX.
XCMD	X or X(REG)	Examine contents of all registers or just one register.
WCMD	WXXXX,YYYY,ZZ	Route contents of memory locations XXXX through YYYY to TTY punch or to cassette interface.
LCMD	LXX	Load contents of recorded program into memory. In cassette systems, XXth program can be selected.
FCMD	FXXXX,YYYY,ZZ	Fill contents of RAM locations from XXXX to YYYY with constant ZZ.

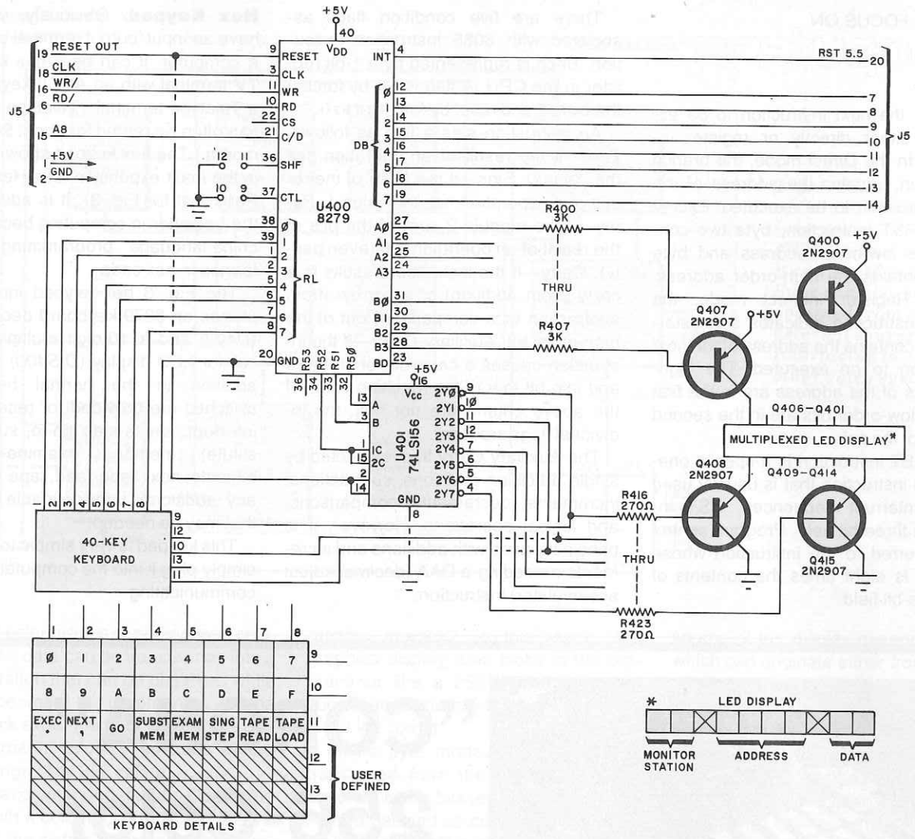


Fig. 3. Hex keypad terminal for use with Explorer computer.

HEX KEYPAD PARTS LIST

DIS1—Eight-digit multiplexed calculator LED display array
Q400 through Q415—2N2907 or equivalent transistor
R400 through R407—3000-ohm, ¼-watt, 5% tolerance resistor
R408 through R415—24-ohm, ¼-watt, 5% tolerance resistor
R416 through R423—270-ohm, ¼-watt, 5% tolerance resistor
U400—8279 keyboard decoder IC
U401—74LS156 3-to-8 decoder IC
Misc.—40-key keyboard assembly; 16-conductor cable to mother board; printed circuit board; sockets for ICs (one each 40 pin and 16 pin); solder; etc.
Note: A complete kit of the above parts is available from the source given in the Minimum System Parts List. When a keypad is ordered with a Minimum System the latter will have an 8355 ROM programmed to talk to the keypad.

Memory for the 8085 is organized into 8-bit bytes, each with a unique 16-bit binary address that corresponds to its sequential position in memory. (The 8085 can directly address up to 65K of memory, including both ROM and RAM.)

Data in the 8085 is stored in 8-bit registers. When a register or data word contains a binary number, the order in which the bits are to be written must be established. In the 8085, bit 0 is the least-significant bit (LSB), while bit 7 is the most-significant bit (MSB). Program instructions can be one, two, or three bytes long. Multiple-byte instructions must be stored in successive memory locations. The address of the first byte is always used as the address of the instructions. The exact instruction format depends on the particular operation being executed.

The 8085 has four different modes for addressing data stored in memory or its registers. In the Direct mode, bytes two and three of the instruction contain the exact memory address of the data. The low-order bits of the address are in byte two, the high-order bits in byte three. In the Register mode, the instruction specifies the register or register-pair in which the data is located. In the Register Direct mode, the instruction specifies a register-pair that contains the memory address where the data is located. The high-order bits of the address are in the first register of the pair, while the low-order bits are in the second register. In the Immediate mode, the instruction contains the data itself, which is either an 8- or a 16-bit quantity. The LSB bit goes in first, the MSB last.

Unless directed by an interrupt or branch instruction, the execution of instructions proceeds through consecutively increasing memory locations. A branch instruction can specify the ad-

dress of the next instruction to be executed, either directly or register indirectly. In the Direct mode, the branch instruction contains the address of the next instruction to be executed. Except for the RST instruction, byte two contains the low-order address and byte three contains the high-order address. In the Register Indirect mode, the branch instruction indicates a register-pair that contains the address of the next instruction to be executed. The high-order bits of the address are in the first and the low-order bits are in the second register of the pair.

The RST instruction is a special one-byte call instruction that is usually used during interrupt sequences. RST includes a three-bit field. Program control is transferred to the instruction whose address is eight times the contents of this three-bit field.

There are five condition flags associated with 8085 instruction execution. Each is represented by a 1-bit register in the CPU. A flag is set by forcing the bit to 1 and reset by forcing it to 0.

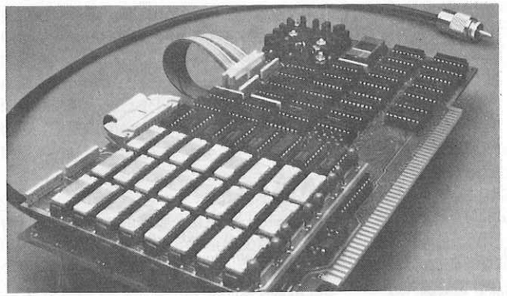
An instruction sets a flag as follows: Zero—if the result of an operation has the value 0: Sign—if the MSB of the result of an operation has the value 1; Parity—if the modulo 2 sum of the bits of the result of an operation is 0 (even parity); Carry—if the instruction results in a carry (from addition) or a borrow (from subtraction or a comparison) out of the high-order bit; Auxiliary Carry—if the instruction causes a carry out of bit three and into bit four of the resulting value. If the above criteria are not met, the individual flags are reset.

The Auxiliary Carry flag is affected by single precision additions, subtractions, increments, decrements, comparisons, and logical operations. However, it is principally used with additions and increments preceding a DAA (decimal adjust accumulator) instruction.

Hex Keypad. Obviously, you must have an input/output terminal to operate a computer. It can be a hex keypad, a TV terminal with an ASCII keyboard, or a Teletype terminal. (Teletype terminals can often be rented for about $40.00 per month.) The hex keypad shown in Fig. 3 is the least expensive (see Hex Keypad Parts List for Fig. 3). It is adequate for the beginner in computing because machine-language programming is performed in hex code.

The Fig. 3 hex keypad input circuit utilizes an 8279 keyboard decoder chip (*U400*) and a 10-digit multiplexed calculator LED display (*DIS400*) output. In addition to the normal hex input, switches are provided for reset, vector-interrupt, single-step go-to, subst (substitute) memory, examine-registers, execute, next, tape-read, tape-load, plus any additional user-definable functions that may be needed.

This keypad is very simple to use. You simply plug it into the computer and start communicating. ◇



"CORONA" 256-Color Peripheral

BY JEFF LOWENSON, ROBERT MARSH & JAMES SPANN

Upcoming S-100 bus compatible kit with full color graphics and alphanumerics.

EDITORS AT POPULAR ELECTRONICS are frequently privy to exciting new products that are in the final stages of pre-production design. This information includes all the details on how it works and "hands on" experience with custom-wired samples. One such product about which we'd like to share information with readers is Processor Technology's "Corona," a high-resolution, full-color graphics accessory for microcomputers. The Corona will provide 256 colors (or shades of grey in a 256-by-208 display with graphics and alphanumerics mixed—all under software control.

Note: on the cover is an artist's conception of a computer game using the Corona.

The Corona is designed to be fully bus compatible with the SOL-20 microcomputer and VDM-1 video display module, both made by Processor Technology. However, it can be modified as required to operate with other S-100 bus formats. The Corona-1K kit with 8K of memory will be marketed through computer stores in the near future for $395.

Technical Details. The display resolution of the Corona is 256 × 256, with a display size of 256 horizontal by 208 vertical. Its 53,248 pixels can be used with a selection of any 16 out of 256 possible colors (or grey levels). The alphnamerics can be mixed and overlaid with the graphics and/or external video input. The Corona uses 8K of 8-bit bytes in the low-color range and 24K of 8-bit bytes in the full-range version. (See Corona Specifications Table.)

In addition to game playing, this new graphics system is a powerful tool for business, artistic, scientific, and educational applications, since vivid graphics, poster-like displays, and full-color animation are available.

Since the Corona's signals can be mixed with video from a low-cost monochrome TV camera and with alphanumerics from a computer, the final video can display a scene from a camera with

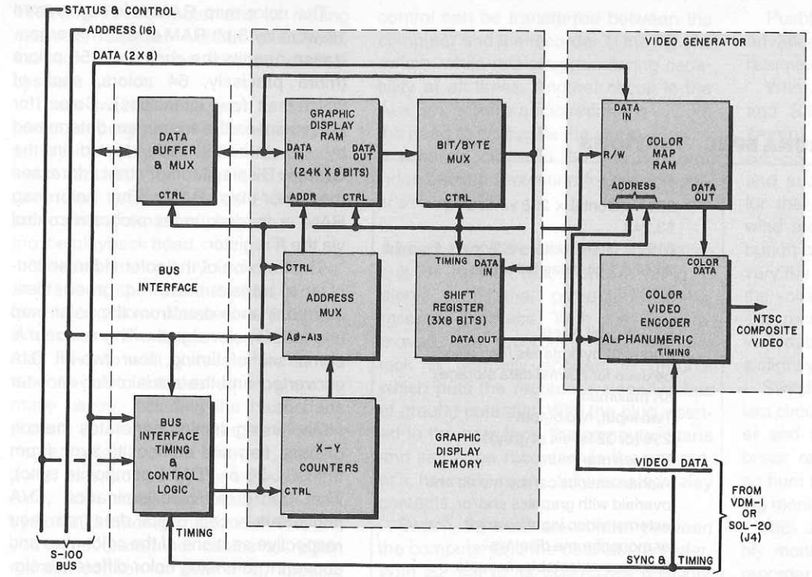


Fig. 1. Block diagram of Corona shows logic interconnections. The NTSC output means that it can be video recorded. Sync can also be obtained from an external source for interfacing to other video systems.

a set of color graphs superimposed on it. Scientific data can be transformed into a presentation that can be observed while an experiment is in progress. Alpha feedback experimenters will find this color approach valuable because of the wide range of its 256 colors.

It is recommended that the Corona be used with a color monitor to take advantage of the better color and crisper images available.

Circuit Operation. As shown in Fig. 1, the heart of the Corona system is the Graphic Display Memory that stores information in three 256 × 256 × 1 bit planes, each of which represents a 256 × 256 CRT screen matrix. The three combined planes contain three bits of color information for each dot on the TV screen. The memory can be used in two ways—for color-picture storage or as conventional computer memory. This means that when the graphics are not used, the computer's memory is expanded by the amount of memory contained in the graphics interface (see Fig. 2 memory map).

Memory access by the computer is handled in two modes. In the *bit* mode, each full-color point can be individually read or written to by the computer. This mode simplifies interfacing with BASIC and FORTRAN to take advantage of their powerful trigonometric and matrix functions. (Matrix operations enable the programmer to write powerful software for scaling, translation, and rotation of graphic images.) In this mode, the graphics display area looks to the programmer like a 256 × 256 Cartesian coordinate system, with the origin at the lower left corner.

In the *byte* mode, graphics data is transferred from the computer to the Corona, eight bits at a time, with the RAM organized as conventional 24K by 8-bit memory. The byte mode permits very fast loading of complete screens from peripheral devices, such as a flop py-disk or a cassette-tape system.

The bus interface and control logic section (Fig. 1) controls the flow of data between the computer and the Graphics Display Memory. This logic synchronizes the TV scan and computer memory requests. This functional block also contains the command registers, memory timing, and fast erase logic.

The address multiplexer selects the source of the display memory address, which can originate either from the computer or from the X-Y logic. The X-Y counters generate the X-Y address coordinates that represent a point on the CRT screen. Data from the display memory is thus mapped on the TV.

MEMORY MAP

FFFF	CORONA MEMORY
E000	NOT USED
D000	SOL/VDM-1 MEMORY
C000	PTDOS
8000	USER MEMORY SPACE
0000	

Fig. 2. Memory map shows RAM arrangement of Corona.

The bit/byte multiplexer is used in the bit mode to change or read one bit into each of the three memory planes. The shift registers convert the eight and 24 bits of parallel data from the Graphics Display Memory into a serial address for the color-map RAM.

The video generator section can provide up to 256 different colors (or 32 shades of grey), eight of which can be displayed graphically at one time. Either SOL-20 or VDM-1 alphanumeric characters can be mixed under program control to interleave graphics and text information anywhere desired on the screen. All the video sync signals are provided by the SOL-20 or VDM-1.

Alphanumerics can be displayed in a distinct ninth color that is selected under software control to provide the best contrast with the eight graphics colors. There are also an additional eight colors where the graphics and alphanumerics intersect.

Any one or all of the displayed colors can be rapidly changed without rewriting the graphics memory contents (that is, without changing the form or shape of the picture). This unique feature can create a shimmering rainbow effect with very simple programming.