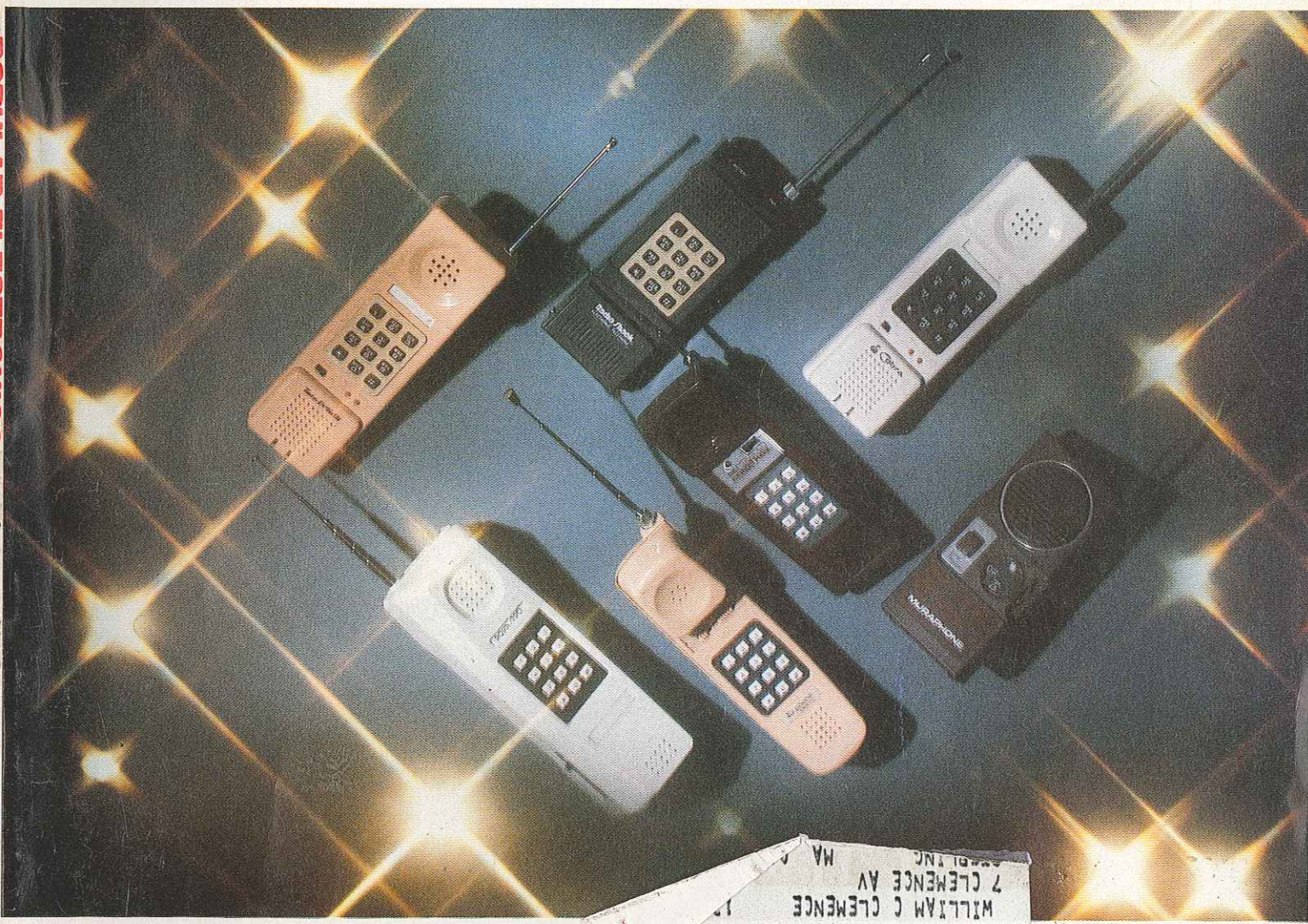


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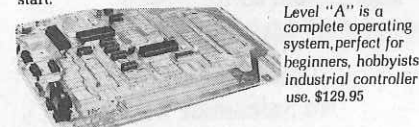
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System Monitor (Hex Keypad/Display Version): Tape load with labeling... tape dump with labeling... examine/change contents of memory... insert data... warm start... examine and change all registers...



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Level "A" With Hex Keypad/Display.

single step with register display at each break point... go to execution address. Level "A" in this version makes a perfect controller for industrial applications, and is programmed using the Netronics Hex Keypad/Display. It is low cost, perfect for beginners.

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Explorer/85 With Level "C" Card Cage.

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- LSI controller.
- Single or double density.

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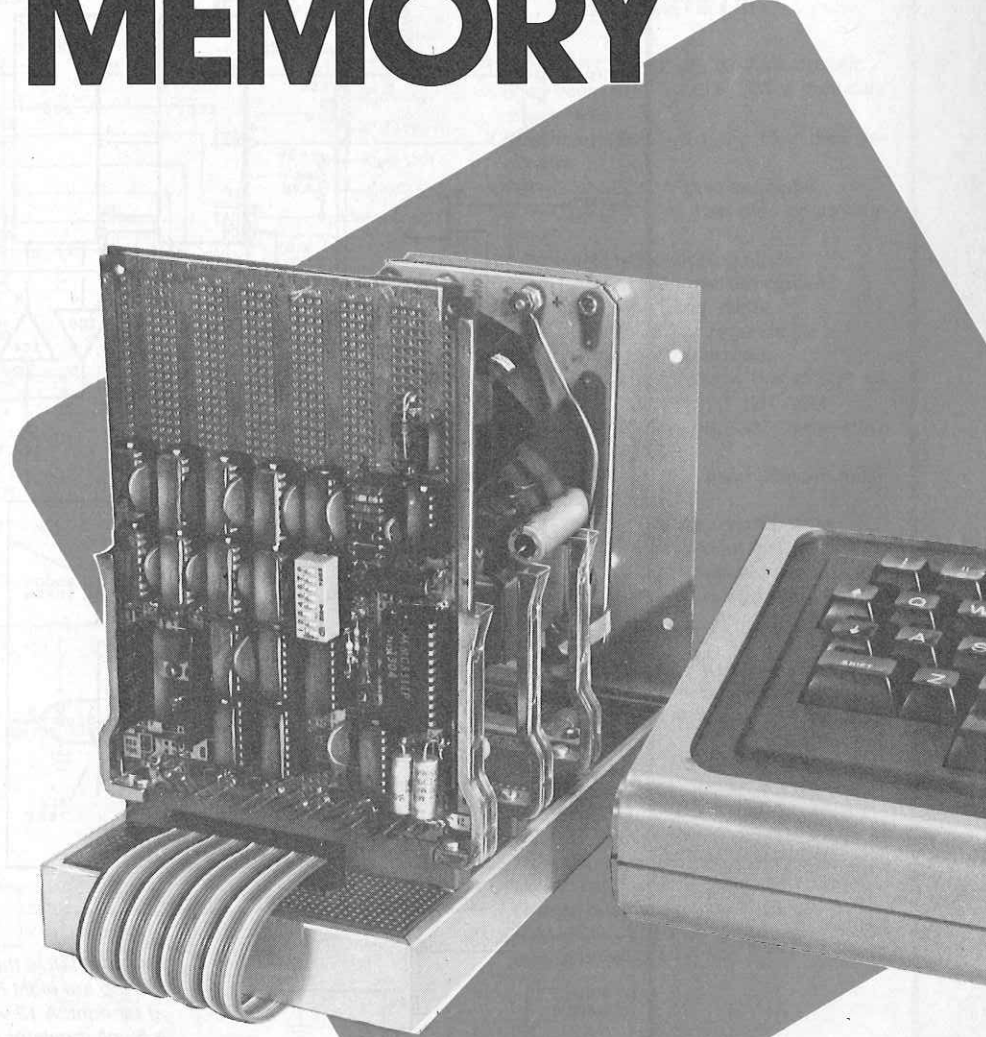
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PLUG-BOARD SYSTEM FOR ADDING 16K OF DYNAMIC RAM WITH A 4K BONUS

BY ADOLPH A. MANGIERI

AN INEXPENSIVE EXPANSION OF TRS-80 MEMORY



A MICROCOMPUTER with 4K of RAM (random access memory) can perform reasonably well, but its small memory locks it out of using much sophisticated software. In most systems, memory can be expanded by installing memory chip sets or plug-in memory boards. However, in the particular case of the Radio Shack TRS-80, installation of a RAM chip set leaves 16K inside the machine and 4K of removed RAM unused. Actually, this can be a bonus if you build the memory board and expansion interface described in this article.

The modification detailed here provides a total of 20K of RAM and a plug-board system that allows experiments with I/O ports. The memory board features a universal address decoder that allows placing the RAM on any 4K boundary. If you program in machine language using the TRS-80 TBUG monitor, you can switch the memory block to the remote end of memory where the small utility program really belongs. Also, the board is easily converted to accept 16K RAMs if desired.

The simplicity of memory upgrade from 4K to 16K is the direct result of the use of 16-pin RAM chips. These multiplexed-address input dynamic RAMs are in wide application because of their low cost and power consumption. The latest additions to this family of devices provide up to 64K bytes with eight memory chips.

Memory Basics. The Z80 microprocessor distinguishes memory access machine cycles by concurrently issuing a 16-bit memory address and memory request (MREQ), along with either a read (RD) or write (WR) pulse. These and other control signals operate the memory blocks of a computer. A typical memory chip includes address input, write, chip-select (or chip-enable), and data input and output lines.

Computer memory consists of a number of memory blocks arranged in sequence. A memory block may consist of one 1K x 8 read-only memory (ROM), two 1K x 4 RAMs, or eight 16K x 1 RAMs, to name a few of the possible configurations. Whatever the chip size, the storage elements of the device are arranged in a matrix. For example, the storage matrix of the 4027 (4K x 1) chip consists of 64 rows by 64 columns, yielding 4096 bits. A memory element within the matrix is selected by matrix row and column decoders. For a 4K x 1 memory chip, the address decode range is from 000 (zero) to FFF hexadecimal or 4096 decimal.

To allow stacking memory blocks end-to-end, an external memory address decoder is required. The address decoder continuously scans the higher-order computer address lines and exclusively

selects one memory block at a time, depending on the address from the CPU.

The block and timing diagram shown in Fig. 1 illustrates the operational arrangement of a 4027 4K multiplexed dynamic memory. The 4027 accepts 12 address line bits (A0 through A11) in two groups through multiplexer switches consisting of six single-pole double-throw semiconductor switches controlled by the MUX (multiplexer control) pulse. The chip data-out and data-in lines are buffered by three-state gate G3, which is controlled by gate G2 and by data-in buffer G4. The input to the address decoder consists of high-order address lines A12 through A15.

Prior to appearance of the RAS, (row address select) pulse, the address decoder is disabled and its output is high. Since gate G2 is inactive at this time, gate G3 is also off. In addition, chip select line CS is high, with memory de-

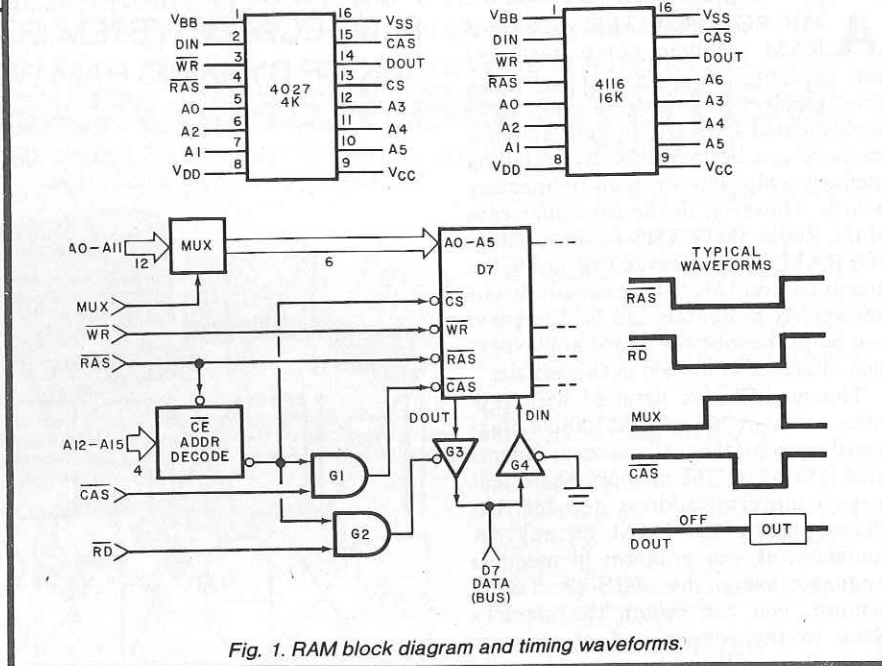


Fig. 1. RAM block diagram and timing waveforms.

selected, gate G1 inactive, and the chip data-out line off. The MUX pulse is low and allows bits A0 through A5 to pass through the MUX switch to the chip's address input pins. On a memory read RD machine cycle, the CPU places a 16-bit address on the system bus, along with MREQ and RD pulses. (Incidentally, RAS is simply a renaming of the MREQ CPU pulse.) When RAS appears, the address decoder is enabled and its decoded output goes low, enabling memory. Also, one input pin of G1 and G2 goes low, allowing read pulse RD to pass through G2 and turn on G3, but the chip is not yet ready to output data. The RAS pulse also strobes bits A0 through A5 into the chip address latches for temporary storage. The MUX pulse next appears and "throws" the multiplexer switches allowing address bits A6 through A11 to pass. Shortly thereafter, the CAS (column address strobe) pulse appears and

strokes the second group of address bits into the chip.

With the full address now entered, the matrix row and column address decoders decode the address and select the stored data cell. At this point, the chip data-out line becomes active and passes the data bit to the system bus through G3. The RAS pulse goes high with chip deselection, and G3 cuts off.

Action is similar on a memory write cycle. Write pulse WR appears, G3 is off throughout the cycle, and data enters the chip through G4. MUX and CAS pulses are not supplied by the CPU; rather, they are developed by other circuit logic and properly synchronized with CPU MREQ pulse. This logic is already present in the TRS-80, and MUX and CAS pulses are on the system's bus in this and most other Z80-based systems utilizing multiplexed-address input dynamic RAMs.

For the 4116 16K version, 14 address line bits are multiplexed to the chip. To make room for two additional address line bits, pin 13 of the 4116 is used to enter bits A6 and A12, sacrificing the chip-select line. Address bits A0 and A13 enter pin 5. Then, to account for the missing chip-select line, the 4116's logic senses the proper sequence and timing of the RAS, MUX, and CAS pulses before enabling the chip.

Memory Refresh. All memory locations of the dynamic RAM must be refreshed within a 2-ms interval to avoid loss of data. This occurs on any memory cycle of a running program. It can be accomplished via software, but this reduces processing speed. Memory refresh, therefore, is best accomplished by hardware.

Refresh circuits are essentially counters that generate sequential addresses

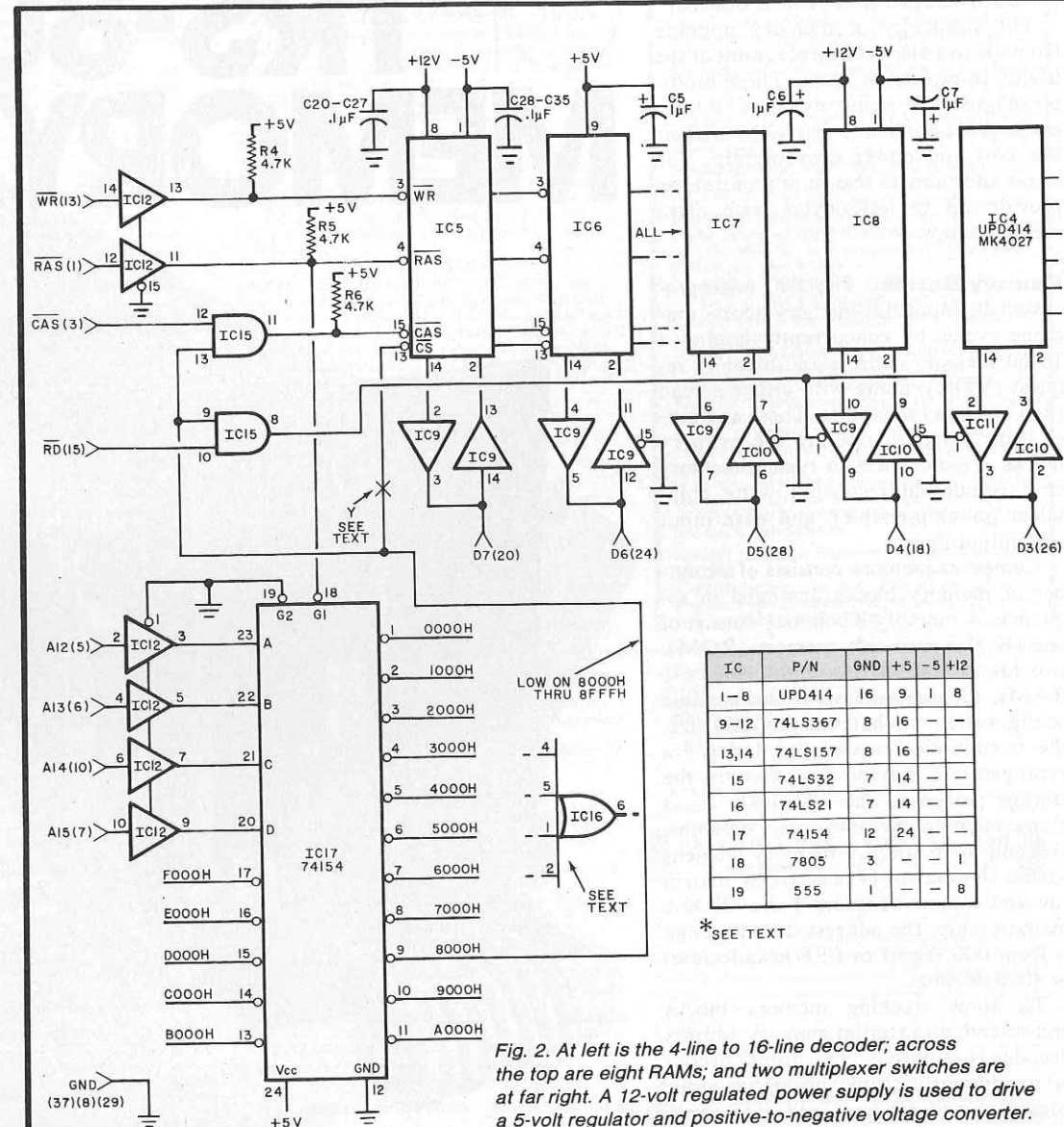
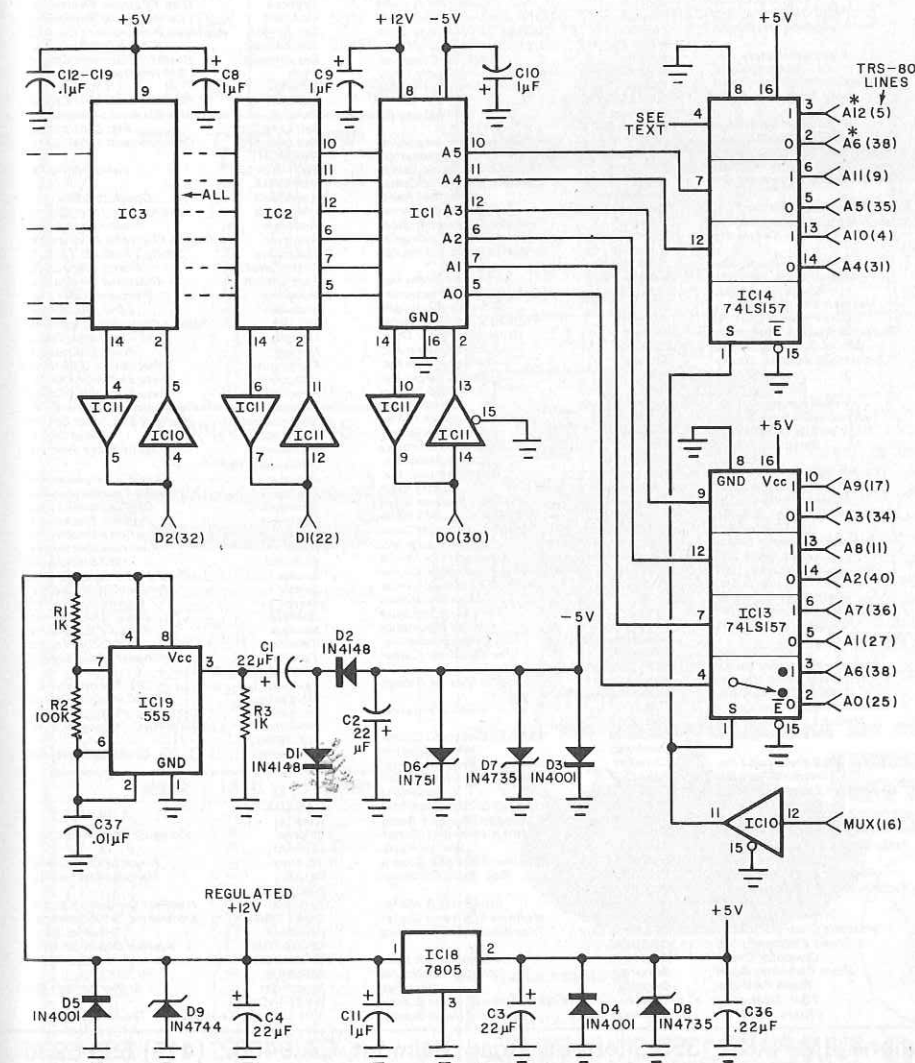


Fig. 2. At left is the 4-line to 16-line decoder; across the top are eight RAMs; and two multiplexer switches are at far right. A 12-volt regulated power supply is used to drive a 5-volt regulator and positive-to-negative voltage converter.



PARTS LIST

- C1 through C4—22-μF, 20-V electrolytic
- C5 through C11—1.0μF, 35-V tantalum electrolytic
- C12 through C35—0.1-μF, 15-V disc capacitor
- C36—0.22-μF, 15-V disc capacitor
- C37—0.01-μF, 15-V 10% disc or polystyrene
- D1,D2—1N4148 switching diode
- D3,D4, D5—1N4001 rectifier diode
- D6—1N751 5.1-V zener diode
- D7,D8—1N4735 6.2-V zener diode
- D9—1N4744 15-V zener diode
- IC1 through IC8—UPD414 (MK4027)* 4K or UPD416 (MK4116)** 16K RAM
- IC9 through IC12—74LS367 three-state hex buffer
- IC13,IC14—74LS157 quad 2-input multiplexer
- IC15—74LS32 quad 2-input OR gate
- IC16—74LS21 dual 2-input AND gate
- IC17—74154 4-to-16 line decoder
- IC18—7805 5-V, 1-A voltage regulator
- IC19—555 timer
- R1,R3—1-kΩ, 1/4-W 10% resistor
- R2—100-kΩ, 1/4-W 10% resistor
- R4,R5,R6—4.7-kΩ, 1/4-W 10% resistor
- *Use similar 4K RAMs on removal from TRS-80.
- **Use JAMECO TRS-16K kit for TRS-80 16K upgrade and for 4K to 16K board upgrade. See text.
- Misc.—IC sockets; wrap posts; 20/40 card edge connector; ribbon cable; plug board; card guides; chassis; card receptacles; heat sink; 12-volt power supply (JAMECO JE210 or similar); perforated board; hookup wire; etc.

that are applied to the chips. For dynamic memory devices, it is necessary only to apply all possible row address combinations to the chip to refresh all memory locations. This RAS-only refresh is achieved in less time, and since the MUX and CAS pulses are absent, the chip is not enabled.

The Z80 CPU includes built-in refresh circuits for RAS-only refresh of the chips, this refresh occurring in the latter part of the opcode instruction fetch cycle, which is a special memory access period. Furthermore, refresh occurs while the CPU is decoding the fetched instruction, effecting hidden refresh. (For complete details, refer to the Zilog Z80 Technical Reference Manual and device specification sheets.)

Circuit Operation. Referring to Fig. 2, address decoder IC17 is a 4-line to 16-line decoder that senses address lines A12 through A15. All decoder output lines at pins 1 through 11 and 13 through 17 are at a high logic level until RAS appears and enables the decoder through strobe line G1 at pin 18. At this time, one of the 16 output lines goes low exclusively, depending on the value of the four address input bits.

Assume that the CPU issues hexadecimal address 8000, the next address following the end of the TRS-80's resident 16K of memory. Address decoder IC17 "sees" 8 (binary 1000) at inputs D, C, B, and A in that order. The 8000 output at pin 9 goes low and remains low through address 8FFF. On the next higher address (9000), pin 10 goes low exclusively and remains low through address 9FFF, and so forth.

Notice that, in each step, the low-order address lines run through the range of 000 through FFF (4096 addresses). Hence, the decoder can exclusively select any one of 16 4K memory blocks over the total possible 64K of memory space. However, on-chip address decoders of a selected memory block decode only the address range of 000 through FFF while depending on the external address decoder to establish block location in memory space.

Multiplexer switches IC13 and IC14 are controlled by the MUX pulse through the S control lines of the devices. Referring to the symbolic spst switch shown on IC13, all "switches" are in position 0, with MUX resting low to allow address bits A0 through A5 to pass to the RAMs. When MUX goes high, all switches move to position 1 to pass bits A6 through A11 to the chips. The multiplexers also buffer the address lines.

The memory circuit is powered by a regulated 12-volt source that in turn, powers 5-volt regulator IC18. Supplying

a small bias current to the RAMs, the -5-volt source is obtained from a charge-pump circuit formed from IC19, a 555 timer that delivers a square wave to the charge-pump circuit connected to pin 3. Regulation of the charge pump's -5-volt dc output is provided by D6, while D3, D4, and D5 provide reverse voltage protection and D7, D8, and D9 give some over-voltage protection.

RAM Kit Installation. We used a modified version of the TRS-80 disassembly instructions that are included in the computer's Technical Reference Manual to access the 4K RAMs. The procedure is as follows: With bottom screws removed and computer in its normal operating position, remove the top to reveal the keyboard. Next, hinge the keyboard to a vertical position, taking care to avoid strain on the short ribbon cable, and remove the five rubber spacers to free the main board. Lower the keyboard to the table top and rest it on its keytops. In a similar manner, hinge the main board outward and place it on the inverted keyboard. Reverse the procedure to reassemble.

We used the Jameco TRS-16K RAM kit which contains eight UPD416 (MK4116) high-speed RAMs and instructions for installation. Since the chips are easily damaged by static electricity, we recommend that you connect an earth ground wire to the main board circuit, and connect yourself to earth ground through a 250,000-ohm resistor

and a wire running to a metallic wrist-watch strap. *Stay clear of ac lines and equipment!* Use a dot of fast-drying white paint to mark the pin-1 position of each DIP shunt and 4K RAM socket location.

Remove the somewhat fragile DIP shunts, and replace with substitutes, such as 16-pin DIP headers, jumper wired according to instructions supplied. The DIP shunts and RAMs extract with difficulty, so go easy. As you remove each RAM, push it into black conductive foam plastic. Then install the 16K RAMs, being sure to orient them properly in their sockets.

If you don't have a similar system, you can assemble the plug-board system shown in Fig. 3 as follows: Install three Vector No. R644-3 44-contact receptacles on 4 1/2" x 6" perforated board drilled as required. Bolt Vector No. BR27D card guides and receptacles to the board and slide the Wire-Wrapped assembly into the 51X-1 aluminum frame. The memory board operates off a regulated 12-volt power supply, which can be mounted on a vertical plate bolted to the frame as shown. (If you aren't planning to use a plug-board system at this time, assemble the circuit on a Vector No. 8802 Circbord that has etched buses on one side of the board, and slide the board horizontally into the aluminum frame.)

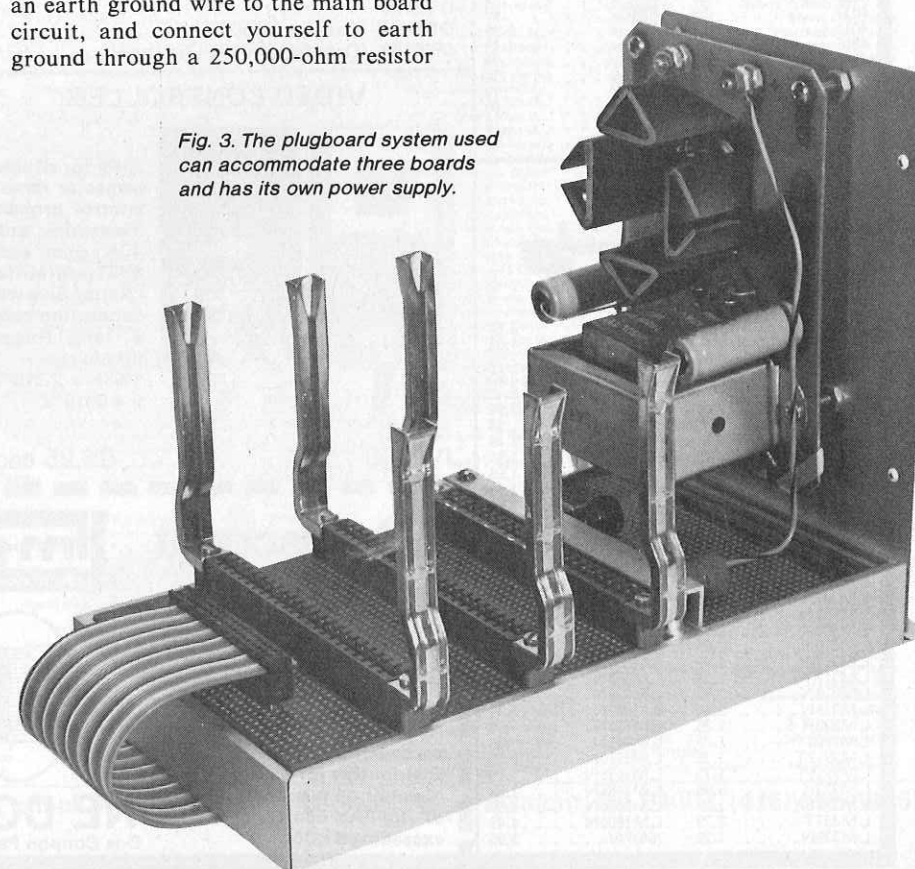


Fig. 3. The plugboard system used can accommodate three boards and has its own power supply.

Use only a short ribbon cable to interconnect the computer and expansion system. Connect a 6" length of 40-conductor ribbon cable to a TRS-80 card edge connector. For reduced crosstalk, overlay one side of the cable with aluminum foil. Then connect bare wire pig-tails to the connector's ground lugs and tape the pigtails to the foil. Omit any connection to TRS-80 5-volt line 39.

If you prefer a disconnect at the plug-board system, cut a preassembled 40-conductor female IDC ribbon cable to length and solder to the edge connector. Install two rows of No. T46-5-9 wrap posts into the perforated board with pin faces in square alignment to accept the female IDC plug.

The plug board shown is a Vector No. 4494 44-contact board with etched ground and supply planes on opposite sides. Assign the +12-volt supply to one of the spare bus lines. Install the sockets for the multiplexer and buffer ICs in the first two socket tiers near the card fingers and install the RAM sockets in the third and fourth socket tiers. This leaves ample room for another bank of eight memory devices. Do not install the ICs in their sockets until told to do so!

Charge-pump components can be installed on a DIP header and plugged into a single socket as shown. Install small bypass capacitors with minimum lead lengths. (In the prototype, some bypass capacitors were connected directly to socket-wrap posts.) The board is preferably chain-wrapped using the Vector No. P180 Slit-N-Wrap or similar tool. To keep crosstalk low, avoid bundling the wires.

When 20K of RAM isn't enough, you can easily install 16K RAMs on the expansion board to obtain a total of 32K of memory. To do this, first break the wire at point Y (see Fig. 2) to RAM pin line 13. Remove address line A6 from pin 3 of IC13 and connect address line A13 to pin 3 of IC13. Wire lines A6 and A12 to IC14 as shown, and connect pin 4 of IC14 to RAM pin line 13. Remove the connection from pin 9 of IC17 and wire it to pin 6 of IC16. Assuming there is 16K of RAM inside the TRS-80, connect the four input pins of active-low OR gate IC16 to pins 9, 10, 11, and 13 of IC17 in any order.

After checking your wiring for errors and shorts, install only IC19, apply power, and check that the proper supply voltages appear at the appropriate socket pins. Disconnect power. Then install the remaining ICs, taking precautions with the MOS RAMs.

Checkout. You can check the 16K of RAM installed in the TRS-80 by running the "Function and RAM test" pro-

CKMEM PROGRAM

ADDR	CODE	MNEMONIC	REMARK
4400	21 18 44	LD HL, 4418H	; INITIALIZE POINTER
4403	0E 01	LD C, 01H	; TEST PATTERN BUFFER
4405	71	LD (HL), C	; WRITE PATTERN IN LOC.
4406	06 08	LD B, 08H	; SET LOOP COUNT TO EIGHT
4408	CB 06	RLC, (HL)	; ROTATE LEFT CIR. IN MEM
440A	CB 01	RLC, C	; AND IN REGISTER C
440C	79	LD A, C	; GET TEST PATTERN AND
440D	BE	CP (HL)	; COMPARE
440E	20 05	JRNZ, 5	; EXIT ON MEM ERROR
4410	10 F6	DJNZ, -10	; ELSE LOOP TILL DONE
4412	23	INC HL	; POINT TO NEXT MEM LOC.
4413	18 F0	JR, -16	; LOOP TO CONTINUE TEST
4415	CD 91 40	CALL, 4091H	; STOP IN TBUG

grams listed in the TRS-80 User's Manual. Running time is about 12 minutes. Next, with the power disconnected from both the TRS-80 and expansion module, connect the two together. Power-up first energizing the expansion system and then the computer. On typing the command PRINT MEMORY, 19,967 should appear on-screen. If not, deenergize the TRS-80 for 10 seconds and try again. If

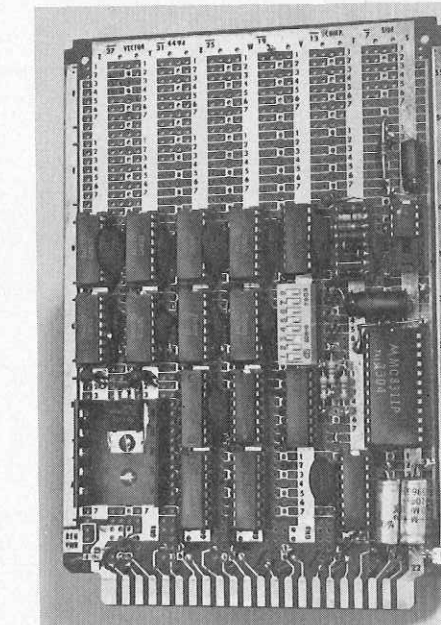
revise machine language programs located at the far end of memory when you add more memory. A DIP switch can be used to select either pin 9 or pin 17 of IC17, allowing instant movement of the 4K block to the far end of memory. On powering up when using memory beginning at F000 always energize the TRS-80 first. Typing PRINT MEMORY should now yield 15,871 on-screen.

With any use of the RESET button, always type in PRINT MEMORY. For rapid memory checks and troubleshooting, use machine language program check memory CKMEM, which runs through 20K of memory in 5 seconds. You may wish to acquire the TBUG monitor for high-speed memory tests if for no other reason than to run CKMEM.

Check Memory Program. The CKMEM program given in the table writes a test pattern of a single 1 bit into a memory location and reads back the stored pattern for a comparison test. Rotated left circularly, this 1 bit is used to check all bit positions. Whenever a mismatch or RAM error is encountered, the program exits to TBUG monitor control and register pair HL holds the address at mismatch.

Entered as listed in Level I machines, the CKMEM program begins testing at address 4418 as shown in the first instruction. No changes are required to relocate the program in memory, apart from starting address initialization. The program can be used to fill memory with 0s by changing the second instruction to 0E 00. To check 4K of RAM at the remote end of memory, change the first instruction to 21 00 F0.

Program CKMEM may miss certain address-line wiring errors of the RAM board that are caught by the TRS-80 RAM test program. Either program will catch bad chips. Program CKMEM and TBUG monitor commands simplify isolation of a bad RAM, but don't be too quick to condemn a chip until it is proven defective by direct substitution. Once the whole system is up and running, you are ready to broaden your programming horizons with a system that has enough RAM to run sophisticated software. ♦



The memory expansion system mounted on a 4494 plug board. There is room for eight additional RAMs if desired.

the computer still won't function properly, power down and check for bus line shorts. (If the program prints out RAM error immediately, look for wiring errors.) If the test program runs well into the test but stops at random times, the most likely cause is noise or crosstalk. A short ribbon cable, low-impedance ground and supply lines, and adequate bypassing are required.

Users of the TRS-80 TBUG machine-language monitor have the option of placing the 4K of RAM at the far end of memory. This obviates the need to