16K STATIC MEMORY

VANDENBERG DATA PRODUCTS

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INTRODUCTION

The 16K Static RAM operates in the static mode as opposed to dynamic memories which require periodic refreshing. All address and data lines are buffered. The memory chips and most of the logic chips are burned in and parametrically and functionally tested. The memory is designed to operate in S-100 systems with a 500ns clock. It requires approximately 10 ma at -16V; approximately 90 ma at +16V; and approximately 650 ma at +8V. Each 4K segment of memory on the 16K card may be assigned a starting address on any 4K boundary. Phantom control is strappable for Sol or other systems. The card does not require a front panel for generation of MWRITE (pin 68). This will allow use of the memory with a stand-alone bus and CPU. Memory chip speed and timing is illustrated on Page 18.

This manual supplies the information needed to assemble, test, and use the 16K memory. We suggest that you first scan the entire manual before starting assembly. Then make sure you have all parts and components listed in the Parts List. Carefully inspect the P.C. board by placing it over a lamp and looking for hairline shorts or opens. Quality control of P.C. boards is difficult and defects found early can more easily be corrected.

Should you encounter problems during assembly, call on us for help if necessary. If your completed module does not work properly, recheck your assembly step-by-step. Many problems stem from poor soldering, backward installed components, and/or installing the wrong component. Once you are satisfied that the module is correctly assembled, feel free to ask for our help. (Telephone calls requiring technical assistance should be placed between 6-8 P.M. California time.)

THEORY OF OPERATION

Refer to Vandenberg Data Products 16K Schematic.

In the 16K memory a cycle is a timed sequence of events that performs one memory access. There are 4 kinds of cycles: read, write, front panel read, and front panel write. All memory accesses are initiated by the leading edge of either DBIN (78) or MWRITE (68).

A central consideration in the operation of the memory chips is the timing of chip enable which should not exceed 2 usec. Otherwise, loss of data may occur (no chip damage).

The memory will be inactive (chip enable low) or become inactive as a result of 3 situations.

First, invalid board address will always cause the board to be quiescent. Valid memory address (VMA) is a long duration signal that very frequently will exceed 2 usec during normal CPU operation. The falling edge of either DBIN (78) or MWRITE (68) will always disable the memory prior to loss of valid memory address and thereby satisfy the time limitation of chip enable (CE). The memory remains inactive until the next occurrence of valid memory address and the rising edge of either DBIN or MWRITE. The above situation is the case during normal CPU operation.

Second, during most front panel operations the CPU will execute normally as above for a few cycles, then enter the wait state with the memory in a read cycle. DBIN and valid memory address will be on for an indefinite period of time. In this situation, 1/2 of the 74LS123 (U3) will time out causing the memory data to be latched by the 8212 for front panel display. The time out occurs at approximately 750ns after the leading edge of either DBIN or MWRITE. The duration of the time out is not critical (U-3, pins 14 and 15). The time limit of the 74123 is longer than the normal duration of a CPU controlled memory read or write cycle, therefore it is functional only during front panel operations.

Third, during front panel controlled memory write cycles, the write signal is excessively long. Half of the 74LS123 detects only the edge of the MWRITE strobe and triggers the other half through the clear input and the write cycle is timed out in approximately 750ns.

Since the only use of the output data latch is during a wait generated by the front panel, the 8212 (U10) passes data straight through from the memory to the bus during normal memory read cycles. (The 16K memory does not generate a wait state.)

The data output is inverted by the uPD410 memory element. Therefore all data written to memory is inverted before storage. Any one of four 4K memory blocks on the 16K memory can output data through the 8212 driver/latch. Only one memory bank (A, B, C, or D) is active at a time. The data output of the other three banks is tristated at the other memory chips.

The tri-state release (TSR) function controls the tri-state output of the 8212. The 8212 is always in the high resistance state except when DBIN, VMA, and MEMR are active high, (U9). When not tri-stated, input to the 8212 is driven directly onto the bus, DIO-DI7.

The memory does not have memory protect. However, unused S-100 bus lines are provided with plated-through holes on the memory card to facilitate jumpers from an external memory control device. Memory bank switching can be implemented through use of external memory control to allow use of more than 64K of memory.

The 16K memory bank is enabled or disabled (switched) through use of P1 connecting to pins 18 and 19 of U8. (Refer to the TTL Data Book for 74154.) P1 is normally connected to ground (enabled) by a trace on the back of the P.C. board. This ground connection must be cut if P1 is to be used by an external memory controller to switch the memory bank. When P1 is grounded the memory will respond to address and control inputs normally. When P1 is high the memory is disabled. When disabled, another 16K memory having the same address assignment may be active without interference.

SOL PHANTOM CONTROL - To implement the Sol 20 phantom memory control, invert the memory control signal into P1 as follows:

- Cut the P1 connection to ground on the back of the P.C. board (U8 pins 18 and 19).
- Cut the spare inverter's grounded input on the component side of the board at P5 coming into Pin 10 of U1. (A small triangle marks where to cut.)
- Connect the phantom control signal(memory disable) from S-100 pin 67 to P5 (U1, pin 10) using the strap holes provided.
- Connect the inverted phantom control signal from P2 or P3 (U1, pin 9) to P1 (U8, pin 19).

Now whenever the phantom control line goes low on S-100 pin 67, the input to the 74154 pins 18 and 19 will go high thereby disabling the entire board and allowing the Sol to access other memory having the same address. This modification is not required unless the Sol owner assigns addresses to the 16K RAM that coincide with Sol system memory addresses.

PARTS LIST

Quantity			
INTEGRATED CIRCUITS			
1	8212 or 74S412	U10	8 bit latch, tri-state buffer
1	74L02	U2	Quad dual input NOR
1	74L20 or 7413	U9	Dual four input NAND
1	74123 or 74LS123	U3	Dual retriggerable one shot
2	74367	U6 and U7	Hex tri-state buffer
2	74368	U1 and U5	Hex tri-state inverter
1	3245	U4	Quad MOS level driver
1	74154	U8	4 to 16 line decoder
32	uPD410	4x8 memory array	4K x 1 memory parts
REGULATORS			
1	7805 or LM340K-5		+5 volt regulator
1	7812 or LM340K-12		+12 volt regulator
1	1N751A 5V Zener Diode		-5 voltage reference
RESISTORS			
4	51 ohm	R1-4	Green, brown, black
2	15K ohm	R5-6	Brown, green, orange
3	1K ohm	R7-9	Brown, black, red
1	1.3K ohm	R10	Brown, orange, red
CAPACITORS			
38	.1 uf	C2,4,7,9-12,15,17-19,21-25,28,30-37,39-41,43-52	Despiking caps
2	100 pf	C8, 14	Timing caps, disk
2	22 uf	C1, 6	Electrolytic
10	4.7 uf	C3,5,13,16,20,26,27,29,38,42	Dipped tantalum
SOCKETS			
2	14 pin		Low profile sockets
6	16 pin		Low profile sockets
32	22 pin		Low profile sockets
2	24 pin		Low profile sockets
20			Wire wrap posts
MISCELLANEOUS			
1	PC Board		
1	Manual		
4 ea.	6-32 screws, hex nuts, star washers		

ASSEMBLY

Check all parts and components against the Parts List. Carefully inspect the etching of the printed circuit board. Look for any areas where the etching may not have been complete. When installing components, refer to the Component Layout drawing to aid you in installing the components correctly.

To simplify reading resistor values after installation, install resistors so that the color codes read from left-to-right and top-to-bottom as appropriate.

Install disc capacitors as close to the board as possible. Spread the legs with needle-nose pliers prior to installation if small-base disk capacitors are supplied with your kit.

The memory IC's used in the 16K memory are MOS devices. They can be damaged by static electricity discharge. Always handle MOS IC's so that no discharge will flow through the IC. Avoid unnecessary handling and wear cotton rather than synthetic clothing when handling the IC's.

Soldering: Use a low-wattage iron, 25 watts, for all sockets and light components. Solder neatly and quickly. Use a 35-40 watt iron for soldering the regulators and heavy components. Over-heating of the P.C. pad or trace can cause the pad or trace to "lift" off the board and permanently damage it. Use only 60-40 rosin-core solder. NEVER use acid-core solder or externally applied fluxes. Maintain a continuous watch for solder bridges while soldering sockets and components. The 16K memory has a solder mask (green lacquer coating) on both top and bottom of the board. This mask minimizes the chance of creating solder bridges during assembly.

Precaution: Never install the 16K memory, or remove it from the computer with the power on. To do so can damage the memory and the computer. Do not install or remove IC's while power is applied to the 16K memory. To do so can damage the IC.

The following tools, equipment, and materials are recommended:

- Needle-nose pliers
- Diagonal cutters
- 25 watt Soldering Iron and 35-40 watt Soldering Iron
- 60-40 rosin-core solder
- Volt-ohmmeter

All components will be on the front side of the board. The front side is identified by the name "Vandenberg Data Products." All soldering is done from the back.

( ) Using an ohmmeter, check the circuit board to insure that there are no shorts between the memory chip mounting pads. Measure between all combinations of vertically and horizontally adjacent pads. There should be no continuity in any of these measurements. This measurement is needed on only one of the 32 memory chip pads except for pins 5, 6, 7, 12, and 17 which should be tested on one chip in each of the four verticle memory columns, A, B, C, and D.

( ) 8 and 12 Volt Bus Test: Measure between positive mounting pad of C1 and pin 50 or 100 of edge connector. Also measure between positive mounting pad of C6 and pin 50 or 100 of the edge connector. There should be no continuity in either measurement.

If you measure continuity in any of the preceeding tests, the P.C. board is defective and should be returned to Vandenberg Data Products for replacement. (Please provide description of problems found on returns.) If none of the measurements show continuity, proceed.

( ) Install all sockets. Carefully avoid flowing solder into empty holes that must be filled later in the assembly with other components such as capacitors. Particular care is required to avoid flowing solder into empty holes while soldering socket pin 22 A6; pin 11 of B2; and pin 6 of U3. Watch the orientation of pin 1 on sockets. Insert each socket snug on the P.C. board from the component side and tack each socket on the back at opposite corners. Solder the entire set completely.

	Quantity	Description
( )	32	22 pin sockets
( )	6	16 pin sockets
( )	2	14 pin sockets
( )	2	24 pin sockets

( ) Install all resistors except R10. Bend leads to fit distance between mounting holes, insert leads, pull down snug to board, bend leads outward on back (solder) side of board, solder, and trim. Be careful not to install R7 into the R6 location. Check installation of R6 and R7 with component layout drawing.

	Location	Value	Color Code
( )	R1-4	51 ohm	Green, brown, black
( )	R5-6	15K ohm	Brown, green, orange
( )	R7-9	1K ohm	Brown, black, red

NOTE:
When installing .1 uf and 4.7 uf capacitors between the rows of sockets in the memory array, insert all capacitors in one row before soldering to avoid solder flowing into empty holes, thereby complicating later installations.

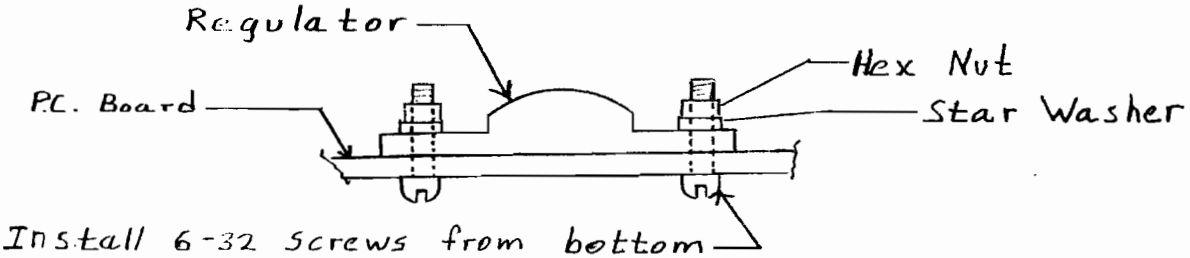
( ) Install ten 4.7 dipped tantalum capacitors: C3, 5, 13, 16, 20, 26, 27, 29, 38, 42. Observe the polarity markings on each tantalum capacitor and install the capacitor leg marked with a "+" or "•" (dot) into the hole labeled "+" on the P.C. board. Also refer to the Component Layout drawing. Bend the leads outward on the back (solder) side of the board, solder, and trim. Check for correct orientation.

( ) Install 38 .1uf capacitors: C2, 4, 7, 9-12, 15, 17-19, 21-25, 28, 30-37, 39-41, 43-52. After bending and inserting leads through mounting holes, pull down snug to board, bend leads outward on back (solder) side of board, solder, and trim.

( ) Install the wire-wrap strips in the memory addressing area above IC-8. 16 pins are for 0-F and 4 pins for A-D on the P.C. board. The plastic should be on the component side of the board. The <u>short</u> end is soldered into the hole from the back side of the board. Before using the memory board, refer to addressing instructions.

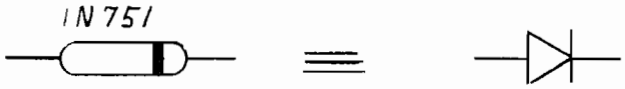
( ) Install C8 and C14 near IC 4 (100 pf each).

( ) Install the two regulators on the component side of the board. (Soldering the regulator legs is the last step.) Be sure the 5 Volt and the 12 Volt regulator (7812 or LM340K-12) is installed in its correct position, at the bottom of the board for the 12V and at the top for the 5V. WARNING: damage may result if the 12V regulator is installed in the 5V location. It is important that a good electrical contact be established between the case (ground), case screws, and the ground plane on the top and bottom of the P.C. board. Fasten each regulator to the P.C. board using two each 6-32 screws, star lockwashers, and hex nuts. To ensure a long lasting mechanical/electrical connection, insert the screws from the back (solder) side of the board (no washer here) and place the star washer between the hex nut and the case of the regulator on the front (component) side of the board. When the regulator is firmly tightened in place, solder the legs and trim off the extra length.



( ) Install the two 22 uf electrolytic capacitors, C1 and C6, in their horizontal position above and below the two regulators. Observe the polarity of the capacitors and install the positive end toward the right edge of the P.C. board. For appearance, bend leads so that the capacitor value, 22 uf, is visible. Solder leads and snip off the extra lead length.

( ) Install the zener diode D1 (1N751A) in its location between the memory chips and the bus pins at the bottom of the board. Position the diode so that its dark band mark (cathode) is on the right-hand side.



Install R 10 (1.3K ohm, Brown Orange Red). Solder and trim.

( ) Check regulator operation. This check is made to prevent potential subsequent damage to IC's from incorrect voltages. (No IC's should be installed.) Install 16K memory in computer. (Use of an extender card is recommended. Do not install the board backwards or install or remove the circuit board with power on.) Turn the power on and measure the

voltages between ground and the output of each regulator. (VCC = +5V, VDD = +12V, VBB = -5V.) Voltage levels should be ±5% in each case. Measure voltage at one memory chip position in each 4K memory bank (A,B,C,D). Pin 1 of uPD410 = -5V; pin 11 = +5V; pin 18 = +12V. (Pin one is marked on P.C. board with white dot.) If any voltages are incorrect, determine and correct the cause before proceeding. Especially check for solder shorts. If voltages are correct, turn power off, remove module from computer, and continue assembly.

( ) Install all IC's in the individual locations. Pay careful attention to the proper orientation. Pin 1 is indicated by a dot on the P.C. board and assembly drawing. All IC's have the same orientation with pin 1 to the upper right. Pin 1 is usually identified on the IC by a dot on the case.

	IC No.	Type
( )	U1	74368
( )	U2	74L02
( )	U3	74LS123
( )	U4	3245
( )	U5	74368
( )	U6	74367
( )	U7	74367
( )	U8	74154
( )	U9	74L20 or 7413
( )	U10	8212 or 74S412

( ) Install 32 uPD410 memory chips. Pin one is marked on the chip and on the board with a dot. Pay careful attention to proper orientation.

CAUTION: MOS MEMORY INTEGRATED CIRCUITS CAN BE DAMAGED BY STATIC ELECTRICITY DISCHARGES. HANDLE THESE IC's SO THAT NO DISCHARGE FLOWS THROUGH THE IC. AVOID UNNECESSARY HANDLING AND WEAR COTTON CLOTHING RATHER THAN SYNTHETIC CLOTHING WHEN HANDLING THESE IC's. (STATIC CHARGE PROBLEMS ARE MUCH WORSE IN LOW HUMIDITY ENVIRONMENTS.)

( ) Inspect all IC's for orientation. All IC's have the same orientation. Pin one is toward the right side of the board.

( ) Inspect all IC's for pins not correctly inserted in socket. Carefully straighten any bent pins with needle-nose pliers and reinsert the chip in its socket. Note: the 14 and 16-pin

sockets are high reliability Burndy products that have a higher than usual extraction force. Use an extractor tool, if available, to aid in chip removal.

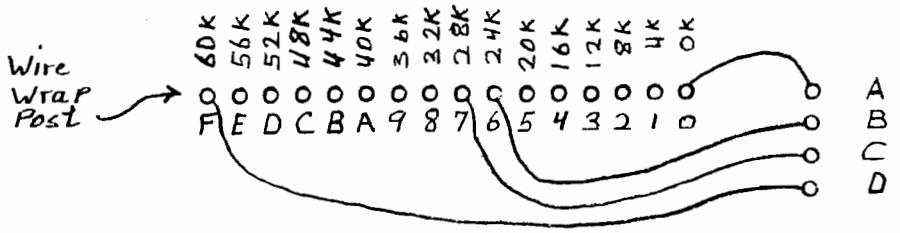
( ) Address each 4K segment of the 16K memory. See below.

( ) Install the 16K memory in your computer and test it for proper operation. Be certain the 16K memory address selection does not conflict with existing memory address assignments. Verify front panel operation. Memory test programs and instructions for testing are provided in this manual.

MEMORY ADDRESSING:

4 independent 4096 byte memory banks are on the 16K memory card. They are labeled A,B,C,D along the top of the memory card. Each 4K bank select has a wire wrap pin labeled A,B, C, or D in the memory addressing area near IC 8. Any one of 16 memory addresses, 0000-F000 Hex(00-60K Decimal, 1K = 1024), can be assigned as the starting address for a 4K memory block. This is done by connecting any one of the 16 address pins to any one of the bank select pins. Wire wrap, slit and wrap, or point-to-point soldering work well. No bank (A,B,C, or D) should have more than one connection (address). The four 4K banks can be but do not have to be contiguous. For example Bank A could be assigned 0 to 4K, Bank B and C 24 to 32K, and Bank D 60 to 64K.

The above example would be connected as follows:



CAUTION: Be sure memory address selection does not conflict with other memory address assignments.

SHORT MEMORY TEST

When the user loads the program, the starting address must be patched into Hex locations 0003 and 0004. The end address plus one must be patched into locations 0006 and 0007.

First, the program writes zeros into all addresses that are to be checked. Next, it starts again at the first address, reads a byte, and compares it to the pattern that was written in. If that byte matches the pattern that was written, the byte is incremented by one and stored into the address from which it was read. This process saves time by writing the next test pattern long before it will be needed in the next read loop.

The program continues to read, verify, and rewrite until it finds an error (byte that doesn't match reference pattern) or until all addresses have been checked.

If there are no errors, the program repeats again and again; the pattern will vary from 0 to 255 and back to 0, etc.

If there is an error, the address where the error occurred is saved at locations 003C and 003D Hex. (These locations will remain FF, FF if no errors are found.) The reference pattern will be stored at 003A. The bad data that is read is saved at location 003B.

After saving the error information, the program loops at location 0022 until the user stops it. For the jump to self, the user can substitute a jump to his own binary-to-ASCII conversion and I/O routines.

To locate the memory chip in which the error is occurring, data bits are labeled 0 through 7 along the left edge of the memory card, and memory banks are labeled A through D along the top of the card. Given an address and a failing bit, the problem memory chip can be identified. The short memory test program will give the address and bad data. Exchange memory chips when a bad bit is found in order to determine whether the chip itself is bad or whether the supporting circuit is defective. The memory bit failure should move with the chip if the memory chip is defective. Reliable operation of the VDP 16K memory depends in part upon the condition of your S-100 bus and sockets. Operation on extender cards is not reliable, particularly with Z-80 CPU's. (Extender cards can be used for logic testing and will not harm the memory.)

Begin program execution at 0040 Hex or higher. "*" indicates the bytes to change if the program is relocated.

Hex Address	Hex Obj. Code	Octal Obj. Code	8080 Mnemonic	Comments
0000	AF	257	XRA,A	Zero A Register
01	4F	117	MOV C,A	Set First Test Byte in C
02	21	041	LXI H	SET START ADDRESS
03	xx	xxx	xx	Low byte
04	xx	xxx	xx	High byte
05	11	021	LXI D	SET END ADDRESS
06	xx	xxx	xx	Low byte
07	xx	xxx	xx	High byte
08	71	161	MOV M,C	Zero Test Data to Memory
09	23	043	INX H	Next Place to Store
0A	7C	174	MOV A,H	
0B	BA	272	CMP D	Test High Order byte for
0C	DA	332	JC	END OF MEMORY Test Range
0D	08	010	*	Jump and Write Next Memory
0E	00	000	*	if not end of Range
0F	7D	175	MOV A,L	
0010	BB	273	CMP E	Test Low Order byte for
11	DA	332	JC	End of Memory test range
12	08	010	*	Jump and Write next Memory
13	00	000	*	if not end of Range
14	2A	052	LHLD	Reset Memory Pointer to
15	03	003	*	Starting Test Address
16	00	000	*	
17	7E	176	MOV A,M	Read Memory
18	B9	271	CMP C	Check with Correct Value in C
19	CA	312	JZ	If Correct Value then Jump
1A	25	045	*	
1B	00	000	*	
1C	22	042	SHLD	Error has occurred -
1D	3C	074	*	Save Failing Address
1E	00	000	*	
1F	32	062	STA	Save Bad Data
0020	3B	073	*	
21	00	000	*	
22	C3	303	JMP	STOP LOOP - ENTERED
23	22	042	*	on first Error
24	00	000	*	(User I/O here)
25	3C	074	INR A	Write Next Pattern back
26	77	167	MOV M,A	where we just read to save
27	23	043	INX H	time. Step to next address.
28	7C	174	MOV A,H	Are we at end of Range?
29	BA	272	CMP D	Check High Byte
2A	DA	332	JC	Jump if not to end of range
2B	17	027	*	
2C	00	000	*	
2D	7D	175	MOV A,L	Check Low Byte
2E	BB	273	CMP E	
2F	DA	332	JC	Jump if not done
0030	17	027	*	

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  31     00    000          *
  32     0C    014          INR C          New Reference for Compare
  33     79    171          MOV A,C
  34     32    062          STA            Save for User to see it
  35     3A    072          *
  36     00    000          *
  37     C3    303          JMP            Start Again
  38     14    024          *
  39     00    000          *
  3A     FF    377          DATA           Correct Test Pattern Stored
  3B     FF    377          DATA           Bad Data Stored Here
  3C     FF    377          DATA           Error Address Low Byte
003D     FF    377          DATA           Error Address High Byte
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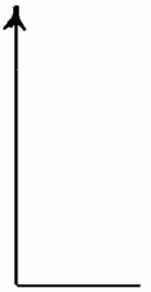


TROUBLE SHOOTING

The following measurement points are silkscreened on the P.C. board.

Label	Description	Location
VMA	Valid Memory Address	U1, pin 2
EA	Chip Enable Memory Column A	R1
EB	Chip Enable Memory Column B	R2
EC	Chip Enable Memory Column C	R3
ED	Chip Enable Memory Column D	R4
TSR	Tri-state Release	U10, pin 1 (feedthrough)
LAT	Latch	Feedthrough (near U5 pin 1)
$\overline{WE}$	Write Enable Not	U1, pin 7

This program may be useful in servicing the VDP memory. An oscilloscope would be used to examine the control signals being generated for the memory chips by the CPU and memory logic. The program operates in a loop that writes the front panel sense switches of an Altair or IMSAI into a single byte in the memory undertest, reads the byte from the memory undertest, and outputs the byte to the front panel of an IMSAI. The loop repeats indefinitely allowing examination of essential signals on the memory card. (Be sure oscilloscope is grounded to CPU chassis first. The oscilloscope should be capable of displaying 400-500 ns pulses. Dual trace is desirable with one trace triggering on CE (C), pin 7, IC 4.)

Hex Address	Hex Obj. Code	Oct. Obj. Code	8080 Mnemonic	Comments
0000	21	041	LXI H	Initialize address pointer to memory
01	00	000	-	LSP Memory Address
02	20	040	-	MSP Memory Address (8K example)
03	DB	333	→IN	Read Front Panel
04	FF	377	FF	Sense switches
05	77	167	MOV M,A	Write Switch Data to Memory
06	7E	176	MOV A,M	Read Data Back
07	D3	323	OUT	Display on IMSAI
08	FF	377	FF	Front Panel
09	C3	303	JMP	
0A	03	003	03	
0B	00	000	└─00	

Measure the presence of the following signals:

VMA (Valid Memory Address) IC-1, pin 2; Duration not critical approximately 1500 ns. Must be active high during CE active high.

CE (Chip Enable) Sellect correct EA, EB, EC, or ED. The signal is a +12V MOS level from the INTEL 3245 TTL to MOS level converter. Pulse duration is normally 400ns. The memory chips are active only when this signal is active high. $\overline{WE}$ (Memory write active low) should coincide with one CE pulse. $\overline{WE}$ duration of 400ns is typical. If CE is not present from the INTEL 3245, check for low address strobe on pin 3 (be sure program address and address jumper are correct). Only the 74154 can be in question if pin 3, U4 does not have active low pulse.

Next test pin 12 of INTEL 3245 (IC 4). Two repetitive active low pulses should be present, one from MWRITE and one from DBIN (Memory read). Absence of signal should be traced back through IC 2 and IC 1.

Next test pin 13 of INTEL 3245. Both pin 12 and pin 13 should be active low simultaneously, however pin 13 will be low longer than pin 12. Pin 13 and IC3 are used for front panel operations, however they must also operate when the front panel is not in control. Pin 9 of the 74123 initiates the deposit of data into memory from the front panel. The other half of the 74123 times out any DBIN or MWRITE signal that exceeds approximately 750ns and activates the latch. Both DBIN and MWRITE pulse duration exceed 750ns when the front panel has control of the system.

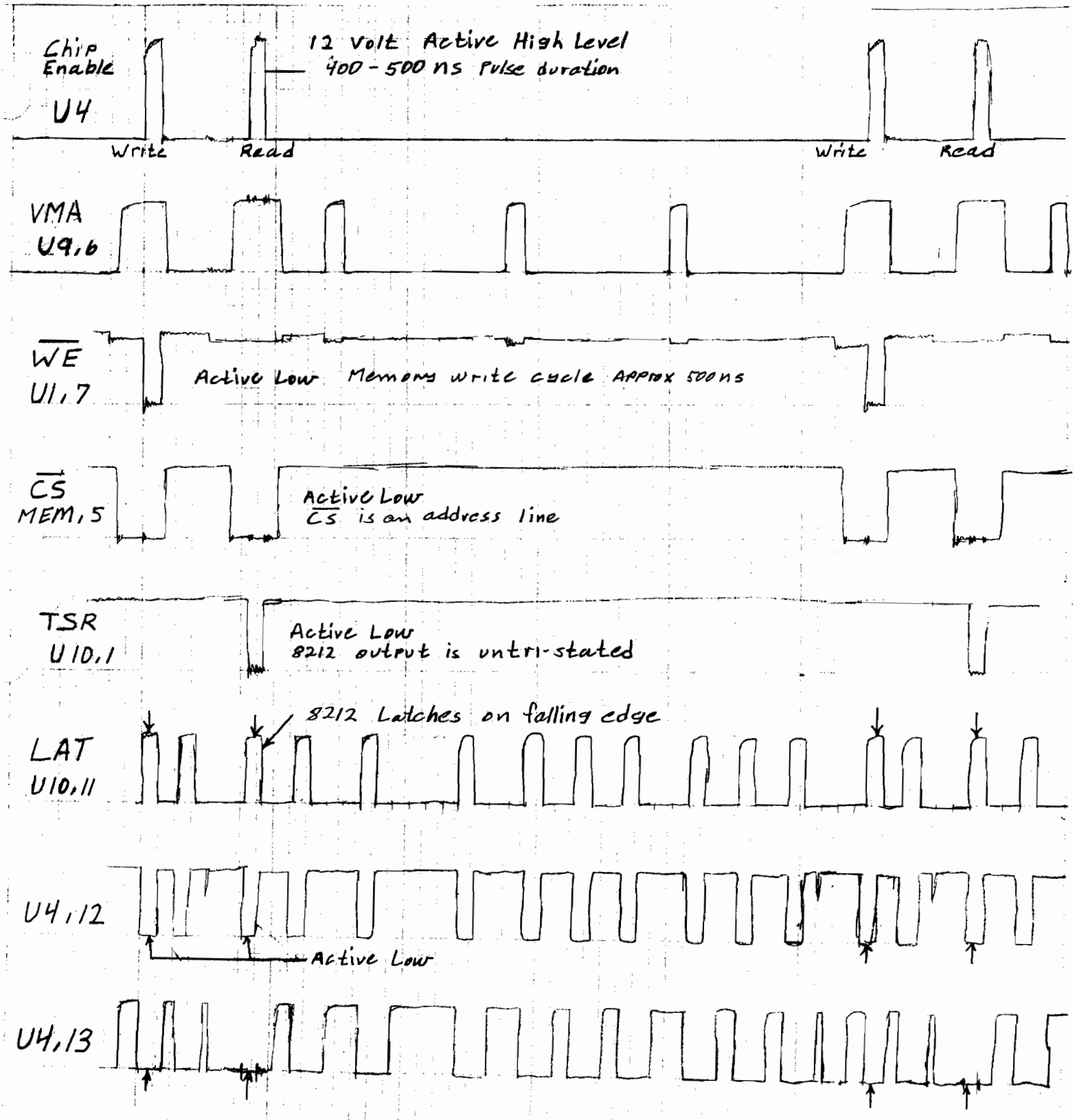
Verify that CE, $\overline{WE}$, $\overline{CS}$, D_{IN}, $\overline{D_{OUT}}$ are delivered to a memory chip. Vary sense switch setting to observe operation of D_{IN} and $\overline{D_{OUT}}$.

TSR - Tri-state Release, this signal, IC 10 pin 1, puts memory data onto the S-100 bus. Active low duration controlled by DBIN.

LAT - Latch, this signal is useful only for front panel operation where CE read and write on time is timed out by IC 3. The data must be latched in order for the front panel LED's DI0 - DI7 to display memory contents. However the latch operates at all times at the end of memory read or write. The 8212 latches on the falling edge, IC 10 pin 11. During program operation the signal is the inverse of pin 12, IC 4.

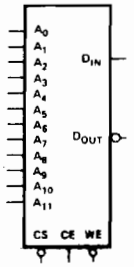
$\overline{WE}$ - Write Enable Not, this signal defaults to a high level except on a memory write operation when the signal is driven low by a MWRITE (bus line 68). (The default is a memory read.) For the memory write to occur, chip enable goes high and $\overline{WE}$ goes low and address and data are stable.

MEMORY TIMING

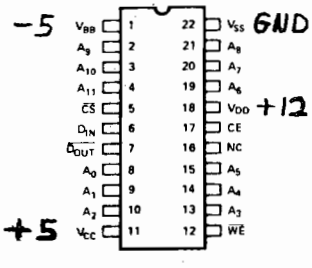


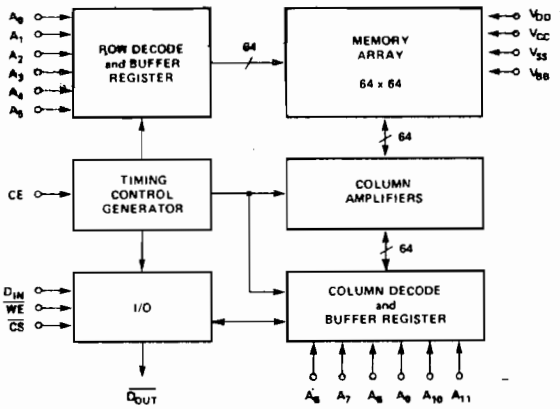
Altair 8800 CPU - Memory Timing example.
500 ns per division - CPU is executing the trouble shooting program given in the manual.

LOGIC SYMBOL

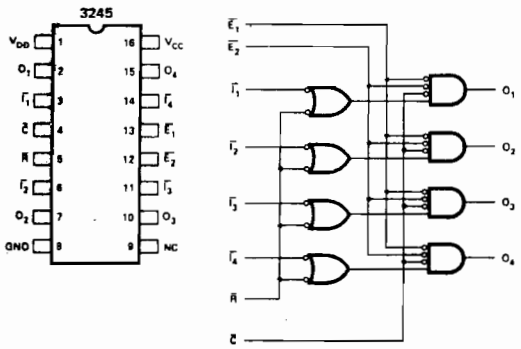


PIN CONFIGURATION



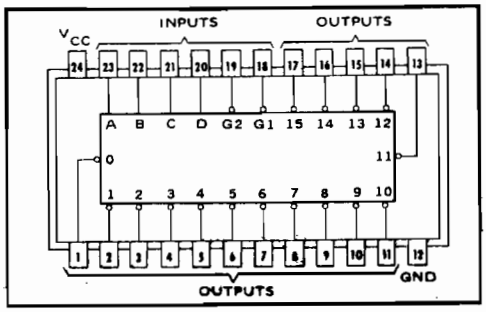


μPD410



U4 3245

(TOP VIEW)

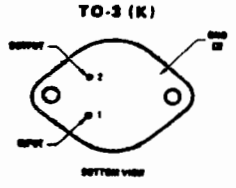


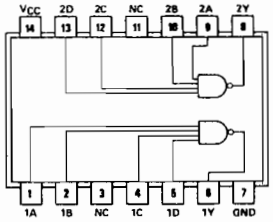
U8 74154

5V 7805

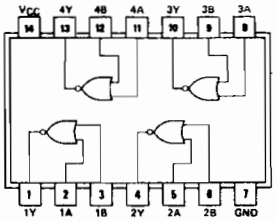
12V 7812

TO-3 (K)





U9 74L20



U2 74L02

'367

FUNCTION TABLE

(EACH DRIVER)

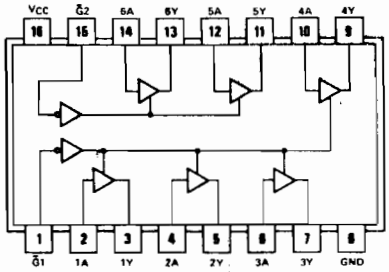
U6,7

74367

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	H
L	L	L

H = high level, L = low level,
X = irrelevant, Z = high-impedance

(TOP VIEW)



'368

FUNCTION TABLE

(EACH DRIVER)

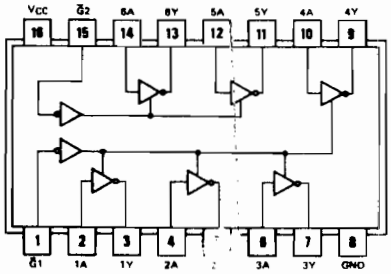
U1,5

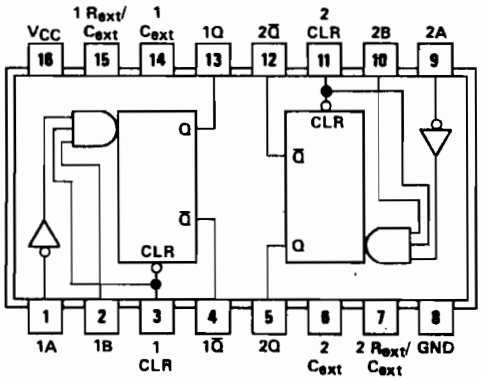
74368

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

H = high level, L = low level,
X = irrelevant, Z = high-impedance

(TOP VIEW)





'LS123 FUNCTION TABLE

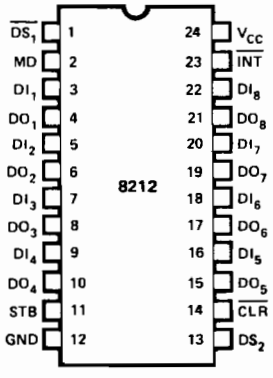
INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

U3 74LS123

U10 8212

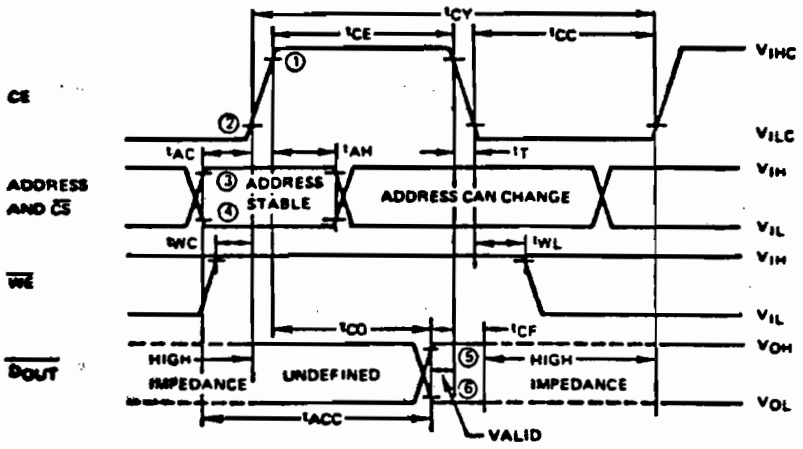
or 74S412

PIN CONFIGURATION

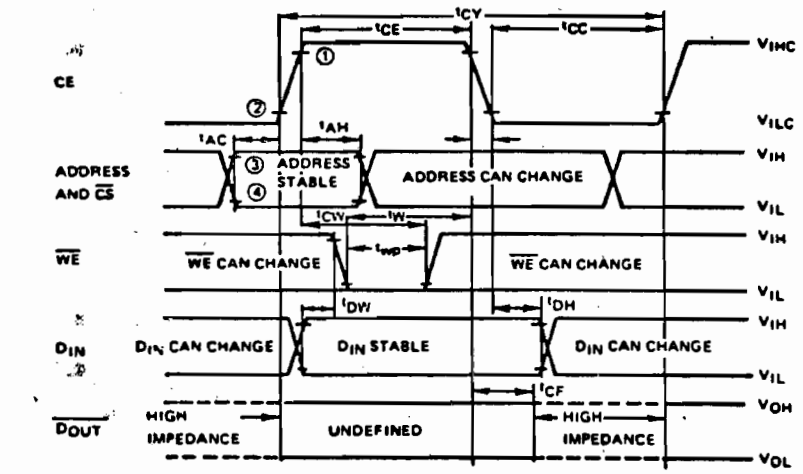


μPD410 TIMING

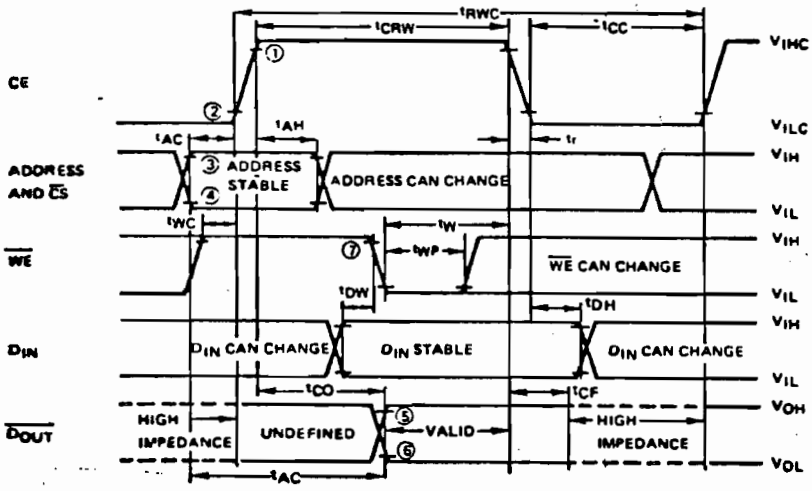
READ CYCLE



WRITE CYCLE



READ MODIFY WRITE CYCLE



NOTES:

1. V_{DD} −2V is the reference level for measuring timing of CE.
2. V_{SS} +2V is the reference level for measuring timing of CE.
3. V_{IH}MIN is the reference level for measuring timing of the addresses, CS, WE and D_{IN}.
4. V_{IL}MAX is the reference level for measuring timing of the addresses, CS, WE and D_{IN}.
5. V_{SS} +2V is the reference level for measuring timing of D_{OUT}.
6. V_{SS} +0.8V is the reference level for measuring timing of D_{OUT}.
7. WE must be at V_{IH} until end of tco.

READ, WRITE AND READ MODIFY WRITE CYCLE

PARAMETER	SYMBOL	μPD410 MIN	TYP	MAX
Address to CE Set Up Time	t_{AC}	0		
Address Hold Time	t_{AH}	90		
CE Off Time	t_{CC}	190		
CE Transition Time	t_T	0		40
CE off to Output High Impedance State	t_{CF}	0		90

READ CYCLE

PARAMETER	SYMBOL	μPD410 MIN	TYP	MAX
Cycle Time	t_{CY}	440		
CE on Time	t_{CE}	230		2000
CE Output Delay	t_{CO}			190
Access Time	t_{ACC}			200
CE to $\overline{WE}$	t_{WL}	20		
$\overline{WE}$ to CE on	t_{WC}	0		

WRITE CYCLE

PARAMETER	SYMBOL	μPD410 MIN	TYP	MAX
Cycle Time	t_{CY}	440		
CE on Time	t_{CE}	230		2000
$\overline{WE}$ to CE OFF	t_W	130		
CE to $\overline{WE}$	t_{CW}	130		
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0		
D_{IN} Hold Time	t_{DH}	60		
$\overline{WE}$ Pulse Width	t_{WP}	130		

READ MODIFY WRITE CYCLE

PARAMETER	SYMBOL	μPD410 MIN	TYP	MAX
Read Modify Write (RMW) Cycle Time	t_{RWC}	560		
CE Width During RMW	t_{CRW}	350		2000
$\overline{WE}$ to CE on	t_{WC}	0		
$\overline{WE}$ to CE off	t_W	130		
$\overline{WE}$ Pulse Width	t_{WP}	130		
D_{IN} to $\overline{WE}$ Set UP	t_{DW}	0		
D_{IN} Hold Time	t_{DH}	60		
CE to Output Delay	t_{CO}			190
Access Time	t_{ACC}			200

WARRANTY

KITS: All parts and materials are warranted to be free of defects at the time of shipment. Defective parts will be replaced free of charge if returned within sixty (60) days of receipt of delivery. Completed kits will be repaired at a labor cost of $20/hour, with defective parts replaced free. In no case will the repair charge exceed $20 without prior notification and approval of the owner.
THIS WARRANTY IS VOID IF THE KIT IS SOLDERED WITH CORROSIVE FLUX.

ASSEMBLED: The assembled units are warranted to be free of defects for one hundred twenty (120) days from the time of shipment. If they are found to be defective in this period they may be returned for repair or replacement free of charge, provided the unit has not been subjected to electrical or mechanical abuse.

Vandenberg Data Products
3998 Berrywood Drive
Santa Maria, CA 93454

ERRATA

Advertising: Vandenberg Data Products has advertised the use of low-power Schottky TTL's. However these parts are replaced with other parts having better noise characteristics.

Schematic:

U1 8T98 should read 74368

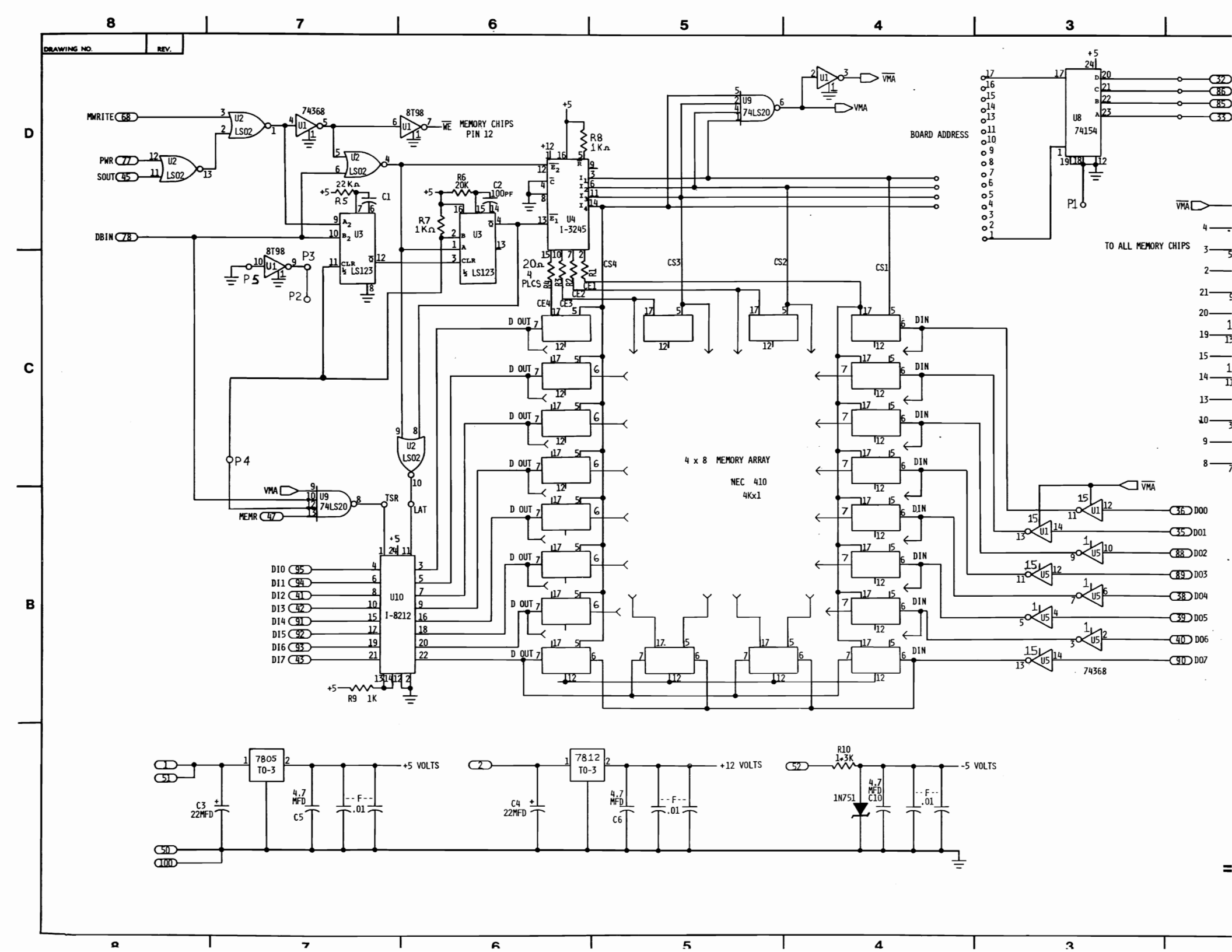
U2 74LS02 should read 74L02

U9 74LS20 should read 74L20 or 7413

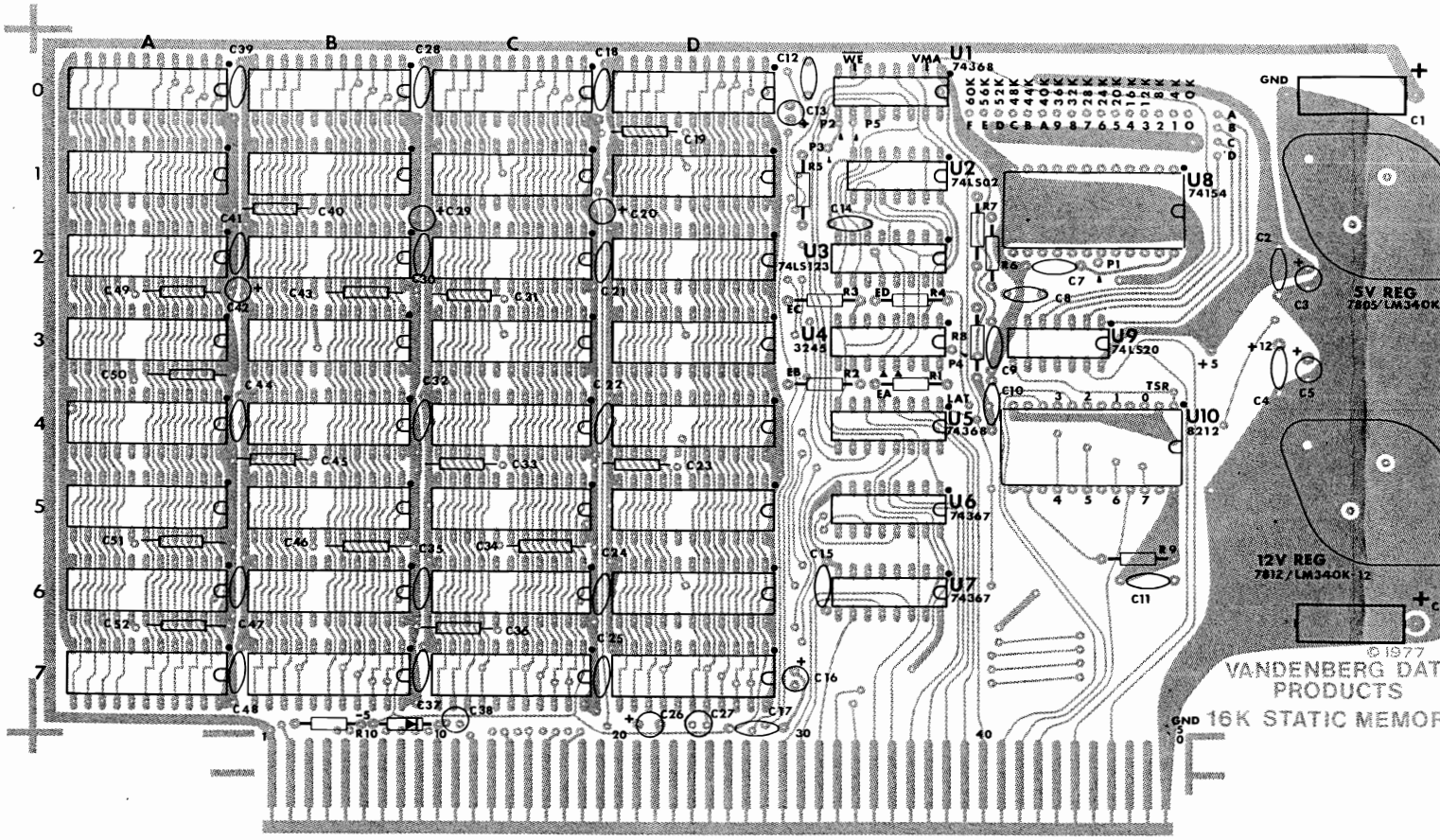
R1-4 20 ohm should read 51 ohm

R5,6 22K ohm should read 15K ohm

Revision 1:
Vandenberg Data Products has made a small cut in one solder pad of C-45 to open a short to an adjacent trace on the back side of the P.C. board. No action is required by the kit builder except to observe that the cut is intentional and therefore avoid reestablishing the short with a solder bridge.


DRAWING NO.
REV.
MWRITE 68
PWR 77
SOUT 45
DBIN 78
MEMR 47
VMA
WE
MEMORY CHIPS PIN 12
BOARD ADDRESS
TO ALL MEMORY CHIPS
4 x 8 MEMORY ARRAY
NEC 410
4Kx1
D OUT
DIN
CS1
CS2
CS3
CS4
U10 I-8212
U4 I-3245
U8 74154
U9 74LS20
U2 LS02
U3 LS123
U1 74368
8T98
R5 22KΩ
R6 20K
R7 1KΩ
R8 1KΩ
R9 1K
C1
C2 100PF
20Ω 4 PLCS
TSR
LAT
P1
P2
P3
P4
P5
D10 95
D11 94
D12 41
D13 42
D14 91
D15 92
D16 93
D17 43
DO0 36
DO1 35
DO2 88
DO3 89
DO4 38
DO5 39
DO6 40
DO7 90
7805 TO-3
7812 TO-3
+5 VOLTS
+12 VOLTS
-5 VOLTS
C3 22MFD
C4 22MFD
C5 4.7 MFD
C6 4.7 MFD
.01
R10 1+3K
1N751
C10 4.7 MFD
50
100
51
52

DRAWING NO. | REV.



5. ● DENOTES PIN 1 OF IC
4. ▲ DENOTES TEST POINT. SEE INSTRUCTIONS
3. C5 THRU C14 ARE 4.7MFD. NOTE POLARITY
2. ALL CAPACITORS MARKED "F" ARE .01MFD
1. ALL RESISTORS IN OHMS, 1/4W

NOTES: UNLESS OTHERWISE SPECIFIED