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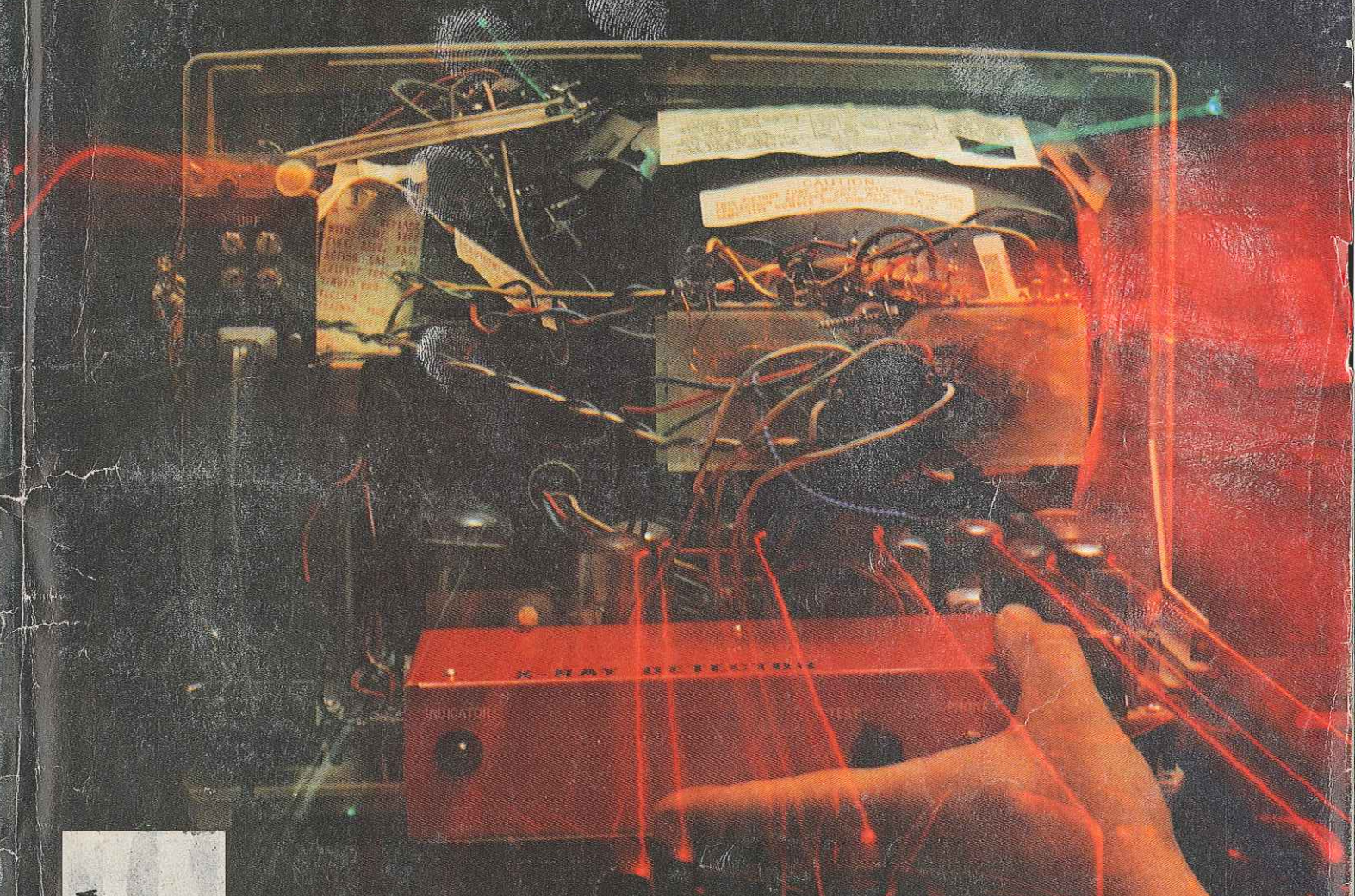
SPECIAL ISSUE—COLOR TV 1971



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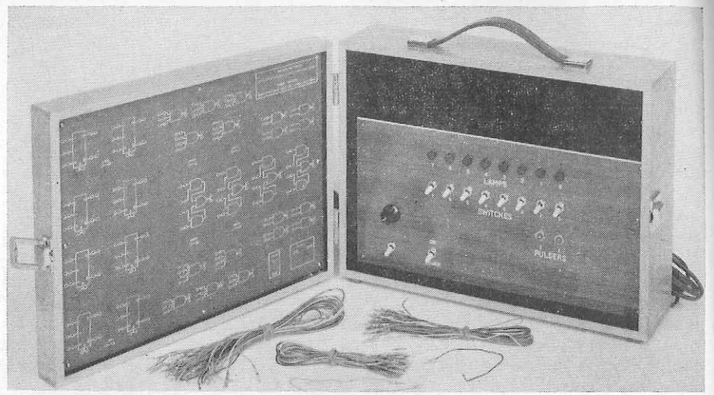
BREADBOARD A COMPUTER WITH
R-E's Logic Laboratory

by DAVID KORMAN

Last month we presented the first part of the computer laboratory. This month construction details, testing and operating instructions are presented.



Clock-lamp driver card

Assemble all diodes and resistors on the card as per the information on the printed circuit card. All diode bands go down or toward the furthest edge of the card. Solder and clip off excess lead lengths.

Install transistors Q0 thru Q7 with flat sides toward the IC's or furthest edge of the card. Solder and clip. Install unijunction transistor Q8 with the flat side toward the nearest edge of the board. Solder and clip.

Install the IC's. There is a black dot on the drawing (solid) and a copper spot on the circuit card to indicate the orientation of the dot on the IC's. Carefully solder all leads. **Do not clip these leads.**

Install the capacitors and insure that the positive end of the tantalum capacitor goes to the positive pad on the circuit card.

Test before using

Testing the gate circuits of the logic laboratory is really quite a simple procedure. The test suggested would not be adequate for extremely high clock rates but will give a good indication of the devices ability to function in the laboratory.

First it would be well to establish a few points:

As with the lamp drivers, the inputs to the logic gates look like a logical "1" if left open or disconnected. This is not acceptable procedure for design purposes for reasons that are best understood by a careful reading of the literature on TTL integrated circuits, but it will work fine at the low clock rates and loads associated with the lab.

There will be more information on this later but here are the necessary NAND circuit conditions to allow you to perform the tests. It requires all "1's" into a NAND gate to get a "0" out. Any zero in will give a one out!

In the test setup shown, the CLOCK output is connected to LAMP 0. The output of the gate being tested is connected to LAMP 1.

All inputs but one of the gate being tested are left open (logical "1") and the clock set for minimum speed is connected to the input to be tested. When the clock goes to "1", the output of the gate will go to "0" (all "1's" in give a zero out). This means that the CLOCK LAMP, LAMP 0 will be lit and the output lamp, lamp 1, will be out. As the clock goes to "0", the output of the gate goes to "1". The clock lamp goes out and the output lamp comes on.

In other words, if the lamps alternate on and off out of step, the gate input being tested is good. Test the other inputs to the gate in the same way for all 2, 3 and 4 input gates.

Operating instructions

Since every piece of electronic equipment available to industry normally has a set of operating instructions, they are included here followed by a set of test procedures that will

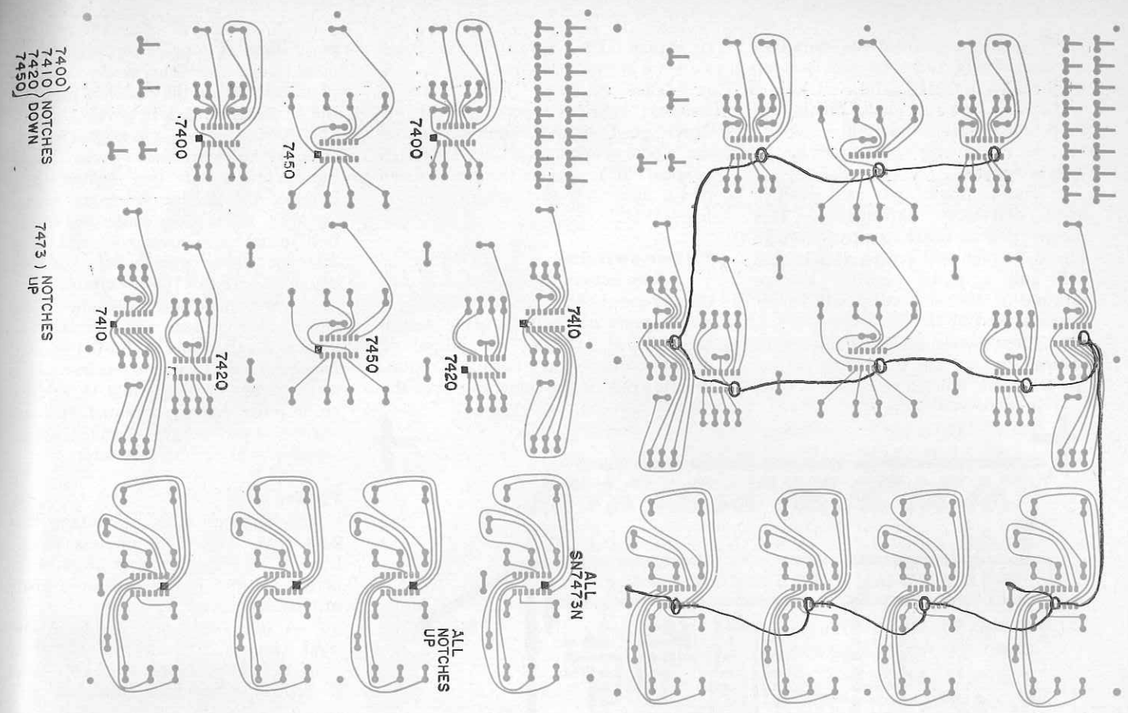
The diagrams on the facing page are repeated from our December issue. Misregistration of color last month made them unusable.

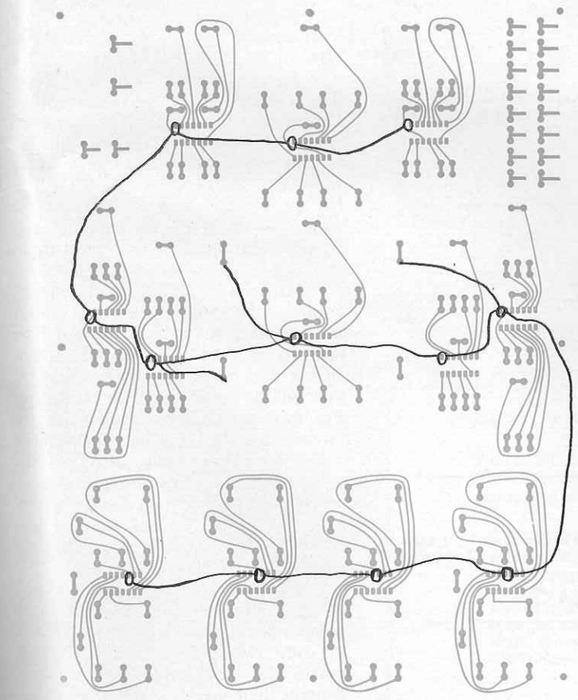
LOGIC LAB HARDWARE SPECIFICATIONS

GENERAL SPECIFICATIONS
1. Size—12.75 x 9.75 x 4.5 inches (stackable)
2. Finish—lacquered birch
3. Weight—5.5 pounds
4. Power requirements—50 or 60 Hz, 105 to 120 volts ac
5. Power switch—toggle on display panel

ELECTRONIC LOGIC SPECIFICATIONS
1. Functions available:
   8 Master-slave J-K flip flops
   8 2 input NAND gates
   6 3 input NAND gates
   4 4 input NAND gates
   4 AND/NOR gates (Exclusive OR or Half-Adders)
2. Type of circuit:
   7400 Series IC's using Transistor-Transistor Logic
3. Logic levels:
   HIGH—+5 volts nominal (+2.4 volts lowest)
   LOW—Ground nominal (0.0 to 0.4 volt)
   Internal Supply Voltage: +5 volts available at HIGH terminals of LOGIC PANEL.
4. Input Loading:
   Unit Load: 1 TTL Load = 1.6 mA at ground. +40 μA at +3 volts. Gate inputs and Flip-Flop J and K inputs present one unit load. Flip-Flop Clock and Reset (C & R) inputs represent two unit loads each.
   Lamp inputs present one unit load each.
5. Output Drive:
   The fan-out of an output indicates the number of unit loads that output can drive. Logic ouputs on the LOGIC PANEL have a fan-out of 10. (They will each drive 10 unit loads.)
   Pulsers and clock have a fan-out of 10.
   Toggle switches and HIGH outputs have an unlimited fan-out.

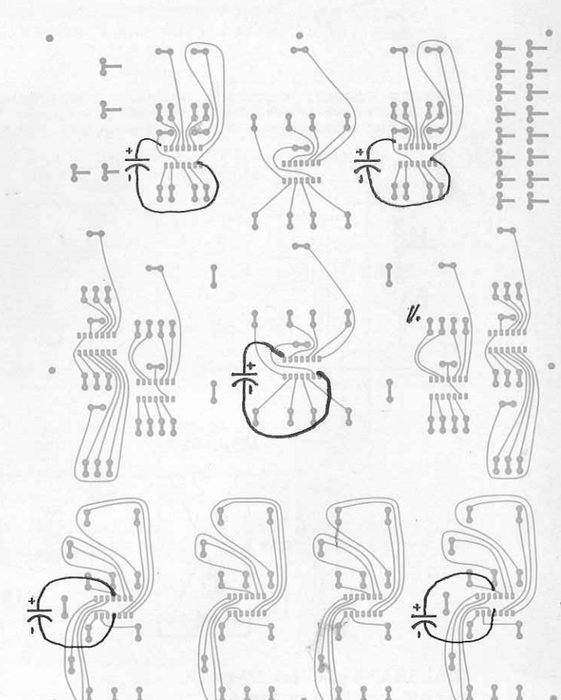
CONTROL AND INDICATOR SPECIFICATIONS
1. Functions available:
   8 toggle switches to generate steady-state logic levels.
   2. pulser switches
   8 lamps used as indicators
   Variable frequency clock
2. Toggle switches:
   Give a HIGH output when toggle is up.
   Give a LOW output when toggle is down.
   Fan-out: limited only by power supply
3. Pulser switches:
   Normally provide a HIGH output.
   LOW output when depressed, remains LOW until released.
   Fan-out: 10 unit loads
   Latches prevent noise from switch bounce.
4. Lamp indicators:
   Normally ON with no input. Can be turned OFF by "daisy-chaining" unused lamps to ground.
   ON when corresponding input is HIGH.
   OFF when corresponding input is LOW.
   LOAD: 1 unit load each.
5. Clock:
   Repetition rate: LO and HI (with each variable)
   Fan-out: 10
   Output: Square wave





TYPE AND LOCATION (top left). The 7473's have their notches pointed up; all others point down.

THE NEXT STEP (bottom left) is to add the ground leads as shown in this figure.



POWER WIRING (top right) on logic panel. Black overlay shows points to be connected with jumpers.

TANTALUM CAPACITORS (bottom right) are wired into position as shown in the black overprint.

allow you to check out the computer lab completely and also give you an opportunity to learn a little of how it works and how the experiments will be detailed in later material.

Logic levels

The computer lab uses positive logic definitions throughout. This means that a more positive voltage (up to 5 volts) will represent a logical "1" and a more negative voltage (ground or almost 0 volts) will represent a logical "0".

These levels are available from several sources. On the LOGIC PANEL, the terminals labeled HIGH are 5 volts or logical "1". The terminals labeled LOW are ground or logical "0".

The DISPLAY PANEL toggle switches have two positions. In the DOWN position, the switch output on the LOGIC PANEL will be grounded (logical "0"), and in the UP position it will have +5 volts as an output or logical "1".

Pulser switches

Two pulsers are provided on the display panel. The output of these pulsers appears on the logic panel terminals labeled PULSER. The output of these terminals is normally HIGH. Pressing one of the switches drives the corresponding output terminal to a LOW level for as long as the switch is depressed. When the switch is released, the output goes back to HIGH.

A NOR gate latch is part of the circuitry and insures that even though the contacts of the switch may bounce, the output from the pulser circuitry, once it has made the transition to the new level will remain at that level. The toggle switches are not provided with this type of circuitry.

The configuration was chosen because these pulsers will normally be used as clock inputs to flip-flops which require a negative going transition to cause them to change state. A positive going pulse can be obtained by feeding the pulser outputs through an inverter as will be described later.

Pulses

A pulse is a signal voltage that goes from one more or less steady level to its opposite level for a short period of time and then returns to its original level.

A pulse that goes from a LOW level (logical "0") to a HIGH level (logical "1") and back to a LOW level is called a POSITIVE, HIGH or "1" pulse.

A pulse (as with the pulsers) that goes from a HIGH level to a LOW level and back to HIGH is a NEGATIVE, LOW or "0" pulse.

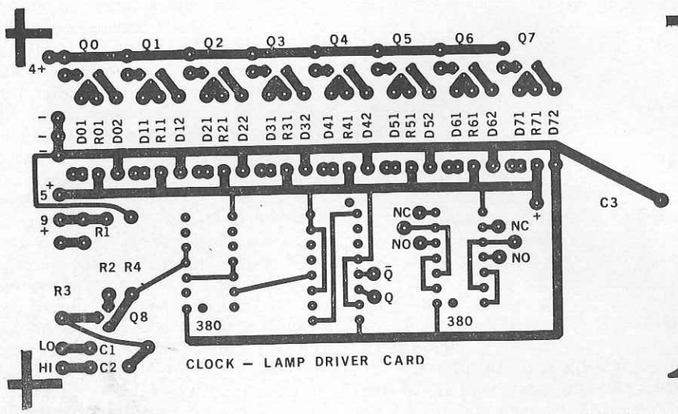
Every computer needs a clock. The computer lab is no exception. Unlike the computer lab, however, computer clocks usually run in the megahertz range. The lab clock frequency can be varied from about 1 Hz to several hundred Hz with the toggle switch in the LO position, and from several hundred to several thousand Hz in the HI position.

After a great deal of consideration, the very high and intermediate frequencies were left out. The lab will be used in two basic modes. In the first mode, all outputs and inputs will be monitored with the lamps. For this reason, high frequencies are unnecessary. It would be impossible to follow lamp transistions at more than a few hundred cycles per second even when using a long chain divider.

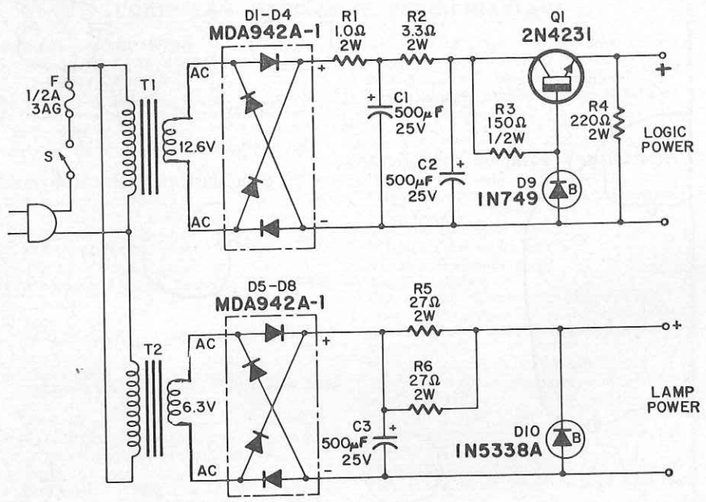
The HI frequencies were chosen to supply stable oscilloscope displays even with long chain dividers.

The clock also outputs logic compatible square waves instead of pulses which along with the adoption of only two basic frequency levels makes the clock inherently less expensive than similar systems. If necessary, the output of the clock can be made a pulse with circuitry that will be described in appropriate experiments.

The operation of all experiments



PRINTED CIRCUIT PATTERN for the clock-lamp driver circuit. This pattern is shown actual size and can be copied directly. Complete boards are available from Southwest Technical Products, 219 Rhapsody, San Antonio, Texas.



NOTES:
IN5338A – 5 WATT 5.1V ZENER
IN749 – 400mW 4.3V ZENER
MDA942A-1 – 1.5A 50V BRIDGE
2N4231 – 2A 35W NPN POWER

POWER SUPPLY is not built on a circuit board. This supply provides regulated dc to the logic circuitry. A separate section of the supply provides power to the lamps. This dc supply uses a Zener diode to regulate the lamp supply at 5.1 volts.

with the lab can be monitored with the lamps. By keeping the frequency low, all of the experiments will change conditions slowly enough to allow the lamps to respond. A lamp will light if its corresponding input is high and will be off if the corresponding input is low. With no connection, the lamp will be on. This configuration saves money and it is easy to put all lamps out as was demonstrated in the testing section.

Unused inputs

Although all of the literature associated with 7400 Series logic suggests that all unused inputs to gates, flip-flops and other elements should be tied to a HIGH level, this is not completely necessary for low frequency operation. The logic circuit, because of its input characteristics, treats an open (unconnected) input as a logical "1" or HIGH level and will operate satisfactorily for almost all low frequency applications. Should the experiment give improper results, connect all unused inputs to a HIGH level before deciding that something is wrong with the IC's or other circuitry.

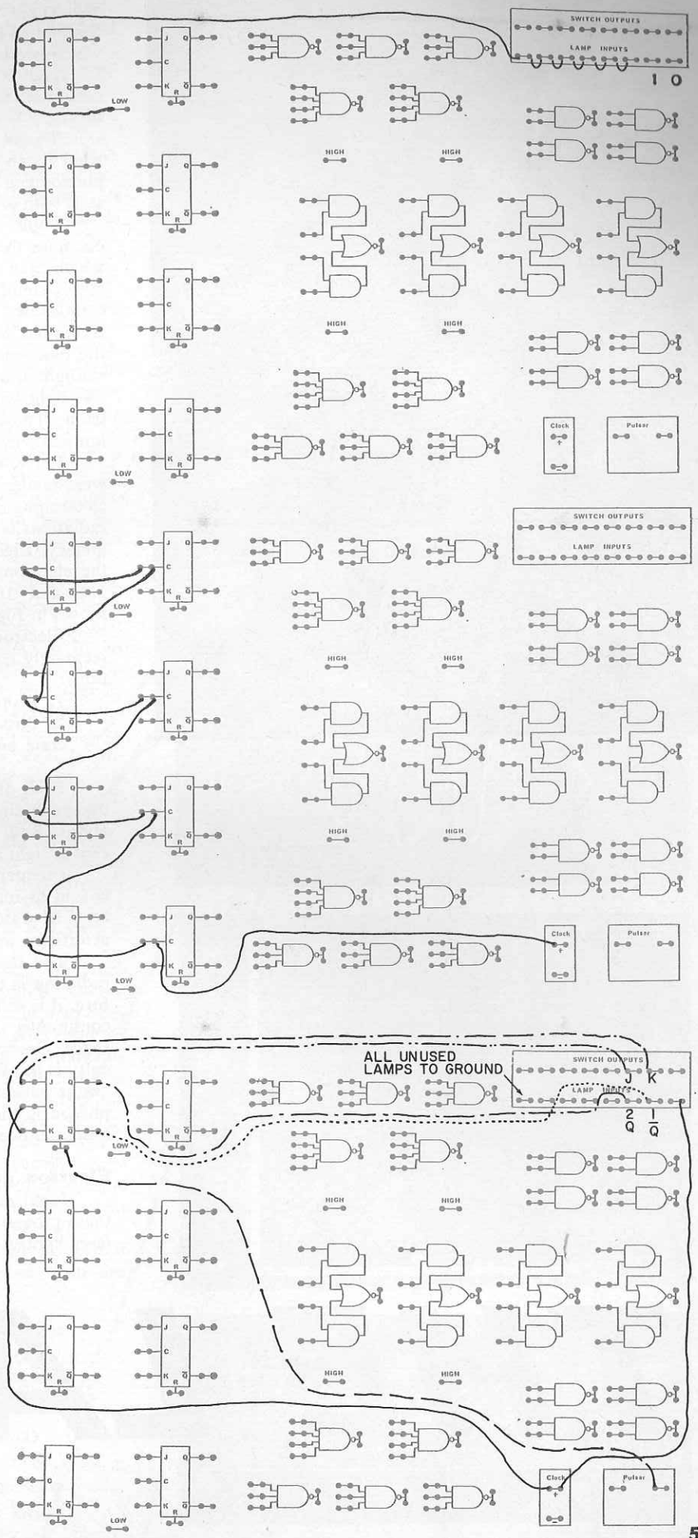
Building larger systems

Two labs can be used together (or more if desired) to build larger logic systems. An even better approach might be to obtain additional logic panels and a heavy duty power supply. In this way it would not be necessary to duplicate the lamps, switches and clock circuitry each time extra logic was required (unless these were also necessary). The only connection that *must* be made between logic panels or additional labs is a ground connection. Simply run a jumper from the LOW terminal on one panel to the LOW terminal on the other panel or panels.

Logic lab wiring

Wiring on the LOGIC LAB is done using a technique called "daisy chaining". If more than two outputs are required from the clock + side, for example, connect one of the clock + outputs to the first flip-flop C input. Run a lead from this C terminal to the next flip-flop C terminal and so forth. In this way, any number of inputs can be supplied from a single output terminal. **R-E**

(Experiments start next month)



LAMP INPUTS (top) chained together to ground turn off the corresponding lamps.

DAISY CHAINING (center) flip-flop "C" inputs from a single clock output.

TESTING FLIP-FLOPS (bottom) is more elaborate than testing other sections.