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FOR MEN WITH IDEAS IN ELECTRONICS

EXPERIMENT WITH A $32 SOLID-STATE LASER

4-CHANNEL STEREO
Speaker Setups
Sansui Matrix

USING OP-AMPS
6 Circuits to try
How they work

BUILD
TRANSISTOR
CURVE TRACER

IC KEY OPENS
ELECTRONIC
DOOR LOCK

R-E's
APPLIANCE
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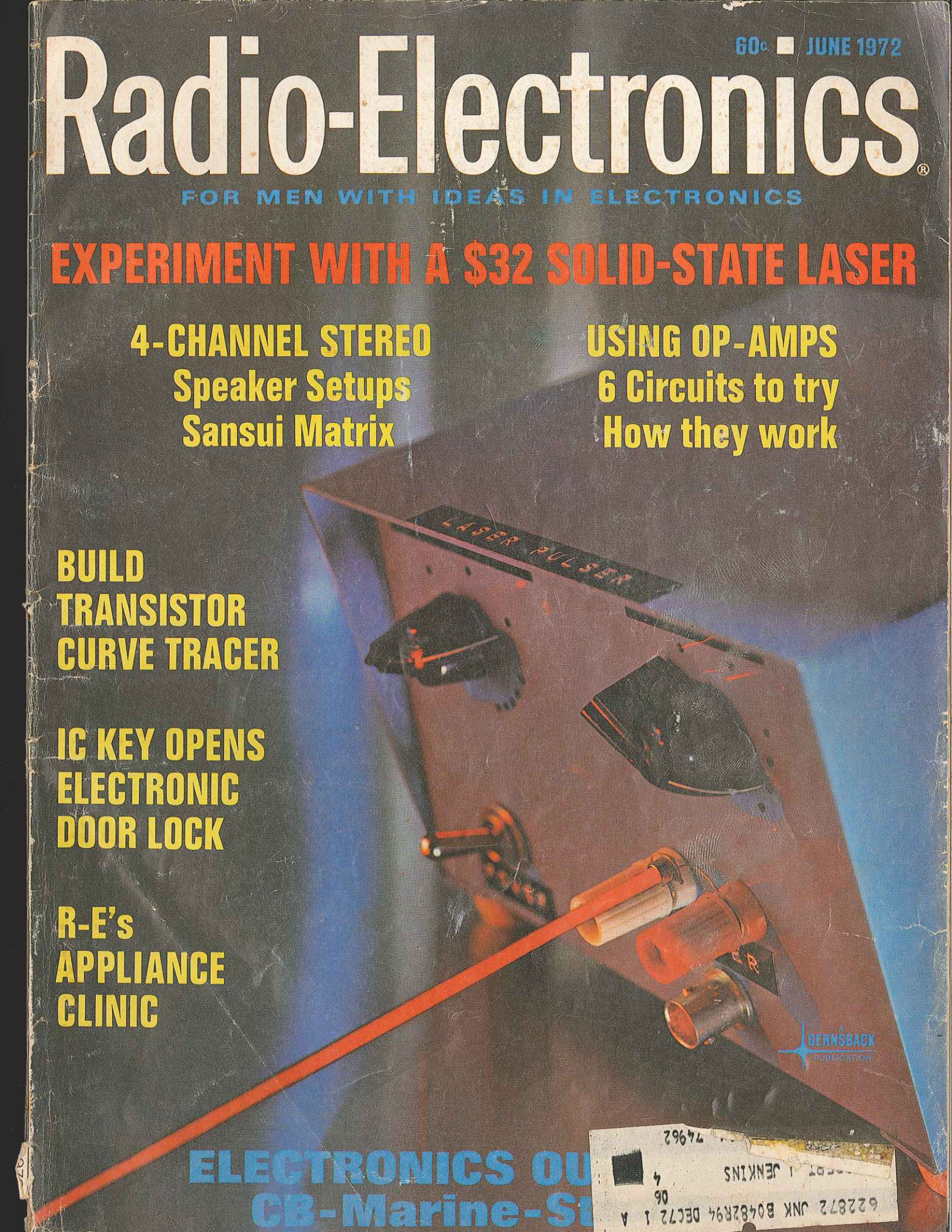

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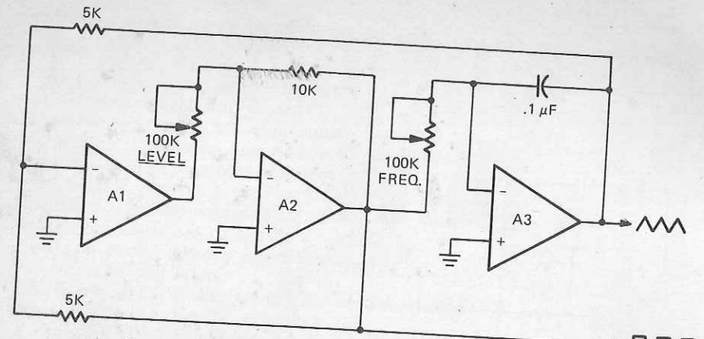


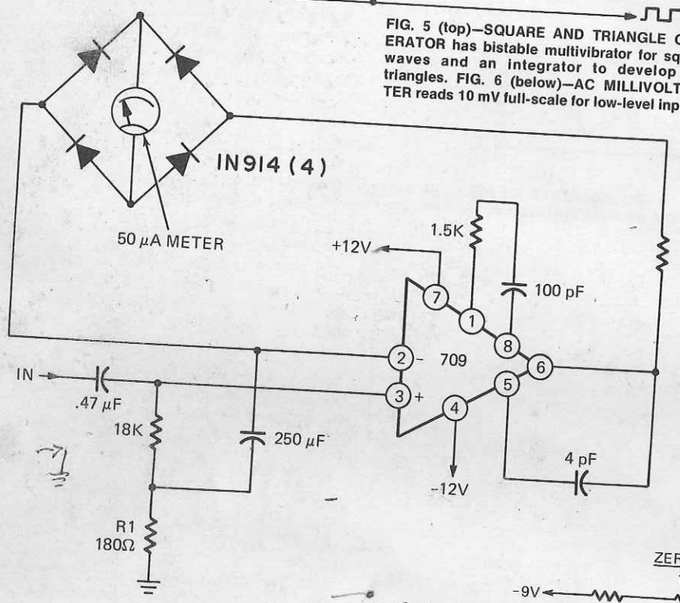


FIG. 5 (top)—SQUARE AND TRIANGLE GENERATOR has bistable multivibrator for square waves and an integrator to develop the triangles. FIG. 6 (below)—AC MILLIVOLTMETER reads 10 mV full-scale for low-level inputs.

clean triangle waveform. Any op amp will do, and if a 709 is used, don't forget the compensation (see other schematics for typical values). No value is given for C1 so use a switched set of values that will produce a clean triangle wave output with the selected square-wave inputs.

Combined generator

If you want to build a combination square and triangle waveform generator, then use the circuit of Fig. 5. A1 and A2 form a bistable circuit generating square waves. A3 is an integrator that forms the triangle waves. Both the frequency and level of the signals can be controlled by the potentiometers.

Sine-wave generator

The op-amp sine-wave generator shown in Fig. 4 can drive 8- to 10-ohm loads and can provide up to 8 volts output. Harmonic distortion is typically less than 0.5% over the frequency range. The lamp provides automatic gain control, while R1 provides the necessary feedback, and to a limited degree, determines the output amplitude. The frequency is equal to $\frac{1}{2\pi}$R2C1. The 47-pF capacitor between pins 8 and 6 provides the high-frequency compensation.

Working with solid-state circuits often calls for measuring very small signal levels. The circuit of Fig. 6 shows a 10-mV (.01-volt) full-scale ac millivoltmeter. Suitable attenuators can be used to change the measurement range. The use of input bootstrapping raises the input impedance to over one megohm. Resistor R1 has to be trimmed for full-scale deflection with 10-mV input. Accuracy is 2% and frequency range is within 3 dB to 150 kHz.

As another example of op-amp use in measuring circuits, that shown in Fig. 7 is a low-voltage-drop microammeter that will operate between 10-μA and 100 mA with an accuracy of 1% if a decent meter and accurate resistor values are used. Variation of accuracy with temperature is approximately .2% /°C.

The circuits shown are only a very small sampling of some of the unique uses of the op amp in test equipment. In future issues we will show you how to make a two op-amp circuit that forms a multimeter with twelve voltage ranges from 0.001 volt full scale to 300 volts full scale, twelve current ranges from 1 μA full scale to 300 mA full scale. Battery powered (two conventional 9-volt transistor radio batteries), this multimeter will be the equal of one selling at many times its construction cost. **R-E**

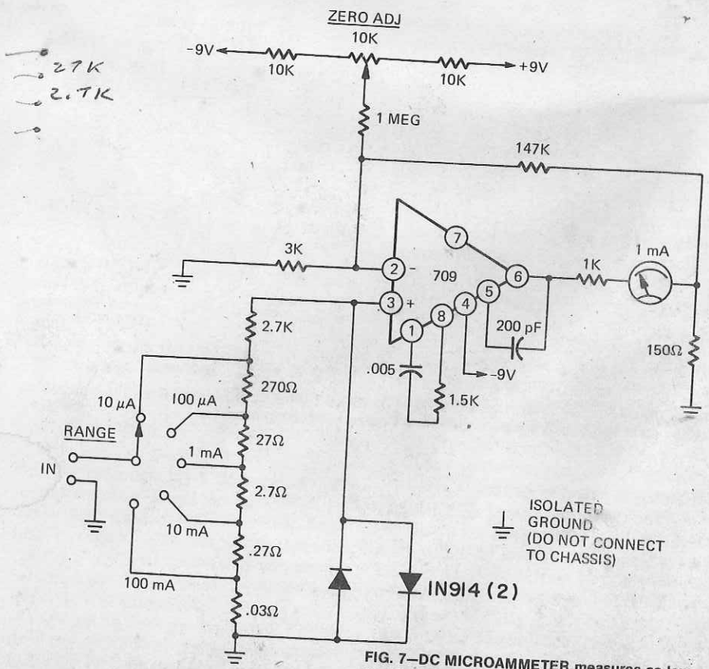


FIG. 7—DC MICROAMMETER measures as low as 10 μA full scale with very low voltage drop.

If you built R-E's digital IC tester last month you must be ready to put it to work. Here's a detailed manual of operation

how to use R-E's IC Tester

by JACK CAZES

NOW THAT YOU'VE COMPLETED THE construction of your DIGI-DYNA-CHECK **(Radio-Electronics,** May 1972), let's see how it can be used for both in- and out-of-circuit testing of a wide variety of digital integrated circuits. By simulating actual operating conditions for the unit under test; the DIGI-DYNA-CHECK performs a functional check of an ic under truly dynamic conditions. Operating power is supplied (+5 volts at 1 amp, regulated), where necessary and logic levels are readily applied to the inputs of the IC under test. All input and output logic levels are monitored, *simultaneously,* with a bank of sixteen indicator lamps, a lighted lamp representing a **1** logic state. A lamp that is off is indicative of either a **0** logic state or an indeterminate condition that is possible when there is no connection at that test terminal.

Gates of all types can be put through their paces by checking the output levels that result from various combinations of input levels. Flip-flops, counters, and shift-registers are advanced through their various states either stepwise (manually), or continuously (automatically) at a frequency of approximately 50 kHz, a rate that can be easily observed with most commonly used oscilloscopes.

Before we get into the actual examples of test procedures that can be used with different types of digital IC's, let's take a closer look at the matrix switch to learn the how and why of its operation. Since it's the heart of the DIGI-DYNA-CHECK, a thorough understanding of its operation is necessary.

The matrix switch consists of twenty 10-position slide switches, each having, in addition to ten *common* positions, a neutral or "no connection" position. The first sixteen sliders are wired to correspondingly numbered pins of the DIP (Dual-Inline Plastic) test socket and to the inputs of sixteen lamp indicators. The remaining four sliders are brought out to four binding posts marked **W, X, Y,** and **Z.**

Each of the ten switch positions is wired, internally, in common, for all 20 switches, to the following functions. See Table I on next page.

Looking at Table I, we see that any number of the sixteen IC contacts as well as binding posts **W, X, Y,** and **Z** can be connected to any of the six internally available functions by merely moving their corresponding matrix sliders to the positions representing the desired functions. Since all switches have their identically numbered positions wired in-common (bussed together), two or more sliders resting on the same numbered positions will result in their IC terminals and/or binding posts being connected together. Sliders **W** through **Z** and positions **A** through **D** form a 4 × 4 matrix with their eight binding posts which, as we shall soon see, can be useful in connecting the test IC to the outside world—to a scope, external power supplies, resistors, capacitors, test leads, etc. When any or all of the sliders **W** through **Z** are in positions **1** through **6,** the corresponding internal functions are available for external use. This can come in handy when checking external circuitry. Note that when sliders **1** through **16** are in positions **A** through **D,** the corresponding monitor lamp inputs are automatically connected to the external binding posts.

Thus, for example, with slider **1** in position **A,** and test leads plugged into binding post **A** and ground, lamp **1** can be used as a logic level test probe for checking relative logic levels on PC boards at locations other than at IC terminals.

The numbering system for DIP integrated circuits is illustrated below. Very often, there is some sort of mark, such as a dot or a number 1 at pin 1. However, even in cases where there is none, pin 1 will always be at the notched end of the IC package as shown in Fig. 1. The remaining pins are numbered counting counterclockwise.

POSITION	TABLE I WIRED TO
0	No connection (Neutral)
1	Ground (to provide circuit common and logical **0**)
2	+5V, regulated (to provide circuit power and logical **1**)
3	STEP (via manual stepping button)
4	$\overline{\text{STEP}}$ (complement of position 3)
5	INT CLOCK (internally available 50 kHz square-wave generator)
6	$\overline{\text{INT CLOCK}}$ (complement of position 5)
7	Binding post **A**
8	Binding post **B**
9	Binding post **C**
10	Binding post **D**

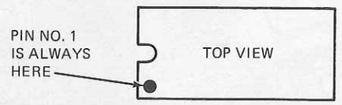


FIG. 1—FINDING PIN 1 of a dual-inline-package (DIP) IC is easy. Just look for the notch in one end as shown here.

In-circuit testing

To test IC's in-circuit plug the in-circuit adapter cable into the test socket of the DIGI-DYNA-CHECK and connect the test clip at the other end of the cable to the IC to be checked. Be sure that the clip is properly oriented, i.e., with IC pin 1 connected to the 1 position of the clip. *A ground connection must* be made between the circuit being tested and the checker to provide a common reference point for the lamp monitors. This can be done either by moving the matrix slider corresponding to the ground lead of the IC under test (if this is known) to GND (position 1), or by connecting a clip lead between one of the ground posts in the checker and a ground or common point on the board containing the IC being tested.

If the IC being checked is operating under its own power supply, the logic levels existing at all of its terminals will be displayed by the indicators directly. If the circuit is not self-powered, power can be supplied from the DIGI-DYNA-CHECK to the V_{cc} terminal of the IC via the matrix switch. Since up to 1 amp is available, the checker's power supply can "fire-up" a board containing many IC's; most digital IC's draw only a few milliamps each. However, current drain for most integrated circuits is dependent upon the output states and how often these states are changing—frequency. This happens because many gates draw extra current while changing state. Most manufacturers specify a maximum current consumption, and their literature should be consulted when in doubt.

One more word of **CAUTION** about using the internal +5 V supply for powering integrated circuits. The internal supply can only be used with IC's that are designed to operate at +5 volts. RTL (Resistor-Transistor Logic) circuits, for instance, require 3.6 volts and can be damaged if connected to 5 volts. RTL units operating from their own power supply or from an external power source of the proper voltage *can,* nevertheless, be checked with the DIGI-DYNA-CHECK via the lamp monitors because their logic threshold region is within the threshold region of the lamp-driver circuits. A knowledge of what the logic states at the IC's terminals should be for a given circuit may be obtained from the spec sheets for the units under test.

It is possible, during in-circuit testing, to connect any of the internally available functions to the circuit under test. Thus, you can connect the STEP or CLOCK function to the input of a shift register, or a counter, or a flip-flop, and carry it through its paces under control of the DIGI-DYNA-CHECK. You can connect up to four IC terminals simultaneously (via positions **A** through **D**), to external components, or to a scope for monitoring input and output relationships.

Out-of-circuit testing

Out-of-circuit IC testing is performed much the same way as is done with a tube tester. The unit to be tested is plugged directly into the test socket, suitable input parameters are set (in the present case, via the matrix switch), and the result is read out on the front panel. In our case, we do not merely get a GOOD-?-BAD reading as with a tube tester, but rather, we obtain a lot more information about the IC under test. We are able to monitor all input and output logic levels *simultaneously,* and to compare them with each other and with expected levels based upon either a prior knowledge of the normal mode of operation of the logic type involved, (gate, counter, flip-flop, shift register, etc.) or from literature describing the specific unit being tested in which the normal input/output relationships are given. This latter type of data is generally contained in a TRUTH TABLE. This table indicates what the outputs should look like when certain combinations of input levels are present as well as what changes should occur when changes are made in the input levels.

Gates are the most basic logic systems. They can have, generally, either of two output states: a *high* or **1** level and a *low* or **0** level. The level or state that is present at the output of a particular gate depends upon the condition of the input(s) to the gate. The simplest gate, the INVERTER, or NOT gate always has an output state that is the opposite of its input (it has only one output and one input); a **1** at its input results in a **0** at its output, and vice versa.

Let's briefly look at truth tables for some of the more common types of logic building blocks (basic logic circuit types). The following table is a combined truth table for two-input NAND, AND, NOR, OR, and EXCLUSIVE-OR gates:

INPUTS		OUTPUTS				
A	B	NAND	AND	OR	NOR	EXCL-OR
0	0	1	0	0	1	0
0	1	1	0	1	0	1
1	0	1	0	1	0	1
1	1	0	1	1	0	0

Some generalizations may be made:

- For the first four types of gates, the output is at one condition for all input combinations *except one.*
- The NAND outputs are the opposite or inverse of the AND outputs for a given set of input conditions.
- The NOR outputs are the opposite or inverse of the OR outputs for a given set of input conditions.
- The EXCLUSIVE-OR gate is at one state if both inputs are identical and in the opposite state if the inputs are different. This property of the EXCLUSIVE-OR gate makes it useful as a digital comparator—for comparing two digital quantities or two digital states with each other.

Similar truth tables and general observations can be made for gates containing more than two inputs; the number of input combinations, of course, increases with the number of inputs involved.

Flip-flops represent the next most complex systems in digital circuitry. One widely used type is known as the J-K flip-flop. Unlike simple gates discussed above which have no memory, *flip-flops remain in a given state even after the input conditions that put it into that state have been removed.* Flip-flops often have two complementary outputs known as **Q** and **not-Q** (written $\overline{Q}$). A J-K flip-flop has a "clock" input that serves as the trigger for the device. Output states are made to change by applying a pulse at the clock terminal. The states assumed by the **Q** and $\overline{Q}$ outputs depend upon the levels present at the **J** and **K** inputs immediately preceeding the clock pulse as well as the states of the **Q** and $\overline{Q}$ outputs at that time. The normal transitions are summarized in the next table.

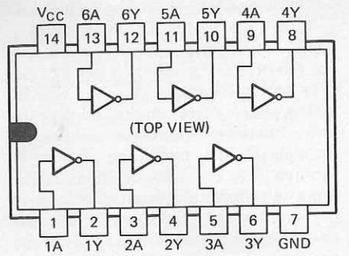
At time, *t*		At time, *t* + 1	
J	*K*	*Q*	$\overline{Q}$
0	0	No change in state (maintains whatever state was present at time, t)	
1	0	1	0
0	1	0	1
1	1	Assumes the inverse of the output states that were present at time, *t*	

NOTE: *t* is the time just before the "clock" pulse.
t + 1 is the time just following the "clock" pulse.

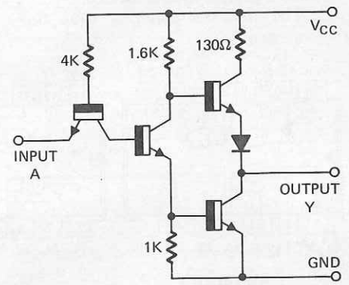
Now we're ready to apply what we've learned about the basic digital logic building blocks to checking digital IC's with the DIGI-DYNA-CHECK. We will select several IC's and carry them through their tests. The following table lists some of the more commonly used TTL (Transistor-Transistor Logic) integrated circuits with their internal terminal connections. We will look at several units listed in the table in order of increasing complexity, including an INVERTER, NAND, NAND with open-collector outputs, J-K flip-flop, and, finally, a **decade counter.**

TABLE II

Pin No.	Set to	Remarks
7	GND	Power supply to the IC
14	+5 V	
1, 2	+5 V	Inputs to gate 1 at logical "1"
4, 5	+5 V	Inputs to gate 2 at logical "1"
9, 10	+5 V	Inputs to gate 3 at logical "1"
12, 13	+5 V	Inputs to gate 4 at logical "1"



SN7404



SCHEMATIC (EACH INVERTER)

FIG. 2—THE SN7404. Basing diagram is at the top. Schematic of each inverter is also shown. There are six in this IC.

SN7404: Hex inverter

This 14-pin IC contains six separate inverters with their inputs and outputs wired as shown in the table below and in Fig. 2. Plug it into the test socket making certain that it is properly oriented, with its pin **1** in hole **1** of the socket. Connect pin **7** to GND and pin **14** to +5 V by moving matrix sliders corresponding to these pins to the positions indicated. This will provide operating power to the IC. Now set the sliders for terminals **1, 3, 5, 9, 11,** and **13** (the six inputs) to +5 V (logical **1**) and note the conditions of the lamps. All lamps corresponding to terminals that are connected to +5 V should be on (**1**) whereas all lamps corresponding to output terminals (**2, 4, 6, 8, 10,** and **12**) should be off (**0**); we have already seen, in our discussion of gates, that INVERTER outputs should maintain states that are the inverse of their inputs. Try other combinations of input states and note that, if the IC is operating properly, all outputs will be the inverse of their respective inputs.

Thus, we can check the entire integrated circuit at the same time . . . all six inverters, simultaneously.

SN7400: Quad two-input nand gates

This IC contains four two-input NAND gates on a single chip. Here again, we will perform tests on all parts of the unit simultaneously. Plug the circuit into the test socket, properly oriented. The truth table for each of the four NAND gates is as was given earlier. Make the initial settings as per Table II at the left.

All input lamps should be at logical **1** (on) and all outputs should be at logical **0** (see truth table for a NAND gate).

Now change the settings for the in-

NUMBER/TYPE	PIN NUMBERS															
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	
SN7400-QUAD 2-IN NAND GATE	IN 1A	IN 1B	OUT 1	IN 2A	IN 2B	OUT 2	GND	OUT 3	IN 3A	IN 3B	OUT 4	IN 4A	IN 4B	VCC	——	——	SN7400
SN7401-QUAD 2-IN NAND-O/C GATE	OUT 1	IN 1A	IN 1B	OUT 2	IN 2A	IN 2B	GND	IN 3A	IN 3B	OUT 3	IN 4A	IN 4B	OUT 4	VCC	——	——	SN7401
SN7404-HEX INVERT GATES	IN 1	OUT 1	IN 2	OUT 2	IN 3	OUT 3	GND	OUT 4	IN 4	OUT 5	IN 5	OUT 6	IN 6	VCC	——	——	SN7404
SN7430-8-IN NAND GATE	IN A	IN B	IN C	IN D	IN E	IN F	GND	OUT	N/C	N/C	IN G	IN H	N/C	VCC	——	——	SN7430
SN7442-4 TO 10 BCD DECODER	OUT 0	OUT 1	OUT 2	OUT 3	OUT 4	OUT 5	OUT 6	GND	OUT 7	OUT 8	OUT 9	IN D	IN C	IN B	IN A	VCC	SN7442
SN7473 DUAL J-K M-S FLIP-FLOPS	CLK 1	CLR 1	K 1	VCC	CLK 2	CLR 2	J 2	NQ 2	Q 2	K 2	GND	Q 1	NQ 1	J 1	——	——	SN7473
SN7474-DUAL D-EDG TRIG FLIP-FLOPS	CLR 1	D 1	CLK 1	PRE 1	Q 1	NQ 1	GND	NQ 2	Q 2	PRE 2	CLK 2	D 2	CLR 2	VCC	——	——	SN7474
SN7480-GATED FULL ADDER	B*	B c	C n	NC n+1	SUM	NSUM	GND	A 1	A 2	A*	A C	B 1	B 2	VCC	——	——	SN7480
SN7486-QUAD 2-IN EXCL-OR GATES	IN 1A	IN 1B	OUT 1	IN 2A	IN 2B	OUT 2	GND	OUT 3	IN 3A	IN 3B	OUT 4	IN 4A	IN 4B	VCC	——	——	SN7486
SN7490-DEC CNTR-DIV BY 2+5	IN B-D	RST 0-1	RST 0-2	N/C	VCC	RST 9-1	RST 9-2	OUT C	OUT B	GND	OUT D	OUT A	N/C	IN A	——	——	SN7490
SN7491-8 BIT SHIFT REGISTER	N/C	N/C	N/C	N/C	VCC	N/C	N/C	N/C	N CP	GND	IN B	IN A	Q	NQ	——	——	SN7491
SN7492-DIV 12-CNTR DIV BY 2+6	IN B-C	N/C	N/C	N/C	VCC	RST 0-1	RST 0-2	OUT D	OUT C	GND	OUT B	OUT A	N/C	IN A	——	——	SN7492

ABBREVIATIONS:
IN—INPUT
OUT—OUTPUT
GND—GROUND
VCC—SUPPLY VOLTAGE
CLK—CLOCK
CLR—CLEAR
Q—FLIP FLOP OUTPUT
NQ—INVERSE Q ("NOT" Q)
PRE—PRESET INPUT
N/C—NO CONNECTION
RST—RESET

puts to correspond to the other input combinations shown in the truth table for a NAND gate to see if the outputs conform to those given.

SN7401: Quad two-input nand gates with open collectors

Testing of these NAND gates is similar to that procedure already discussed above for the SN7400, except that these gates have open-collector outputs and require the addition of "pull-up" resistors to drive the indicator lamps. Pull-up resistors are normally connected between the outputs and +5 V. This is done in the DIGI-DYNA-CHECK as follows:

Move slider **W** to +5 V to bring +5 volts out to binding post **W.** Now, connect pins **1, 4, 10,** and **13** (the NAND gate outputs) to binding posts **A** through **D,** respectively, via their matrix sliders. You can now connect the required resistors (approx. 1000 to 4000 ohms).

Connect V_{cc} and ground and set the inputs as before (for the SN7400) observing the proper terminal connections for the SN7401, and carry the gates through their various input combinations as before.

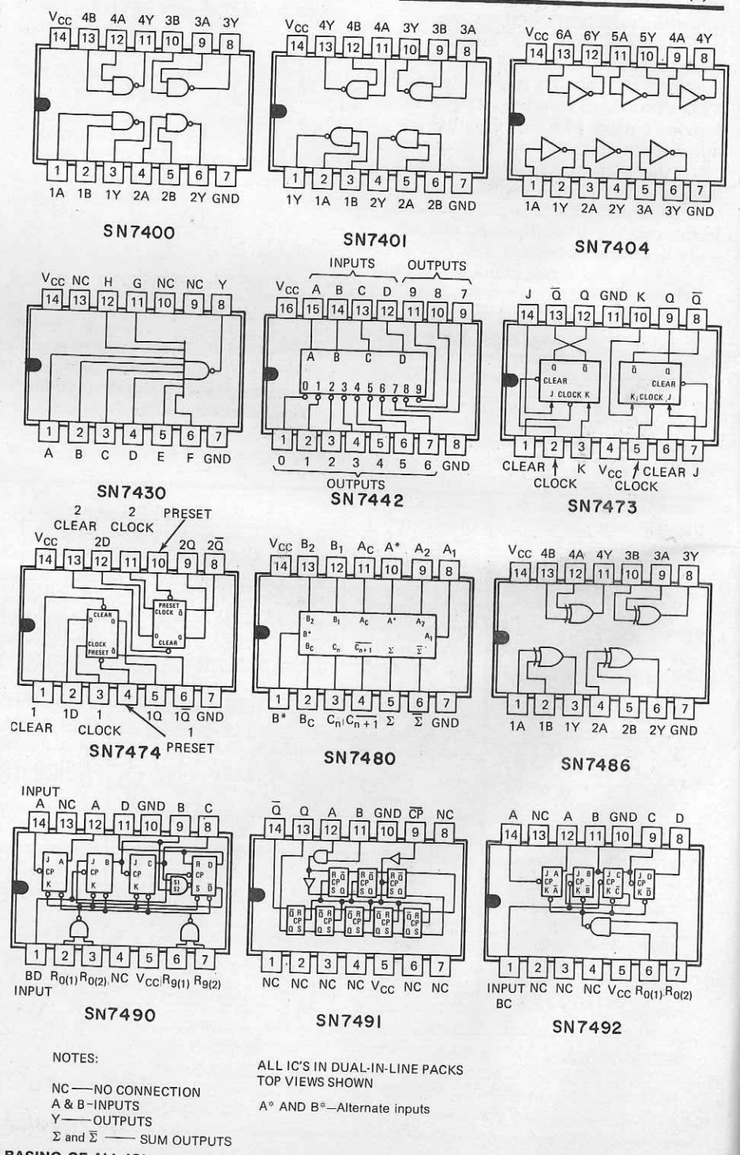
SN7473: Dual J-K flip-flops

This integrated circuit contains two complete J-K flip-flops in a single package. For the sake of simplicity, and since both flip-flops operate identically, we will only go through the tests for one of them. After the IC has been properly inserted into the test socket, connect pin 4 to +5 V and pin 11 to GND to supply operating power to the circuit. Let's go through a manual test, first. Set pin 1 (CLOCK input) to the STEP position and pins 14 (**J**-input) and 3 (**K**-input) to one of the combinations shown in the truth table for a J-K flip-flop. Momentarily connect pin 2 (CLEAR) to GND and then to +5 V and leave it there. This is done to clear it, i.e., bring it to an initial state. Enter a "clock" pulse, manually, by depressing the STEP button one time only and releasing it. The outputs, **Q** and $\overline{\mathbf{Q}}$, should react according to that which is given in the truth table for the particular combination of **J** and **K** inputs that you have entered. Clear the flip-flop again by momentarily grounding the CLEAR input (pin **2**) and returning it to +5 V. Set the **J** and **K** inputs (pins **14** and **3,** respectively) to a different combination of logic states and then enter a clock pulse. Check the result once again and compare it with the truth table. Try the other two J-K combinations, referring, again, to the table. You can also try entering several clock pulses for the **1, 1** combination of J-K inputs. The outputs should oscillate back and forth between two states. The second flip-flop in this IC can be checked out in a similar manner, either separately, or simultaneously with the first one, as above.

To operate the flip-flops automatically, at a rate of 50 kHz. for monitoring input/output relationships with a scope, use the INT CLOCK setting instead of the STEP setting for the clock input. Set the matrix sliders corresponding to the output terminals of interest to positions **A** through **D** and move the sliders **W** through **Z** to the same positions as the input terminals of interest and connect the scope to the binding posts. For every two clock pulses, you should see one square-wave pulse at either of the two outputs. The two outputs (**Q** and $\overline{\mathbf{Q}}$) should be 180° out of phase. A flip-flop is, thus a divide-by-two device.

The SN7490 contains four flip-flops that are internally wired to form separate divide-by-two and divide-by-five counters. These can be operated either separately with their own individual inputs and outputs, or they can be wired, externally, together as a single divide-by-ten (decade) counter by connecting the output terminal of the divide-by-two section to the input terminal of the divide-by-five section and using input A (to the first flip-flop) as the decade input. When it is operated in this mode, the outputs are in BCD code; the four outputs have the values:

Output:	A	B	C	D
Value:	2^0 (1)	2^1 (2)	2^2 (4)	2^3 (8)



BASING OF ALL IC's listed in the table on the preceding page. You'll want these diagrams handy when you set up your IC tester to check out any of these units.

Thus the BCD-coded output of the decade counter is represented by the following conditions of the four flip-flop outputs:

Number	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

When the unit has counted ten input pulses, it automatically resets itself to zero and starts again. Let's now see how this IC is tested with DIGI-DYNA-CHECK.

1. As separate ÷2 and ÷5 counters—

Make the following initial settings:

Pin No	Set to	Remarks
10	GND	To supply power to the IC
5	+5 V	
2	GND	This deactivates the reset inputs to permit the flip-flops to function
3	GND	
6	GND	
7	GND	
14	STEP	Input to the ÷2 counter
1	STEP	Input to the ÷5 counter

Momentarily move the sliders corresponding to pins 2, 3, 6, and 7 to +5 V, simultaneously, and then back to GND. This resets both counters to zero and allows input pulses to be counted. All output lamps should now be off (logical **0**). Depress the STEP button and release it to enter a single count pulse to both sections. Repeat this four more times, comparing the output logic states with those shown in the table above:

Lamp No	Input Pulses 1st	2nd	3rd	4th	5th	Remarks
12 (Output A)	1	0	1	0	1	÷2 counter
9 (Output B)	1	0	1	0	0	÷5 counter
8 (Output C)	0	1	1	0	0	÷5 counter
11 (Output D)	0	0	0	1	0	÷5 counter

2. As a single ÷10 (decade) counter—

Make the following changes in the matrix switch settings:

Move Pin No	to Position
1	A
12	A

Remarks

This disconnects input of the ÷5 unit from STEP and connects a jumper (bus A) between the ÷2 output and ÷5 input.

Reset all counters as described above and then enter ten pulses, noting whether the outputs correspond to the 0 thru 9 BCD code given earlier. Here again, as in our earlier discussion involving the flip-flop tests, the use of the automatic INTERNAL CLOCK function instead of the manual STEP function permits you to use a scope to monitor input/output logic states and waveforms.

Checking current drain IC

It's a simple matter, with the DIGI-DYNA-CHECK, to route +5 volts to the V_{cc} terminal of an IC, indirectly, via a pair of binding posts. An ammeter connected to the posts will then be in series with the power supply to the circuit and will indicate current drain. This is accomplished by moving one of the sliders **W** through **Z** to +5 V, thus bringing +5 volts out to a binding post. Moving the slider corresponding to the IC's V_{cc} terminal to one of the positions **A** through **D** will bring it out to a binding post. Current drain can be monitored continuously while performing other tests on the IC.

We have seen that there are many ways in which the DIGI-DYNA-CHECK can be used to test digital ICs. A complete description of all of its uses is beyond the scope of this article. The use of a matrix switch together with the input/output binding posts makes the checker *almost* universal. Any IC terminal can be connected to any function, either internally or externally. Where needed, special adapters can be made to accommodate package types other than 14- and 16-pin DIPs. Thus, you might say that the DIGI-DYNA-CHECK is as close to *obsolete-proof* as you can get!

The multitude of ways in which this tester can be applied to digital IC testing is limited only by your imagination! **R-E**

Many readers have already asked "Where do I buy parts to build my own Digital IC Tester, as described in the May 1972 issue?" The answer to that query was supposed to have appeared at the end of the parts list last month. As you must know by now, it did not. Therefore, we are presenting here, the listing that was omitted last issue:

The following kits of parts are available from The Electronetics Co. Inc., P.O. Box 278, Cranbury, N.J. 08512.

DDC-1 consisting of Q1 thru Q36; D1 thru D5; bridge rectifier; IC1; matrix switch and DIP test clip: $54.50, including postage and insurance.

DDC-2 consisting of a manual listing pin connections for many popular integrated circuits, useful for programming the DIGI-DYNA-CHECK: $2.00 including postage.

cb radio call light

CB transceivers are often installed on motorcycles, sports cars, snowmobiles and in countless other noisy locations. The high noise level may cause an operator to miss an incoming call. An article in *Electron* magazine (Toronto, Ont.) shows how a call light can be added to indicate that a signal is being received.

The circuit in Fig. 1 can be added to receivers that produce a negative-going voltage at the squelch output when a signal comes on the air. The lamp turn-on voltage depends on the setting of the squelch control. The indicator circuit can also be driven by the emitter voltage of an rf transistor if this voltage swings negative on an incoming signal. With this arrangement, the lamp comes on with a S4-S6 signal. The circuit in Fig. 2 can be used in sets where an incoming signal develops a positive-going voltage.

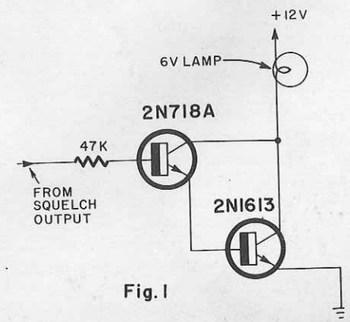


Fig. 1

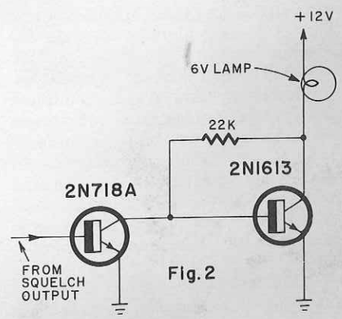


Fig. 2