computer corner

Z-80 *An in-depth look at the pin-out of the Z-80 IC and the Z-80's timing.* WILLIAM BARDEN, JR.

LAST MONTH'S COLUMN COMPARED THE Z-80 with the 8080 and discussed the Z-80's architecture. Now let's take a look at the pin-out of the Z-80 IC and the Z-80's timing.

Z-80 pin-out

Figure 1 shows the signal pin-out of the Z-80 IC. The Z-80 is implemented in a 40-pin dual in-line package. The 16-line address bus is designated A15 through A0. The external data bus is D7 through D0. A single-phase TTL-level clock input is at the ϕ pin. The input frequency is a nominal 2.5 MHz, producing minimum instruction times of 1.6 μs.

The $\overline{\text{RESET}}$ input initializes the CPU by zeroing the program counter, setting the I and R registers to zero, disabling interrupts by resetting the interrupt enable flip-flop, and setting interrupt mode 0 (to be discussed in a later column). Setting this signal to a zero logic level is the normal method to reset the CPU.

The $\overline{\text{RFSH}}$ (refresh) output informs external logic that the contents of the R counter is now on the address bus and that a refresh read of the dynamic memories can be done by means of the $\overline{\text{MREQ}}$ signal.

The $\overline{\text{MREQ}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals are tri-state outputs indicating a memory request for a read or write to the CPU. The address bus holds a valid address for the memory operation when $\overline{\text{MREQ}}$ is low (zero logic level), and either $\overline{\text{RD}}$ or $\overline{\text{WR}}$ is low. The $\overline{\text{WAIT}}$ signal is brought down to a zero logic level by the memory after $\overline{\text{MREQ}}$. The $\overline{\text{WAIT}}$ signal remains low until external memory is finished, enabling the CPU to interface to slower speed memory.

When output signal $\overline{\text{M1}}$ goes low, the CPU is in the operation code fetch cycle of instruction execution. If both $\overline{\text{M1}}$ and $\overline{\text{IORQ}}$ are low, an interrupt acknowledge cycle is in progress.

Output signal $\overline{\text{IORQ}}$ indicates that the address bus holds a valid I/O address for an I/O read or write (input- or output-type instruction). If $\overline{\text{M1}}$ is also low, an interrupt acknowledge cycle is in progress.

Input signal $\overline{\text{INT}}$ is an interrupt request. If the interrupt enable flag IFF is enabled (by software) and the $\overline{\text{BUSRQ}}$ signal is high, the interrupt is accepted and the $\overline{\text{IORQ}}$ signal is brought low during the $\overline{\text{M1}}$ signal to indicate an interrupt acknowledge to the interrupting I/O device.

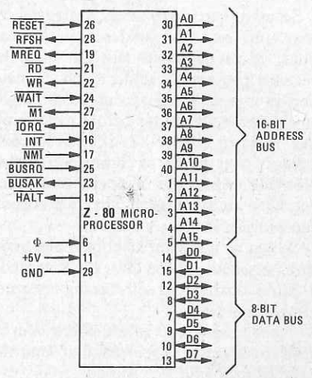


FIG. 1

Input signal $\overline{\text{NMI}}$ is triggered by a negative-going edge. The nonmaskable interrupt it produces cannot be disabled and is recognized at the end of the current instruction. Once received, $\overline{\text{NMI}}$ causes the CPU to restart to location 0066_{16} (described in a later column).

Input $\overline{\text{BUSRQ}}$ (bus request) requests the CPU to give up control of the address bus, data bus and control signals. When the CPU responds by bringing output signal $\overline{\text{BUSAK}}$ (bus acknowledge) low, those lines can be controlled by external logic for DMA (*D*irect *M*emory *A*ccess) or other uses. When the external device is finished, it brings up the $\overline{\text{BUSRQ}}$ line, giving control back to the CPU.

The $\overline{\text{HALT}}$ output indicates that the CPU has executed a halt instruction. An $\overline{\text{NMI}}$, I/O interrupt or control-panel action must occur before normal operation can resume. The halt instruction would normally be used either to wait for an interrupt or to halt program execution for an end-of-program condition or an error condition.

Z-80 timing

Execution of any instruction by the Z-80 CPU consists of a number of machine cycles, each (designated M) consisting of several basic clock cycles. The first machine cycle (M1) is always an operation code fetch and decode. Figure 2 shows the execution of the simple LD R,N instruction, which loads CPU register R with the eight-bit data value in the instruction.

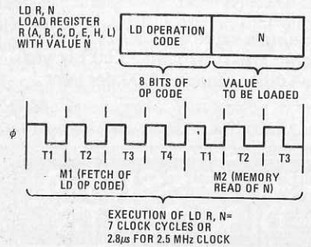
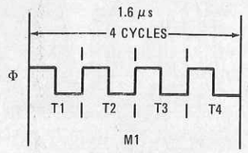


FIG. 2

The various instructions in the Z-80 take anywhere from 4 cycles (1.6 μs) to 20 cycles (8 μs), depending on the length and operations of the instructions. The simplest instruction is one in which only the op code was fetched from memory and the operation of the instruction could be completed during the M1 cycle. An example of this would be the one-byte instruction to complement the contents of the accumulator register CPL. (See Fig. 3.) The one's complement could be completed in the four clock cycles of T1 (1.6 μs).



CPL INSTRUCTION (FETCH OP CODE AND ONE'S COMPLEMENT A REGISTER

FIG. 3

Loading the A register with an eight-bit operand from memory requires a fetch (memory read) of the op code for the load operation, two memory reads of the memory address within the instruction, and one memory read of the operand, a total of four machines cycles or a total of 13 clock cycles (5.2 μs). (See Fig. 4.)

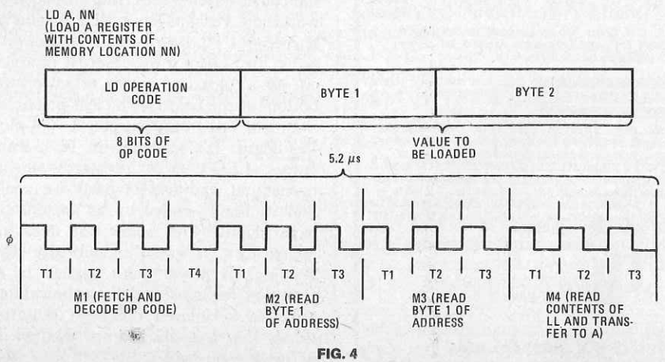


FIG. 4

All executive times might be lengthened if the CPU was interfacing to a slow memory.

The next column in this series will discuss the different types of instructions associated with the Z-80. **R-E**

Federal suit planned against Virginia radar detector laws

A New Hampshire resident's wife was recently arrested in Virginia for violating that state's anti-radar laws. Bill Edwards, a Hillsborough, NH, engineer and ad manager, is so incensed over what he deems to be a violation of due process that he plans to file a federal class-action suit against the state of Virginia.

Apparently, no other laws had been violated. His wife not only had her radar detector confiscated but was even required to supply the tools to remove it. No anti-radar law exists in New Hampshire.

The suit will charge violation of interstate commerce laws and federal preemption as well as seeking the return of all confiscated radar detectors seized during the two-year period of Virginia's anti-radar laws. Since approximately 5,000 such detectors have been taken from out-of-state drivers during this period, at an estimated cost of $100 each plus an average $100 fine per detector, Virginia could stand to lose a million dollars in damages alone, if the suit is successful.

FCC cartoon show sends a big 10-44 to all CB'ers

For those not in the know, "a big 10-44" is CB lingo for "I've got a message for you." In this case, the Federal Trade Commission's message is a 10-minute cartoon slide-and-sound show aimed at schools, clubs, and other interested associations; the purpose: to acquaint everyone with the importance of Citizens band rules and regulations.

The show, entitled "10-4 Uncle Charlie," features such CB characters as Rhinestone Cowboy, Earthmama, Bucketmouth and others. Included in the program are 72 slides, a 10-minute audio tape cassette, a script and a question-and-answer book designed to take care of the more common CB questions. The program can be purchased from National Audiovisual Center, General Services Administration, Order Section, Washington, DC 20409. The slide-show package costs $15.00.

IHF has big plans for the future

The image and the future of the Institute of High Fidelity (IHF) are both changing—for the better, thinks Bernie Mitchell, president of IHF. Some of the changes envisioned for IHF are: regularly scheduled meetings for manufacturers to discuss problems and exchange views; better communications tools to "sell the product" to potential buyers; and last, but not least, a major trade show for all hi-fi manufacturers, called the IHF Show, to be held in May, 1978.

President Mitchell is very enthusiastic about the trade show, which will promote the industry to potential and existing retailers. Not one but several seminars are planned, covering such diverse topics as advertising, accounting problems, service problems, store displays, market research and countless other ideas to help hi-fi dealers share in the industry's growth.