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computer corner

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THIS MONTH, WE WILL DISCUSS COMPUTER interrupts, with emphasis upon the hardware and software associated with the vector interrupt. The three signals that you use in vector interrupt circuits include INT (input pin-14 on the 8080A), INTE (output pin-16), and $\overline{\text{INTA}}$ (not available on the 8080A but derived externally with additional logic).

The interrupt operation proceeds as follows: An interrupting device supplies a positive-going clock pulse to the INT (interrupt request) input of the microprocessor. The microprocessor recognizes the interrupt request either at the end of the current instruction being executed or while the CPU is in the halt state. Once an interrupt request is recognized, the CPU is inhibited by an internal flip-flop from recognizing another interrupt request. This internal flip-flop can be set (enabled) or cleared (disabled) with the aid of microcomputer instructions: The interrupt flip-flop is disabled (mnemonic DI) by instruction 363, and it is enabled (mnemonic EI) by instruction 373.

When cleared, the interrupt enable flip-flop inhibits interrupts from being accepted by the CPU. The flip-flop is automatically cleared when an interrupt is accepted; it is also cleared by the RESET input-signal applied at pin-12 of the 8080A IC. Output pin-12 (INTE, or interrupt enable) indicates the logic-state of the interrupt enable flip-flop.

An $\overline{\text{INTA}}$ (interrupt acknowledge) control signal is generated by applying the INTA (interrupt acknowledge) and DBIN (data bus in) control signals to a two-input NAND gate (Fig. 1). A logic 1 at DBIN (output pin-17 on the 8080A) indicates to external devices that

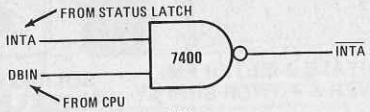

FIG 1

the data bus is in the input mode. The INTA control signal is a positive clock-pulse that is generated as a status output with the aid of a status latch connected to the 8080A microprocessor. The interesting aspect of the INTA control signal is that it permits you to "jam" an interrupt-vector instruction byte directly into the instruction register within the 8080A. This can only be done during an interrupt, but nevertheless it is a unique and highly interesting operation that is possible with the 8080A microprocessor.

A simple circuit that demonstrates how a single-byte instruction can be jammed into the instruction register is shown in Fig. 2. Assuming that the interrupt enable flip-flop has been previously enabled by instruction 373, the interrupting device must supply a

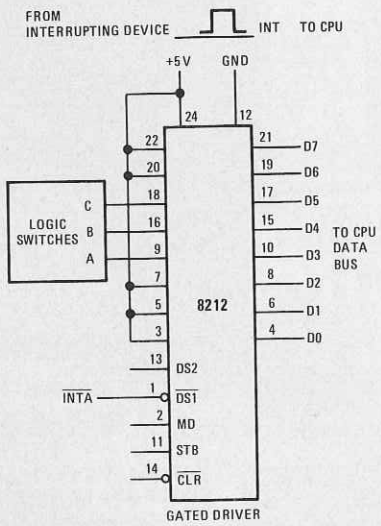

FIG 2

logic 1 input at INT in order to generate an interrupt request. The microcomputer finishes the current instruction, and then generates the interrupt acknowledge signal, $\overline{\text{INTA}}$, that jams the desired vector instruction-byte on the data bus and into the instruction register. Although any instruction byte can be jammed into the instruction register during an interrupt, usually the eight following instructions are used to produce a useful result:

Instruction	Mnemonic	Call the subroutine that starts at:
307	RST 0	HI = 000 and LO = 000
317	RST 1	HI = 000 and LO = 010
327	RST 2	HI = 000 and LO = 020
337	RST 3	HI = 000 and LO = 030
347	RST 4	HI = 000 and LO = 040
357	RST 5	HI = 000 and LO = 050
367	RST 6	HI = 000 and LO = 060
377	RST 7	HI = 000 and LO = 070

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The first sixty-four memory locations are reserved for interrupt *service routines* or *pointers.* These are extremely short programs, often consisting of only a single jump instruction, that tell the 8080 microcomputer what to do or where to go for a specified interrupt condition. Such routines precede the main program and associated subroutines in memory. If interrupts or restart instructions are not used, this portion of memory does not have any special significance.

Figure 3 is probably the simplest priority-encoder interrupt circuit that can be used with an 8080 microcomputer. The Intel 8212 IC is used as an 8-bit three-state buffer that inputs the instruction byte into the instruction register. The 74148 8-line-to-3-line priority-encoder IC has the following truth table:

Inputs								Outputs			
0	1	2	3	4	5	6	7	C	B	A	E0
X	X	X	X	X	X	X	0	0	0	0	1
X	X	X	X	X	X	0	1	0	0	1	1
X	X	X	X	X	0	1	1	0	1	0	1
X	X	X	X	0	1	1	1	0	1	1	1
X	X	X	0	1	1	1	1	1	0	0	1
X	X	0	1	1	1	1	1	1	0	1	1
X	0	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	0

The letter X means that the logic state is irrelevant.

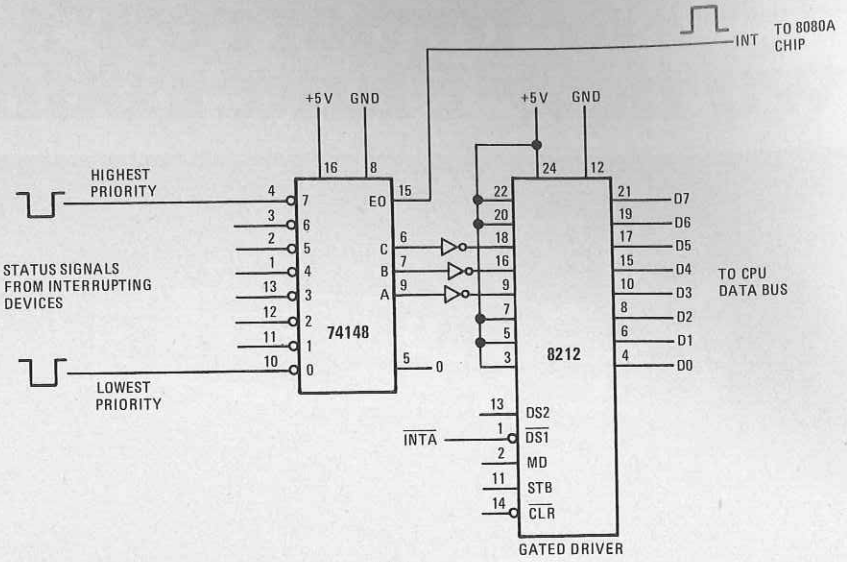

FIG. 3

The purpose of the circuit in Fig. 3 is to input the restart instruction, 3Y7, into the microcomputer. Five of the eight inputs to the 8212 IC are tied to a logic-1 state. The remaining three bits supply the encoded vector-address of the restart subroutine. By virtue of its truth table, the 74148 priority encoder provides eight priority levels. The inputs to this IC should be latched. The IC provides the three-bit binary output that corresponds to the highest valued priority input that is at a logic-0 state. The inverters invert this information to supply the three-bit "Y" component of the restart instruction.

If there is a logic 0 at any of the inputs to the 74148 IC, a logic-1 output will be generated at the E0 output (pin 15). This output serves as the input to the interrupt request pin, INT, on the 8080A chip. Upon receiving an interrupt request, the microcomputer responds with an interrupt acknowledge output, $\overline{\text{INTA}}$, that strobes the selected highest-priority restart instruction into the instruction register. **R-E**