IC FUNCTION GENERATOR EXPERIMENTS—BUILD A 2650 COMPUTER

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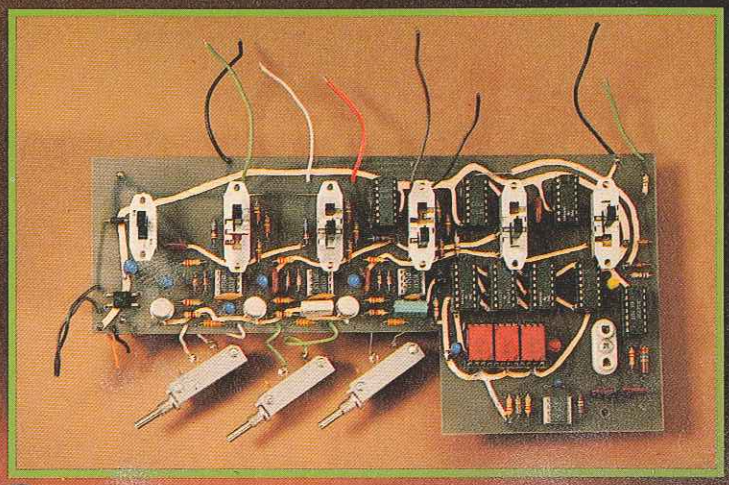

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them to the spectrum analyzer which was swept from 20 Hz to 20 kHz in the usual log-sweep mode. The resultant response curve of the left-channel equalizer is shown in Fig. 7, and it

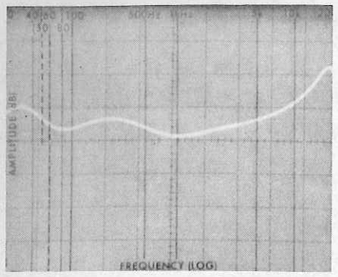


FIG. 7—ACTUAL EQUALIZER RESPONSE with the control settings shown in Fig. 6-b.

corresponds quite closely to the point-by-point or octave-by-octave settings shown of Fig. 6-a.

Connecting the equalizers into the audio chain and, again using pink noise, I observed the face of the Shure analyzer and noted that all lights were extinguished with the exception of the 32 Hz and 16 kHz indicators. (The 63 Hz indicator blinked every now and again, briefly, as I moved about the room, but was off when I returned to my "listening" chair.) The indicator lights are shown in the photo of Fig. 8.

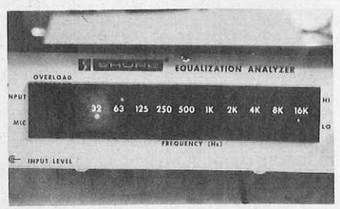


FIG. 8—EQUALIZATION ANALYZER shows total frequency response of hi-fi system after equalization.

Having a good source of pink noise at my command, I decided to measure overall response using this form of wide-band noise and the sweep filters of the spectrum analyzer (which were set to their narrowest bandwidth). First, I measured overall response with the equalizers bypassed. The results are shown in the upper trace of Fig. 9. Then the sensitivity of the analyzer was lowered (but with levels unchanged) so that a second trace could be displayed without superimposing it on the first sweep, and both left- and right-channel equalizers (preset as outlined before) were switched into the system and the sweep was repeated. The much improved results are shown in the lower trace of Fig. 9.

Still aware that single-tone sweeps have their problems, I nevertheless

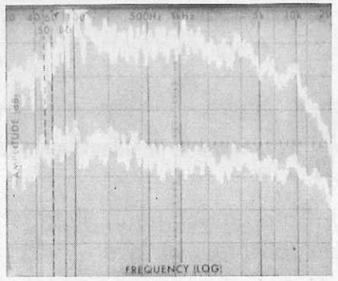


FIG. 9—TOTAL FREQUENCY RESPONSE of hi-fi system without equalization is shown in upper trace. Lower trace shows response after equalization.

decided to have another go using this method and, while those narrow-band bumps and valleys still showed up in Fig. 10, a comparison between Fig. 10 and Fig. 1 shows that even using this crude measurement approach, a great amount of improvement is evident.

You may recall that I never did

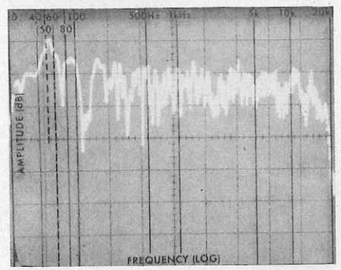


FIG. 10—SINGLE-TONE FREQUENCY RESPONSE of hi-fi system after equalization.

TABLE 1—EFFECTIVE AMPLIFIER POWER (watts) based upon various amounts of boost (dB).

AMPLIFIER RATING (WATTS)	+1 dB	+2 dB	+3 dB	+4 dB	+6 dB	+8 dB	+10 dB
20	15.8	12.6	10.0	7.96	5.0	3.16	2.0
30	23.7	18.9	15.0	11.94	7.5	4.74	3.0
50	39.5	31.5	25.0	19.90	12.5	7.90	5.0
100	79.0	63.0	50.0	39.80	25.0	15.80	10.0
150	118.5	94.5	75.0	59.70	37.5	23.70	15.0
200	158.0	126.0	100.0	79.60	50.0	31.60	20.0

succeed in bringing the 32 Hz and 16 kHz octaves to a "flat" response. Referring to Fig. 6 once more, you will also note that I settled for only +6 dB at the highest octave and less than +4 dB at the lowest octave. Perhaps you are wondering why I didn't crank these end-octave controls up to their full +12-dB capability. This brings us to a possible trouble area caused by equalization.

Moderate amounts of equalization can do wonders for the sound of your hi-fi system and, indeed, having now heard the difference between a *properly* equalized system and one which is not, I would not be without an equalizer from this point onward. But improper use of an equalizer can cause real havoc with your system. Suppose, for example, that my system had been perfect even without equalization except for those end upper and lower octaves. I might have pushed the 32 Hz and 16 kHz levers up to their extremes, but if I had done so, my amplifier would probably clip and distort at those extreme frequencies.

If I was lucky enough to hear the distortion before my tweeter burned out (or my woofer-cone ruptured), I would have had to "back off" on my volume control or lowered the effective power output *average* of my entire system by an enormous factor. Table I shows the *effective* available amplifier power of different amplifiers having different nominal power ratings when one or more equalization levers are set to different degrees of boost in an attempt to flatten the response of a system. Note that if a mid-frequency lever is boosted only 3 dB for example, the effective power available from the system (without clipping) becomes half of the amplifier's actual power rating. And, in an extreme case where 10 dB of boost at some specific frequency is required, a 200-watt amplifier becomes, effectively, no more powerful than a 20-watt amplifier with a flat response.

So, while we are convinced that system equalization can do wonders for a hi-fi system when used in moderation, over equalization to compensate for system deficiencies that are beyond helping can cause more damage and grief than no equalization at all.

The experience gained with the Shure equalization analyzer also convinced us that despite our long years of listening to hi-fi systems, attempting to equalize a system "by ear" can be a hopeless task. We hope that now that correct procedures are available as inexpensively as they are, that more and more audio dealers will offer in-home equalization service to serious audiophiles when they buy a graphic equalizer. Once we became familiar with the analyzer, actual correct setting of our equalizer controls took no more than about five minutes, and, despite the fact that none of the controls for either channel was set more than 6-dB away from "flat" (and most were displaced considerably less than that), we could not help marvelling at the improvement we heard. **R-E**

Build 2650-Based Microcomputer System

Part II. Built on a single printed-circuit board, this 2650 microcomputer contains a video and cassette tape interface and resident supervisor program. Add a keyboard, video monitor, cassette tape recorder and power supply for a complete working system

JEFF ROLOFF

LAST MONTH, A DESCRIPTION INCLUDING specifications and schematic appeared.

This month, an in-depth look at the troubleshooting procedures plus the component placement diagram is given.

Troubleshooting

After applying power to the PC board, the first thing to check is the power-supply voltage. If the output of an adequate (5 volts, 3 amperes) power supply is pulled down by connecting it to the board, there is either an IC put in backwards (if the supply is not pulled completely to ground) or else the power-supply lines are shorted somewhere on the board. If an IC is plugged in backwards, it will become very warm immediately after the power is applied. If the supply is actually shorted to ground, the process is much more tedious since you must inspect both supply lines to discover the point of the short. If quality IC's were purchased, the majority of problems are caused by solder or etch shorts. For this reason, it is a good idea to check the whole board for little solder spatters.

Logic and display circuits

The logic section of the board is the next part of the board to test. You need a scope for this part, and its bandwidth should be above 10 MHz. (You can also send the board into Central Data to have a trained technician test it for $15.00 an hour.) Connect the scope to the composite video signal that appears on plug 5, pin 5, of the board. Observe the sync pulses that appear at the zero-volt level. There should be one short sync pulse (down from 0.5 volt) every 63.5 μs, and one long pulse every 16.667 ms. If either of these two trains of pulses are not there, or have the wrong frequency, you must check the Timing Chain and Sync Generator section of the circuitry.

The Timing Chain and Sync Generator circuit contains a crystal-oscillator as the basic timing source. (A complete schematic appears in last month's issue of **Radio-Electronics.**) This is a standard oscillator with the 14.192640-MHz crystal used as the main feedback element. The signal from this oscillator is buffered using three other inverters from IC53. The first divider network that this signal goes to is formed by IC50, IC51 and IC52. These three IC's are used to divide the master clock down to a signal that has a period of 63.5 μs. The three counters are all fed by the same clock, so that all of the outputs change state at the same instant. The enable pins of the two low-order counters are fed from the previous counter stage(s) in an arrangement that forms a 10-bit syncronous binary counter. Pins 1, 2 and 13 of IC54 monitor the states of this counter. When all three of the monitored lines are high, the clear line is activated which resets all of the counters.

The D1, D2 and D4 outputs of IC52 provide the first three binary divisions of the master clock. Since the characters are eight-dots wide, output D4 has the width of one character (it is the divide-by-eight output). The last output of this counter, along with all of the outputs of IC50 and IC51 (designated the 'C' outputs) provide a count of the current character position on the display. While it is counting from 0 to 79, the characters are actually appearing on the screen. While counting from 80 to 112 (during which the counters are reset), the display is in the process of horizontal blanking.

The horizontal sync signal is generated by IC62-a. The sync signal is eight character-spaces wide, which is about 4.5 μs. Also, the three dot signals that come from IC52 (D1-D4) are all OR'ed together to form the $\overline{\text{LOR}}$ signal that is used in the Display Generator circuit to load the data from the character generator into the shift register once for every character. The $\overline{\text{LOR}}$ signal has a duty cycle of 1/8 (negative duty cycle, that is), and it goes low for this one dot period at the very beginning of each character.

Now that the signals are defined for all of the areas of each scan line, the up and down position on the screen must be defined. The three other counters

(IC55-IC57) serve this function, IC55 is used to count down by 12 and the other two are connected to count down by 21. The input that enables the first counter is the $\overline{\text{EOL}}$ signal that reset the previous counters at the end of a scan line. The output of this counter is monitored at pins 3 and 4 of IC54, to determine when 12 scan lines have been counted. When this event has occurred, its output at pin 6 drops and resets the counter. The reason that it counts to 12 is that there are 12 scan lines for each character line on the screen (i.e., vertically there are 12 dots for each character). The L1, L2, L4 and L8 outputs of this counter are used to determine which scan line of a character line is currently being displayed. From lines 0 to 7, the display section is actually displaying a character (since the actual character size is eight-dots tall), while from lines 8 to 11, the display is blanking between lines.

The reset line for IC55 is used to clock the next two counters that determine the character line being displayed. The counters (IC56 and IC57) are both reset by IC54-b when a count of 21 character lines is reached. From character lines 0 to 15, the display is actually showing characters on the screen (or at least it can be), while from character lines 16 to 21, the vertical blanking is in effect. Vertical sync is generated in this time period by IC62-b. Pins 4 and 5 of IC64-a are inputs to the gate that mixes the vertical and horizontal sync signals to form the composite sync signal.

The video-blanking signal is composed of a horizontal blanking and vertical blanking signal. The horizontal blanking signal is generated by IC64-b and IC66-b. The output of IC66-b is high when C64 and C16 are both high (at character position 80) and later changes back to low when $\overline{\text{EOL}}$ is present. Any of the four inputs to NOR gate IC70 indicate that the screen should be blank when they are high. So there are three other signals that indicate that the screen should be blanked and all of them are OR'ed together to form the master blanking signal. The vertical-blanking area is indicated by LN16. Any one of the four scan lines between character lines is indicated by L8. The DISPMEM line is high whenever the processor is accessing the display RAM. Wrong character patterns would appear when the display RAM is accessed, so we just blank the screen during this small interval to cover up the few out of place dots. The DISPLAY ACCESS signal is low whenever the screen is to be blanked. This signal is delayed one more character time (to make up for the delay in accessing the RAM and character generator in the Display Generator circuit) by IC65, using pins 2 and 5. If the processor is accessing display memory, pin 8 of IC65 is low and is a one character-time delayed version of the DISPLAY ACCESS signal. This in turn keeps $\overline{\text{BLANK VIDEO}}$ (pin 5 of IC65) low a little after DISPLAY ACCESS disappears to make up for the recovery time required by the RAM. The $\overline{\text{BLANK VIDEO}}$ signal goes to the output shift register and keeps the output data low by clearing the register.

If these circuits are operating correctly, a good video signal should be present that can be connected to a video monitor. Figure 1 shows the composite-video

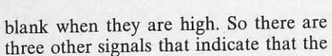


FIG. 1—COMPOSITE VIDEO SIGNAL supplied to video monitor.

signal. If the sync signal is correct, the monitor should immediately lock onto the video signal and display a stable picture. If the picture does not lock-in, try lowering the value of the 330-ohm resistor (R9) in the video output stage (such as 220 ohms) and lower the value of the 100-ohm resistor hooked to the base of the two transistors. This will adjust the sync level and the total video-output level to suit your monitor. If you have a standard monitor, you will not have to do this since the output signal is standard.

If the characters on the screen waver, there is still a problem with the Timing Chain and Sync Generator circuit. Check this circuit out again, looking for any imperfections in the signals that indicate a bad IC or a shorted line. This probably won't happen, since a fault in the circuit usually causes major problems and not just a little wavering on the screen.

Now that a pattern appears on the screen, it must be identified. If it is a prompting character (a period) and the cursor appears in the upper left corner of the screen, the whole system is probably working. All that is needed is to hook up an ASCII keyboard and tape recorder to the correct plugs and see if commands can be entered into the monitor. (The procedure for testing the cassette interface is given later.) If you have either random characters on the screen or just 16 solid horizontal bars, the processor section of the board is probably not working. This prevents the supervisor program from being read in and thus the screen is not cleared.

Processor

The Processor and Bus Driver circuit divides the master clock by 12 to obtain the CPU clock. The divide-by-6 counter IC58 starts its count at 10 and counts up to 15. After the count of 15, inverter IC53-a connected to the carryout line and load input is used to load the 10 and start the division again. Flip-flop IC66 divides this carry signal by 2 to obtain the square CPU clock. The frequency of this clock is about 1.183 MHz, and if the faster version of the 2650 is put into the board, the counter's inputs can be changed to increase this frequency. The CPU clock signal is gated through IC11-a with the $\overline{\text{STOP CLOCK}}$ signal that allows you to externally stop the clock by bringing the line low. The timing relationships of the microprocessor is shown in Fig. 2.

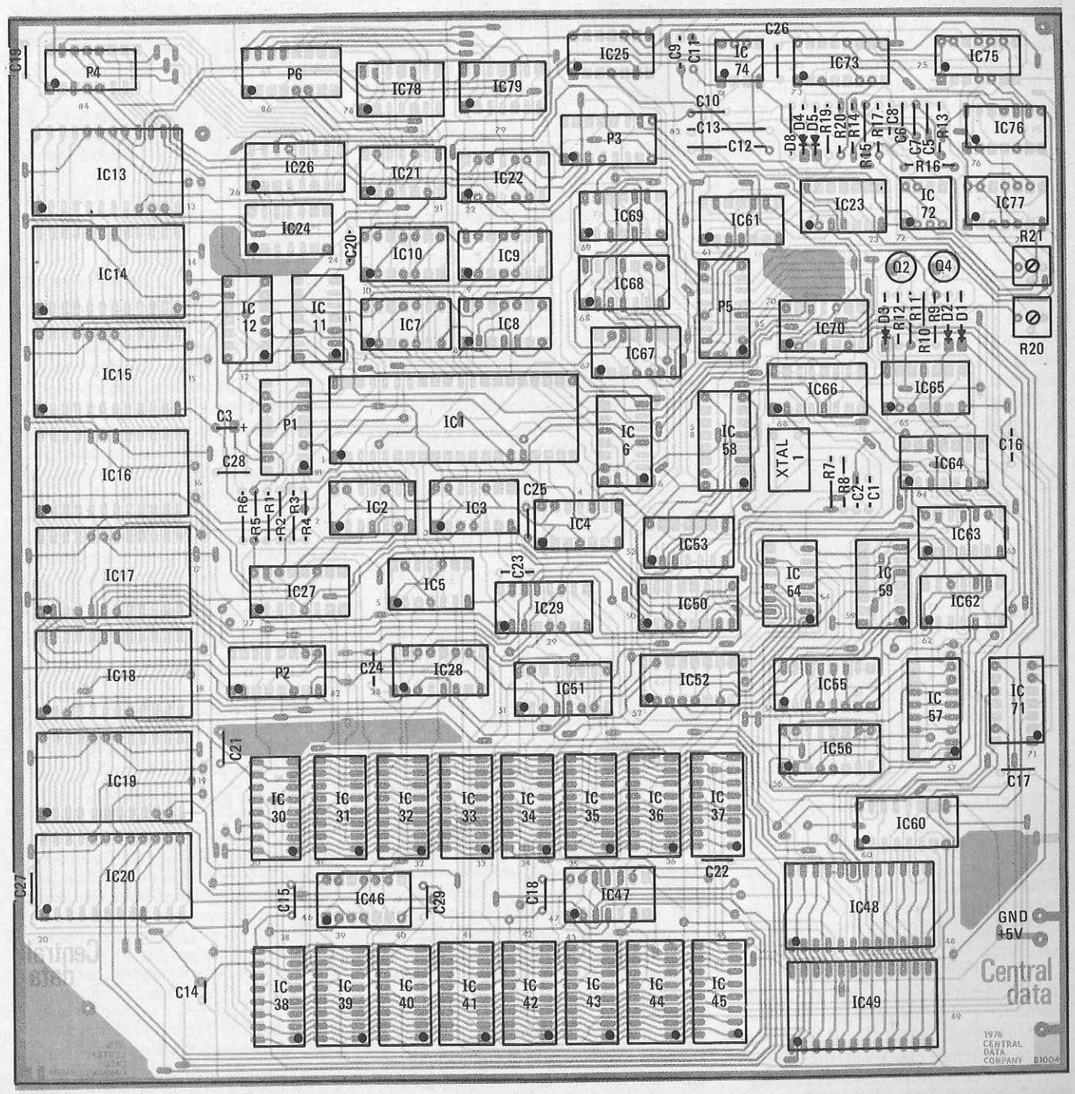
Pin 16 of the 2650 is the reset input, and the RESET signal is generated using a Schmitt trigger and an R–C time constant. Capacitor C3 is initially discharged and the RESET line is therefore high. As the capacitor charges through resistor R6, the output of the inverter will change to a low level allowing the processor to operate—starting at address zero in memory. All of the outputs of the processor, except for RUN/WAIT, are buffered with tri-state drivers or an inverter in the case of the serial output line.

The tri-state drivers have their enable pins available for data bus override operations. For instance, bringing the $\overline{\text{ADDR DISABLE}}$ line low causes all of the address buffers to be disabled. This allows another device to take control of the address bus. The same is true for the data and control buses. So, by bringing these three enable lines low, you can effectively disconnect the 2650 from any external memory.

The SERIAL INPUT and SERIAL OUTPUT lines come directly from pins on the processor that can be inspected or set by special processor instructions. This allows the system to get by without a UART and also allows high flexibility as far as output rates and formats.

The data bus buffers are tri-state buffers, with either the in or the out buffers being enabled at one time. If the $\overline{\text{R}}$/W line is low, the processor is reading data, so the input buffers are enabled. If this line indicates that the processor is outputting data to the data bus, then the output buffers are enabled. Although buffers are not needed, they were put in so that any memory added to the system would not need to have its own set of buffers.

In the area of expansion, Central Data offers a S100 compatable bus board. It generates signals derived from



COMPONENT PLACEMENT diagram

PARTS LIST

All resistors ¼ watt, 5%.
R1-R6, R14, R18—10,000 ohms
R7, R8, R16, R17—1000 ohms
R9—330 ohms
R10—150 ohms
R11—82 ohms
R12—100 ohms
R13—620 ohms
R15—470 ohms
R19—20,000 ohms
R20—68,000 ohms
R21, R22—20,000-ohm trimmer potentiometer
C1, C2, C11—100 pF, disc
C3, C14—100 μF, 16 volt, electrolytic
C4, C8—0.01 μF, disc
C5, C6, C7, C9, C15-C29—0.1 μF, disc
C10—0.0022 μF
C12, C13—0.056 μF, ±10% polyester film
D1, D2—1N914 diode
D3—1N4729 Zener
D4, D5—1N4148 diode
Q1, Q2—2N5139 transistor

IC1—2650 microprocessor (Signetics)
IC2-IC10, IC21, IC22, IC78, IC79—74126
IC11, IC64, IC69—7408
IC12—7414
IC13, IC17—3624, pre-programmed PROM containing supervisor program
IC14-IC16, IC18-IC20, IC48—3624, PROM (see text)
IC23, IC24, IC65, IC75, IC77—7474
IC25, IC71, IC76—7400
IC26—9344, 4-bit by 2-bit multiplier (Fairchild)
IC27-IC29—74157
IC30-IC45—2102-1, RAM (Signetics)
IC46, IC47—74125
IC49—3624, pre-programmed PROM character generator, upper case
IC50-IC52, IC55-IC58—74163
IC53—74S04
IC54—7410
IC59—7432
IC60—74166
IC61, IC68—7411
IC62—7420
IC63, IC67—7404
IC66—74109
IC70—7425
IC72—555, timer
IC73—74123
IC74—CA3130
XTAL1—14.192640 MHz series-resonant crystal
MISC.—One 40-pin DIP socket for IC1, six 16-pin DIP sockets and printed-circuit board.

The following parts may be ordered from: Central Data Company, P.O. Box 2484, Station A, Champaign, IL 61820.

IC49—3624, pre-programmed PROM character generator, upper case, $27.

IC13, IC17—3624, pre-programmed PROM containing supervisor program, $27 each.

PC board, predrilled and etched, $30.

An assembled and tested microcomputer board, $325.

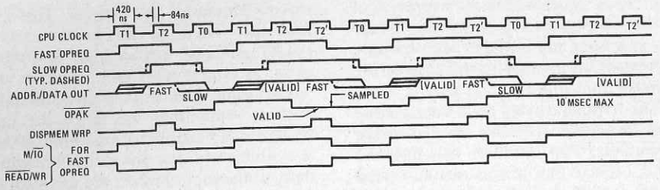


FIG. 2—2650 MICROPROCESSOR timing relationships.

the 2650 board that will interface directly with any standard 8080 static RAM board or I/O board. The board has room for five edge connectors, and is plug expandable with extender boards.

Locating a problem in the Processor and Bus Driver circuit requires inspection all of the address and data-bus lines to be sure that all of the signals are at standard TTL levels. If one line is stuck either high or low, carefully clip the pins of the IC's that this line runs to until the problem clears. The last pin that was clipped is the one holding the line, so replace the IC. Before cutting the IC pins, check the power supply on all of the IC's that the line runs to. Also, if any of the IC's are tri-state buffers, check to be sure that they are not gating data onto the line at the wrong time (an enable pin may be stuck in the enable state.)

If the processor's bus checks out, then you check to be sure that the RAM interface to the processor is working since that would also cause the random characters to appear on the screen. Initially, when the supervisor program is executed (right after reset), it clears the screen by sending the ASCII code for a blank (H20) on the data bus to the RAM, and then sequentially accessing all of the display positions and writing the data. Therefore, right after a reset, the DISPMEM line should undergo many transitions. If it doesn't, check out gates IC61-a and IC69-a that are used to generate this signal from the address lines. Note that the DISPMEM line indicates what page the processor is accessing—if it is the 4K page where the display RAM resides, this line is high.

If the DISPMEM line checks out, then look at the write-pulse generating circuitry. IC61-a (pins 1,2,12 and 13), along with flip-flop IC23-a, is used to generate a signal that is high at pin 5 of IC23-a for the first CPU clock cycle following the low to high transition of the OPREQ-signal. This is gated with $\overline{R}$/W line and the CPU clock by IC61-b. This signal finally goes through one last gate that turns on the write line of the RAM's if the processor is accessing the display memory page. This write line should have high activity right after the power is tuned on.

If these signals check out, then check the data-bus drivers IC46 and IC47. They are used to gate data from the display memory onto the data bus so that the processor can read the contents of the RAM. It is helpful to have a dual-trace scope for this, so that the input to the buffers and the output can be observed at the same time. Then check to see that the input and output of the buffers are the same when the enable is high.

There is almost nothing that can go wrong with the character generators, their operation is simple. IC49 is the one that is used for the normal operation of the board, with IC48 being an optional character generator for lower case, graphics, or other characters. Therefore, when supervisor program is the only thing that is running, it only selects character generator IC49. For this reason, the chip enable on IC49 (pin 20) should be low whenever the video is not blanked. This is easily checked with a dual-trace scope. If the other character generator is selected, and it is absent, a block of all on dots will appear on the screen. So, if you have several of these selections in a line, you will have a big horizontal bar on the screen rather than characters. Two of the output lines of the RAM may also be shorted, which would cause some characters not to be displayed. Again, a dual-trace scope is needed to check the data-out lines against one another to see if any look shorted.

The output shift register is IC60. It is loaded with the character generator's outputs at the first horizontal-dot position of each character, and then sends the eight-bit word out serially at the master-clock rate. Note that the clear line on IC49 is driven by the $\overline{\text{BLANK}}$ $\overline{\text{VIDEO}}$ line from the Timing Chain and Sync Generator circuitry.

The addresses for the display RAM are multiplexed by the Display Memory Address Switch. If the DISPLAY ACCESS line is low, the processor's address lines are selected to address the display RAM. This is the case when the display is being blanked (and thus the processor tries to access the display memory, raising the DISPMEM line and dropping the DISPLAY ACCESS line). The other case is when the display RAM is addressed by the Timing Chain. The signals C1 to C64 are gated in, along with LN1 to LN8, to select the correct address.

If the gating circuit for the ROM is not working properly, the supervisor program will not run. The output at pin 12 of IC-67 goes low whenever the ROM is selected. When using the supervisor program, this line will always be low when the DISPMEM line is also low. In other words, the supervisor only has two places to operate from, it will always be selecting one of these places.

The I/O ports 8 are also enabled using a good deal of gating circuitry. If the data bus doesn't have the right signal levels, check the two groups of data-bus buffers to be sure that they are not gating data onto the bus. This could happen if the enable pins are locked in a high state. Either a write data or a write control instruction will access the output port.

If the circuitry checks out, the supervisor program must be working for all of the operations except the tape routines. It is a simple matter to set up the cassette-tape interface and once it is set, it will stay perfectly aligned until it is changed. The potentiometer for the 555-timer should be adjusted so that the output of the 555 is a 4800-Hz square-wave. This is divided by two by the first flip-flop (pins 3 and 5 of IC77), and again by the second half of this same IC. The serial output line is clocked through part of IC75, and then this output is used to gate on one of the two frequencies. The R–C network at the output of IC76 (pin 11) is used to decrease the output-voltage level and change it into a more rounded signal. The demodulator section is just a monostable and operational amplifier.

continued next month

NOAA updates list

The National Oceanic and Atmospheric Administration (NOAA) National Weather Service has updated its list of stations to about the end of last year. The network is the sole government operated system for communicating weather, disaster or other warnings direct to the public. Weather receivers are available at most electronic stores.

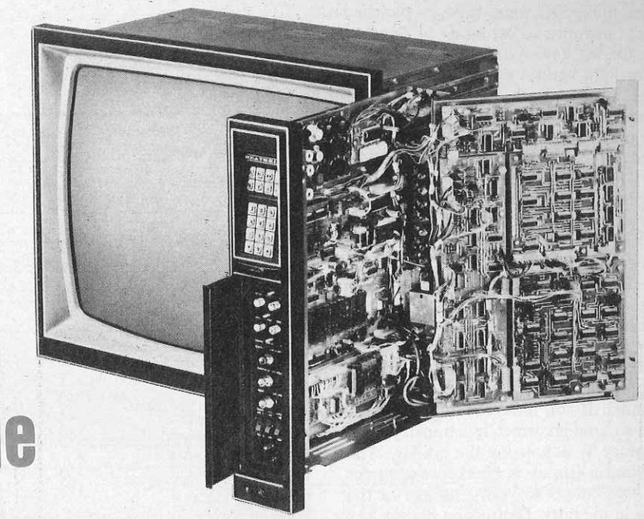
The broadcasts are at 162.40, 162.475, or 162.55 MHz. A listing (by state, call letter and frequency) of the stations in service available free by writing to the National Weather Service, Silver Spring, MD 20910.

Zenith gets a patent for improved electron gun

Zenith's EFL (*E*lectrostatic *F*ocus *L*ens) has received Patent No. 3,995,194, granted to Zenith research and development engineers Allen Blacker and James W. Schwartz.

The EFL gun extends the focusing action over a longer distance by using four electron lens elements, instead of only two as in most electron guns. This concentrates the beam to produce a spot size as much as 60 percent smaller than in conventional gun systems. The new in-line gun is housed in the narrow neck of the company's 19-inch 100-degree picture tube. **R-E**

HEATHKIT GR - 2001



Programmable Color TV

It's the first set on the market with programmable automatic channel selection. Enter a series of time/channel combinations on the keyboard, and the set automatically switches to the channel at the programmed time

ART KLEIMAN
MANAGING EDITOR

BACK IN 1974, THE HEATH COMPANY SHOOK the foundations of the TV industry with the introduction of the GR-2000 color TV receiver. That set contained unique features found in no other set at the time, including silent all-electronic varactor tuning, touch-to-tune channel selection, touch volume control, on-screen digital channel readout, on-screen digital clock readout and a fixed L-C IF bandpass filter. (See the February 1974 issue of **Radio-Electronics** for a full report on the GR-2000.)

Heath's latest introduction—the GR-2001—contains features that set it apart from the rest of today's industry. This is the first TV set to feature programmable automatic channel selection and automatic antenna rotator control. With the programmable channel selection feature (offered as an optional accessory, the GD-1185), the user programs a time/channel combination and the TV set automatically switches to that channel at the programmed time. Two blocks of 16 (for a total of 32) time/channel combinations can be programmed at any one time. The automatic antenna rotator control, also offered as an option, automatically orients the antenna to a programmed direction when a channel is selected. It replaces the control portion of a standard antenna rotator system.

The GR-2001 includes all the features that made the GR-2000 unique. In fact, the two receivers are basically the same. One difference that is immediately apparent is the method of channel selection. On the GR-2000, two pushbuttons scan the channels up and down until the desired channel is reached. The new GR-2001 has a 3 × 4 calculator-type keyboard containing the numerals 0—9. Channel selection is accomplished by entering two digits on the keyboard. The remaining two keys function the same as on the GR-2000—they scan the channels.

As far as the chassis is concerned, it remains basically the same as the GR-2000. Some modifications have been made for improved performance. Heath redesigned the audio circuitry for better sound and included phase-locked-loop circuitry to eliminate the vertical and horizontal hold controls.

The programmable automatic channel selection feature really caught our attention. This one feature sets this set aside from all others on the market. The circuitry for this optional accessory is complex, containing 60 IC's mounted on four printed-circuit boards, not counting the on-screen digital clock option that must be included for this accessory to function. Since the feature is unique, let's take a look at how the channels are programmed.

Channel programming

In addition to the 3 × 4 keyboard used for channel selection, there are 8 pushbuttons and a rocker switch used for operating the programmer. Three of these pushbuttons are used for mode selection and the other five are used for entering data into the programmer.

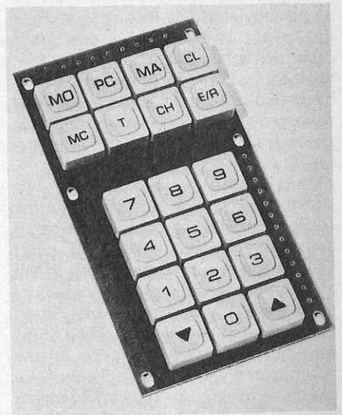


FIG. 1—NUMERICAL KEYBOARD is used for channel selection. The eight keys located above the numerical keyboard are used to control the automatic channel selection feature. Channels can also be scanned using the two keys with the arrowhead designations.

Figure 1 shows the layout of the keyboard and eight pushbuttons. The rocker switch selects between two memory banks and is located behind a door on the front panel.

Programming the time/channel data is a matter of manipulating the mode,