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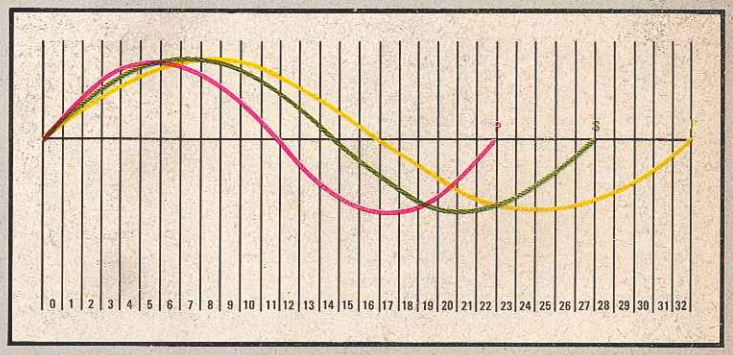

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computer corner

Z-80 *An in-depth look at the Z-80 and how it differs from the 8080.* WILLIAM BARDEN, JR.

THE Z-80 MICROPROCESSOR IS THE LATEST in the line of MOS LSI (*M*etal-*O*xide-*S*emiconductor *L*arge *S*cale *I*ntegration) microprocessors that evolved from the Intel 8008. Designed and produced by Zilog, Inc., the Z-80 is "downwards compatible" with the Intel 8080 instruction set, just as the Intel 8080 instruction set included the Intel 8008 instruction set. Not only can the Z-80 execute programs based on the 8080 instruction set, but it includes 80 additional instructions that supplement the 78 instructions of the 8080.

Accompanying the new instruction set is a new architecture, which, in general, encompasses the architecture of the Intel 8080. Whereas the 8080 has seven general-purpose registers, a stack pointer and a program counter available to the programmer, in addition to internal registers not accessible to the user, the Z-80 has another *set* of the seven general-purpose registers and two *index* registers. All of the nine new registers are available to the programmer. In addition, two other registers provide interrupt control and memory refresh control.

The third difference between the Z-80 and the 8080 is the pin-out, the signals associated with the 40 pins of the Z-80. As in the 8080, a 16-bit address bus enables a direct address of 65,536 bytes of memory. Likewise, an eight-bit data bus allows transfers of eight bits or one byte of data between the Z-80 CPU and memory or I/O devices. However, the Z-80 requires only one +5-volt power supply and only a single-phase clock, and adds an external NMI (*N*on-*M*askable *I*nterrupt) line. In comparison, the 8080 requires three supply voltages (+5, −5 and +12 volts) and a two-phase clock, and has only a single interrupt line.

The final major difference between the Z-80 and the 8080 is in the clock speed. Some microcomputer manufacturers hand-select Z-80's that will run at clock speeds of 4 MHz, twice as fast as the standard 8080 version. The standard version of the Z-80, however, operates at 2.5 MHz, which is 25% faster than the 8080's 2.0-MHz clock speed.

All in all, the above features make the Z-80 an attractive replacement for the 8080, and at least seven manufacturers are producing either microcomputers based on the Z-80 or microcomputer boards that are compatible with the MITS (S-100) bus. Many commercial users are seriously considering using or are already using the Z-80 microprocessor in new designs. This first of a series of columns will discuss the Z-80 in terms of the architecture, pin-out description, address modes and instruction set and use.

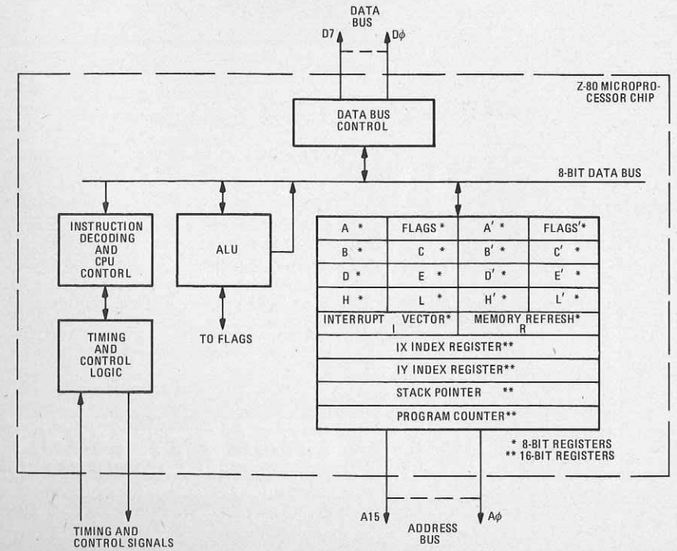

FIG. 1

Architecture

Figure 1 shows the basic architecture of the Z-80 microprocessor. The program counter holds the address of the current instruction that is being fetched from external memory. Since it is a 16-bit register, up to 65,536 (64K) bytes of external memory can be addressed to fetch an instruction. The stack pointer is also a 16-bit register and addresses a memory stack area anywhere within external memory. As in other microprocessors, this stack area is used for temporary storage of variables in the program, storage of the PC during subroutine calls and storage of registers during interrupt processing.

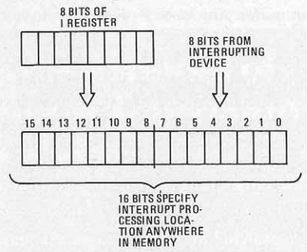

FIG. 2

Memory-refresh register R is a seven-bit counter that continually counts every instruction fetch. The contents of the R register (0 to 127) are sent out on the seven least significant bits of the address bus while the current instruction is being decoded. External memory logic uses the count to refresh dynamic RAM memories. The I register, or Interrupt Page Register, is loaded by the program and provides the eight most significant bits of an interrupt vector address (Fig. 2), while the lower eight bits are supplied by the interrupting device. An interrupt processing routine can therefore be located anywhere in the 64K of memory.

Two 16-bit index registers, IX and IY, perform an indexed type instruction useful in accessing tables in memory. This addressing mode will be discussed in a later column in this series.

The general-purpose registers are divided into two groups, each consisting of seven general-purpose registers, designated A, B, C, D, E, H, and L. As in the 8080, six of these registers operate together as register *pairs*: B and C, D and E, and H and L. Taken together, a register pair is 16 bits, although either register of the pair can be used as an eight-bit register by itself.

Accumulator register A is the primary register used in arithmetic and logical operations in the Z-80. At any time, the CPU can switch from one group of seven registers to the other group of seven registers by a single instruction. The other group has the same designations except that they are primed—A′, B′, C′, D′, E′, H′, and L′. There are many advantages in having the additional storage of the second group of registers as, for example, in rapid interrupt processing and increased processing speeds when temporary results can be held in the second set of CPU registers rather than in memory.

Two sets of flags, F and F′, are associated with the register groups. The flags are set as a result of arithmetic and logical operations performed by the ALU (*A*rithmetic and *L*ogical *U*nit). The flags record whether the results of the last operation produced carries, a zero result, a negative result, parity, and/or overflow, and can be tested to cause conditional branches in the program (Fig. 3).

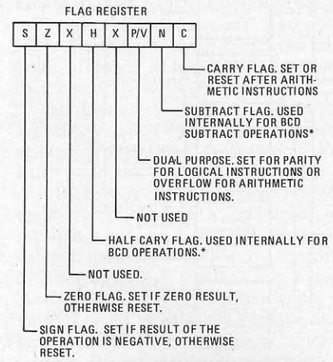

FIG. 3

The ALU is an eight-bit arithmetic or logical unit that can add, subtract, shift, AND, OR, exclusive OR, and perform other operations on two binary operands. It also performs addition or subtraction of two BCD (*B*inary *C*oded *D*ecimal) operands. The current set of flags is set on the results of the arithmetic or logical operation.

Next month, the column will continue with a discussion on the pin-out of the Z-80 IC and the Z-80's timing.

In the column that will follow, the discussion of the Z-80 will include: interrupts, interfacing techniques, the different types of instructions and the various addressing modes. R-E

SERVICE QUESTIONS

continued from page 77

−0.3 volts and it ought to be −4.8 volts. Transistor and diode replaced. Where is it?—G.M., Washburn ME.

In the AGC from what you have found so far. Try clamping the IF AGC at about +1.5 volts and see if this gives you a picture. If so, leave the clamp voltage there and check your AGC keyer to make sure that you do have the keying pulse *and* the video signal on the base. You need both of these to get any AGC action. I suspect that one of them didn't show up for work this morning!

HORIZONTAL PROBLEMS

There are all kinds of screwball problems in this Curtis-Mathes CMC-40. The horizontal hold is very unstable, color acts up and so on. The waveforms on the AFC diodes are very odd. I found a burnt resistor which seems to be R115, on the flyback. I'm confused!—J.G., Hatfield.

To start with, replace that resistor. R115 is a pulse-coupling resistor from the flyback to the AFC. While you are there, check the capacitive voltage-divider network C520/C521. If one of these is open, the pulse will be off. Also, from

continued on page 83