state of solid state

A new processor from National that can function as a programmable calculator or as a number cruncher for your microcomputer. **KARL SAVON,** *SEMICONDUCTOR EDITOR*

IF YOU HAVE EVER TRIED TO PROGRAM A microcomputer to do an elementary decimal arithmetic calculation, you know how complicated simple things can get. The National MM57109 MOS/LSI Number-Oriented Microprocessor is designed to make life considerably easier. Its language is calculator-oriented, and the circuit can be used with or without a separate controlling microprocessor. In control applications such as measurement and navigation systems, the device functions with the aid of an external program counter and program source. Where number handling is only one part of the overall picture, the number cruncher becomes the peripheral to a more conventional microprocessor.

The number cruncher

Microcomputer instruction sets are limited to binary addition with the occasional luxury of subtraction. A couple of machines have BCD adjustment instructions or can do BCD arithmetic, but this is only of limited help.

To develop a software math package that can handle scientific or more generally floating-point calculations is an education in itself. Decimal inputs must be converted to binary and normalized for the best use of the available memory space. The calculations must be done and the results rounded off and converted back to decimal. In addition to the magnitude of this task, even if such a package were already available, the math routines eat up memory and, of course, must be loaded from a storage medium or programmed into ROM or PROM.

The MM57109 performs conventional scientific calculations, does program branches based on flag and register tests, and inputs and outputs data with coordinating handshake signals. It combines the arithmetic functions of a scientific calculator with the control instructions used in stand-alone microcomputer systems.

This device is actually a mask-programmed version of the MM5799 part of the COP (*C*alculator *O*riented *P*rocessor) family; these processors have CPU, ROM, RAM, and I/O circuitry on the same IC.

Figure 1 is the block diagram of the MM57109. There are eight internal registers, each with 12 digits of storage. Registers X, Y, Z, T and M are accessible through programming. It is possible to expand the internal register files with an external 256 × 4 RAM. Lines DA1 through DA4 and the external instruction storage are used to address these 16 registers.

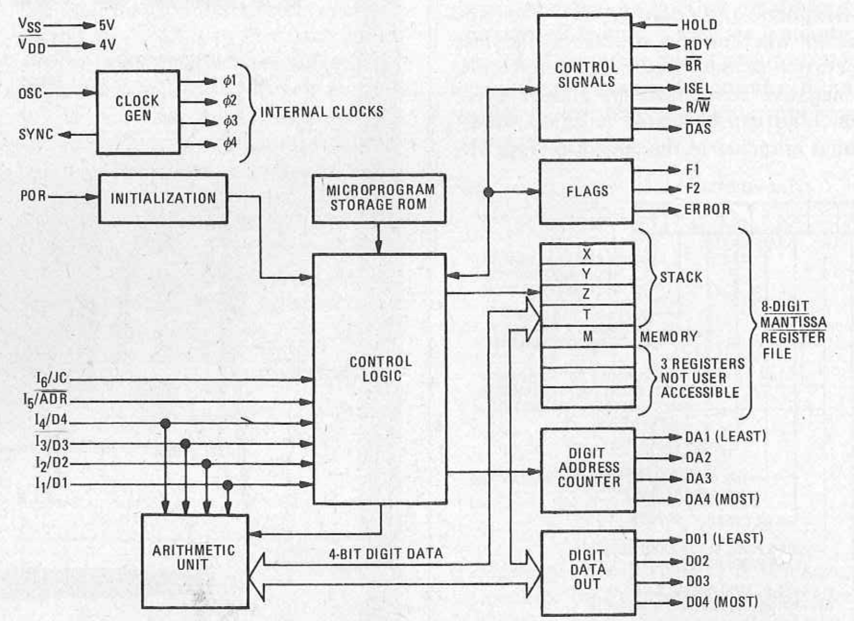


FIG. 1—NUMBER CRUNCHER. National's MM57109 is a dedicated processor that can be used as a stand-alone programmable scientific calculator or as a peripheral for your microcomputer.

The clock generator runs from an external noncritical single-phase 400-kHz oscillator. The clock circuitry generates a SYNC output pulse every four oscillator cycles to form a 10-μs "microcycle." Each instruction requires the execution of many microcycles.

The initialization block provides automatic power-on resetting when 5 volts is first applied to the POR terminal and then switched to −4 volts. Three pulses on the RDY line signal that the MM57109 is ready for its first instruction.

The instruction format includes a 6-bit operation code. Pins I1 through I6 are the instruction input pins driven by the external program source. They also function as the data lines when the ISEL line is set to logic 0.

When the device is ready for an instruction, the RDY line goes high and remains there for as long as the HOLD line is held high. The HOLD line is switched to ground when the instruction from the program source has been accessed. If the system timing is such that the instructions are always ready within 9 microcycles of when the RDY line goes high, the HOLD line can be permanently wired to ground. When the MM57109 is used in a stand-alone system, the RDY line becomes the clock for the external program counter. The parallel outputs of the program counter address the program memory, which holds the sequential instructions.

The $\overline{BR}$ control output provides the results of test instructions. The output is a 4-bit, microcycle low pulse when the performed test proves true.

Numbers have BCD-encoded 8-digit mantissas and 2-digit exponents, and are manipulated in a four-register stack and memory register in Reverse-Polish style. The device can be considered as a programmed scientific calculator with a different type of I/O interface and separate program counter and instruction source.

Each of the four stack registers and the logic-1 memory register store the bits of the 8-digit mantissa and 2-digit exponent as well as sign bits and decimal-point position indicator.

Numbers are transferred in and out of the MM57109 through data pins D1 through D4. Single decimal digits are received serially as 4-bit BCD words. Either the floating point or scientific notation mode is selected with the TOGM (*TOG*gle *M*ode) instruction. On initialization, the mode is set to floating point, which does not use exponents. The SMDC (*S*et *M*antissa *D*igit *C*ount) instruction sets the number of digits between 1 and 8, and is initially set to 8. As digits are fed in or out serially, the state of lines DA1 through DA4 identifies the digit.

There are three flag outputs: F1, F2 and Error. Flags F1 and F2 are set by instructions SF1 and SF2 or pulsed by instructions PF1 and PF2. The Error output is set high when calculation errors occur, such as taking the logarithm or natural log of a number less or equal to 0, a result exceeding the 10^{-99}-to-10^{99} range, and taking the square root of a negative number.

Input JC shares the I6 line and is tested with a TJC instruction.

The MM57109 instruction set has a total of 70 digit-entry, move, math, clear, branch, I/O and mode control instructions. Instructions have a 6-bit op code, and another two bits available for extended hardware such as device selection using the AIN instructions. Two-word instructions use a second 8-bit word that holds a branch address or the mantissa digit count.

The digit entry group of instructions are: 0–9, decimal point, enter exponent, change sign, π, enter, no operation, and halt.

If the instruction preceding an entered digit is enter, register X is cleared and the digit is put into X. When a number is entered, the stack is pushed; the contents of Z move into T, Y into Z, X into Y, and X is cleared to 0. This "initiation of number entry" occurs only once for each series of digits corresponding to a single number. Digits following the eighth mantissa digit are ignored. As in calculators, the number-entry mode is terminated by any non-entry instruction. The IC then normalizes the number by shifting the decimal point until it is to the right of the first mantissa digit and adjusts the exponent accordingly.

The move instructions include the stack operations, register exchange, memory store and recall, and left and right shifts of the mantissa.

The math group does the conventional four functions, plus trigonometric and logarithmic functions.

Two clear instructions clear and initialize the system.

The branch group is divided into two subclasses: The test class that checks the JC, Error and register X conditions. The count class increments or decrements memory, and branches if memory is not zero.

Input/output instructions are the multidigit IN and OUT and the single-digit asynchronous AIN entry.

Flag instructions control flag 1, flag 2, and R/$\overline{W}$ outputs.

The TOGM, SMDC and INV instructions set the operating mode; the INV instruction sets the inverse mode for trigonometric or memory instructions.

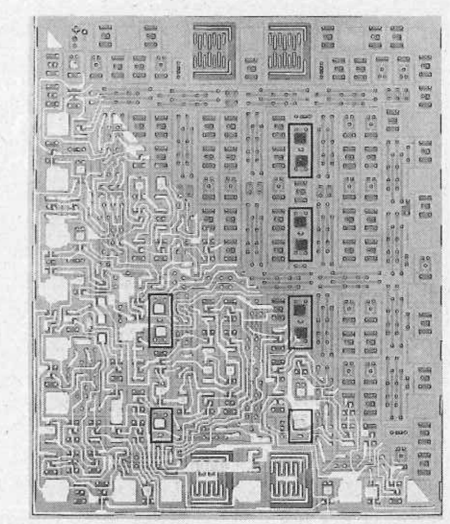
The number of microcycles varies from the hundreds for number entry to tens of thousands for trigonometric functions. For example, the sine function averages 56,200 microcycles and has a worst case of 95,900.

The MM57109 uses a 9-volt power supply that can be split into +5 volts and −4 volts for partial TTL compatibility. The technology is PMOS metal-gate low threshold, and the typical current drain is only 12 mA. For more details, write National Semiconductor Corporation, 2900 Semiconductor Drive, Santa Clara, CA 95051.

NMOS and MOS/bipolar monochips

Interdesign's digital n-channel MOS silicon-gate monochip is the result of a joint project with Fairchild Semiconductor. The 138 × 138-mil IC has the equivalent of 262 gates.

Interdesign claims that this IC is more area-efficient than I²L, the logic design is more conventional than I²L, and is also directly TTL- and CMOS-compatible. This is the first of a series of closely stepped sizes which will allow optimum choice of size.



LARGEST LINEAR CHIP on the market. Interdesign's semicustom *Monochip F* contains 460 components.

Monochip E is 70 × 70-mils, has 200 components and 18 bond pads. Monochip F is 90 × 110-mils, has 460 components, including 10 MOSFET's and four high-current NPN's, and 24 bond pads. For information, write Interdesign, Inc., 1255 Reamwood Avenue, Sunnyvale, CA 94086. **R-E**