computer corner

Z-80 *How to interface the Z-80 to other devices and the associated timing*

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LAST MONTH, WE LOOKED AT THE THREE different ways the Z-80 can be interrupted. This month, we'll take a look at how the Z-80 can be interfaced to other devices.

Before discussing some real-world examples of interfacing, we'll look more closely at the interface timing diagrams and interfacing signals involved. The Computer Corner in the December 1977 issue briefly discussed CPU timing for the operation code-fetch portion of instruction execution. The timing for a memory read or memory write is similar except that the M1 cycle (operation code fetch) is not active during the read or write memory operation.

Figure 1 shows the timing diagram for a memory read and Fig. 2 shows the timing diagram for the memory write operation. They are usually three clock-periods long, unless slow memories are being used, in which case additional *wait* clock cycles can be activated by the slow external memory. The $\overline{MREQ}$ signal is used to signal the external memory that a valid memory address is on address bus lines A0–A15. If a memory read is being performed, signal $\overline{RD}$ is brought down to a logic 0. If a memory write is being performed, RD is a logic 1 and signal $\overline{WR}$ is a logic 0. Data is strobed into the CPU register during read operations at the indicated time, or is available for a memory write during most of the three write cycles.

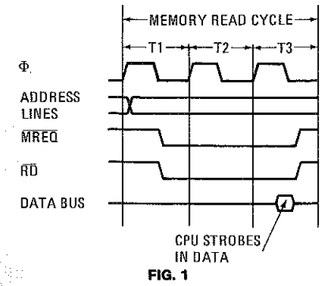

FIG. 1

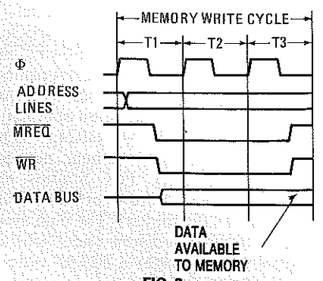

FIG. 2

Provision is made in the Z-80 microprocessor for interfacing to slower memories by the $\overline{WAIT}$ signal input to the Z-80. Bringing this signal down to a logic 0 informs the Z-80 CPU that external memory is not ready to transfer data. Figure 3 shows the result: It simply stretches the memory read or write time as long as required by slow memory.

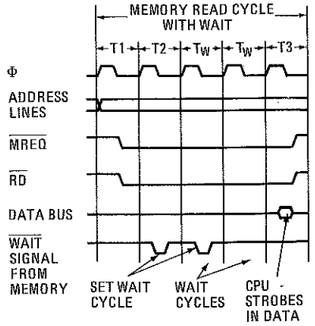

FIG. 3

I/O routines

Input and Output data transfers are initiated by unique I/O instructions. The CPU decodes these instructions and issues a special signal to indicate that data will be transferred to an I/O device, rather than a memory device. The Z-80 and the 8080 are different from most microprocessors in this respect since many microprocessors do not differentiate between memory addresses and I/O device addresses. Address decoding for many other microprocessors is done by the memory and I/O devices in a *memory-mapped* I/O scheme. The net effect is that some of the address range of this type of microprocessor must be dedicated to I/O device addresses, rather than to memory addresses alone.

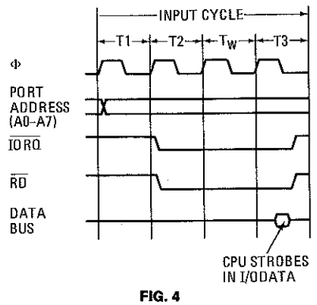

FIG. 4

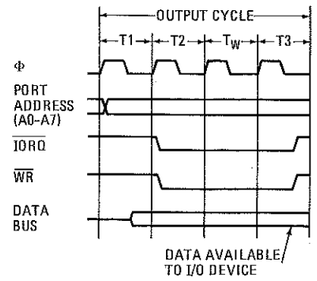

FIG. 5

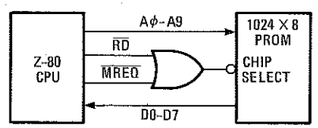

FIG. 6

Figure 4 shows the Input and Fig. 5 shows the Output cycles on the Z-80. Note that the major difference is in the $\overline{IORQ}$ signal that notifies the external I/O device that a valid I/O device address is present on address bus lines A0 through A7. The $\overline{RD}$ and $\overline{WR}$ signals are used in the same sense as in memory read and write operations. Note that input and output cycles are four clock cycles long, because the CPU automatically inserts an additional wait cycle to provide more time for the I/O device to respond. The I/O devices can also use the wait state capability provided by the wait input to synchronize slow-speed I/O devices with CPU execution of Input or Output instructions.

Figure 6 shows the operation of a Z-80 CPU with a 1024-by-8 bit PROM. This simple example allows for no I/O device interfacing and is for demonstration purposes only. Address lines A0–A9 are brought into the PROM to provide 10 bits of address (0–1023). Since presumably no write operations to the PROM will be performed in the program, the signals $\overline{RD}$ and $\overline{MREQ}$ are OR'ed together to provide a chip select signal to the PROM. Signal $\overline{RD}$ is not really necessary since every memory access is a memory read.

Figure 7 shows the same PROM storage with additional RAM storage to supplement the somewhat limited RAM storage of the CPU registers in the first example. Here, it is assumed that the RAM will not contain a program, and that it will provide storage for program variables computed in the course of program execution. In addition, the PROM memory is located at addresses 0000 through 03FF (ϕ through 1023_{10}), while the RAM addresses are 0400 through 04FF ($1024–1279_{10}$). Address-line 10 can therefore be used to decode whether PROM or RAM is being addressed. While $\overline{RD}$ and $\overline{WR}$ must both be provided to the RAM memory, only $\overline{RD}$ is used for the PROM. As in the first example, $\overline{RD}$ is a redundant signal for the PROM since a MREQ with address line A10 = 0 will guarantee that only the PROM is being addressed.

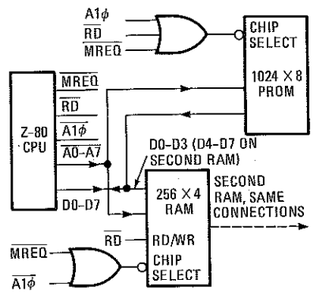

FIG. 7

In Fig. 8, an I/O device is added to the system. Since only one I/O device is used, signal $\overline{IORQ}$ alone is sufficient to inform the I/O device that it is being addressed. A second simplification here is that the I/O device is a read-only device and that no decoding of read-versus-write is necessary. Anytime the I/O device is addressed, the $\overline{IORQ}$ line is brought to a logic 0, and the device will output eight bits of data on the data bus. No address decoding is necessary either, since only one I/O device is used in this type of configuration.

The above examples are simple, workable interfacing examples for memory and I/O devices. Additional address decoding would be necessary in larger configurations, in addition to further gating and buffering of Z-80 outputs and inputs.

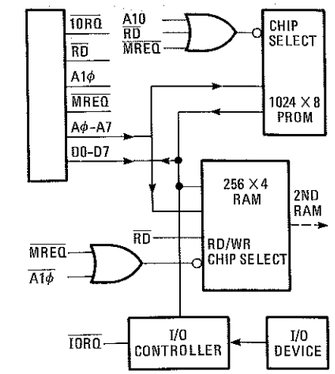

FIG. 8

While the 8080 microprocessor and updates to the 8080, such as the 8085, remain extremely popular and usable microprocessors, the Z-80 offers many advantages over the 8080. The Z-80 appears to be the microprocessor of the future, as short-lived as the future is in the world of microprocessors. We will be watching for up-dates and will keep you advised. **R-E**

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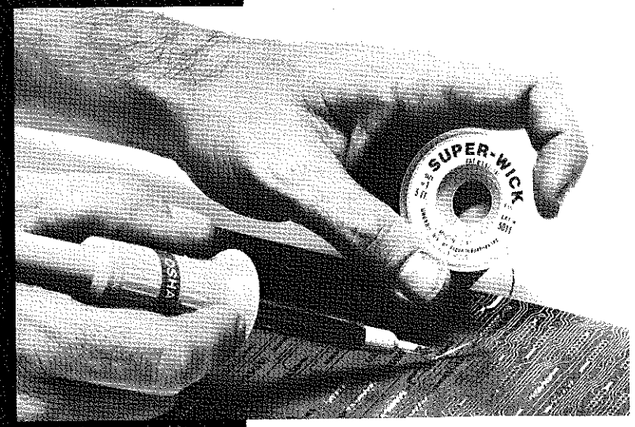

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