computer corner

8080 *A demonstration program for the 8253 timer.*

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IN A PREVIOUS COLUMN, WE INTRODUCED the characteristics of the Intel 8253 programmable interval timer, a 24-pin IC that is very useful in counting and timing operations.

This month's column describes a demonstration program that illustrates the various modes of operation of the timer.

The details of the test circuit are shown in Fig. 1. Although an oscilloscope is handy to monitor the output signal, OUTO, from counter No. 0, we have found it just as useful to use a single 7490

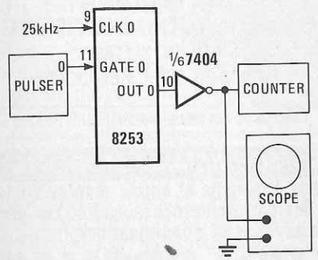

FIG. 1

decade counter IC to detect negative-edge transitions at output signal OUTO. The 25-kHz input clock frequency, which has a period, T, of 40 μs, is the input at CLKO.

Before you use the 8253 IC, you must understand the nature of output signal OUTO as a function of the IC's six different modes of operation: mode 0 through mode 5. Intel literature[1] is somewhat confusing in this area, so the diagrams have been simplified by omitting all signals except for the OUTO signal. This permits you to simultaneously compare all six operation modes, as shown in Fig. 2. Note that modes 0 and 1 provide a negative monostable clock pulse of duration NT; mode 2 provides a series of negative clock pulses of pulse width T and period NT; mode 3 provides essentially a squarewave of period NT; and modes 4 and 5 provide a single strobe pulse of pulse width T at a time NT after a trigger pulse has been applied to counter No. 0. Quantity N is a 16-bit timing byte initially loaded into counter No. 0. In our demonstration program, the timing byte is 000 000_8, which corresponds to the decimal number 65,536. At this point, there are two possible actions input GATE0 can take:

1. GATE0 functions as a *gating* input; when at logic 0, pulses that are input at CLKO do not reach counter No. 0 and no counting occurs. This type of behavior occurs with mode 0, mode 2, mode 3 and mode 4.
2. GATE0 functions as a *trigger/reset* input; a positive-edge transition at GATE0 resets counter No. 0 and initiates counting. Each time there is a positive edge at GATE0, counter No. 0 is reset. This type of behavior occurs with mode 1, mode 2, mode 3 and mode 5.

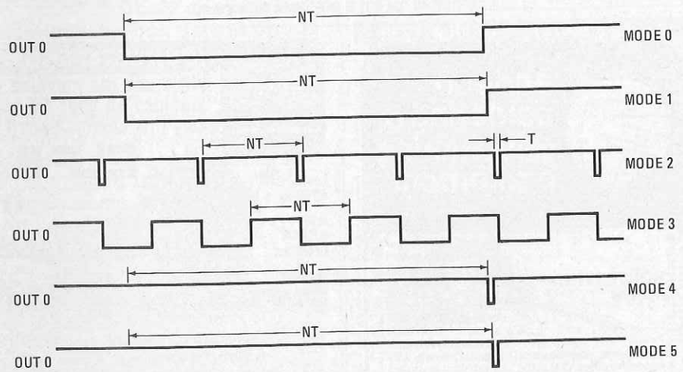

FIG. 2

These different actions can best be observed with the aid of a counter and a value of NT in the range of 3 to 10 seconds. In this case, the value of N is 65,536 and T is 40 μs; so NT = $(65{,}536)(40 \times 10^{-6}) = 2.62$ seconds.

The program that we use to test the 8253 IC is shown in Table 1. Note that a memory-mapped I/O (*I*nput/*O*utput) is used, in which the control register has an address of 200 003_8 and counter No. 0 has an address of 200 000_8. The program is quite simple. First output the control word, 060_8 (mode 0), into the control register. Next, successively load the LO and HI counter bytes, both of which are 000_8, into counter No. 0. Finally, enter a wait loop.

When you execute this program, output signal OUTO goes immediately to logic 0 and remains there for NT seconds, after which it returns to logic 1. You can repeat this behavior only by executing the program a second time starting at memory address 003 000_8.

If you change the control word at location 003 001 to 062_8 (mode 1), start the execution of the program and press the pulser shown in Fig. 1, you will also observe a negative pulse with a duration of 2.62 seconds. If you fail to press the pulser, however, and thus do not apply a positive edge at GATE0, you will observe no monostable pulse. On the other hand, repeatedly pressing and releasing the GATE0 pulse at time intervals of less than 2.62 seconds can prolong the monostable pulse indefinitely. In this way, you are able to produce a *retriggerable monostable multivibrator* input.

The control word of 064_8 lets you observe the mode 2 behavior shown in Fig. 2. Repeatedly generating positive edges at GATE0 at time intervals of less than 2.62 seconds repeatedly resets counter No. 0 and prevents the short negative clock pulses from appearing. You can accomplish the same purpose by allowing GATE0 to remain at logic 0 after you have applied a positive edge. The GATE0 input thus exhibits both gating and trigger/reset behavior.

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TABLE 1—DEMONSTRATION PROGRAM for the 8253 interval timer. The control word at address 003 001 is changed to demonstrate the behavior of the different modes of operation.

Address	Instruction	Label	Mnemonic	Comment
003 000	076	TIMER,	MVIA	/Move control word into accumulator
003 001	060		060	/Mode control word
003 002	062		STA	/Store it within control register
003 003	003		003	/in 8253 interval timer chip
003 004	200		200	
003 005	076		MVIA	/Move LO counter byte into accumulator
003 006	000		000	/LO counter byte
003 007	062		STA	/Store LO byte in counter #0
003 010	000		000	
003 011	200		200	
003 012	076		MVIA	/Move HI counter byte to accumulator
003 013	000		000	/HI counter byte
003 014	062		STA	/Store HI byte in counter #0
003 015	000		000	
003 016	200		200	
003 017	303		JMP	/Wait
003 020	017		017	
003 021	003		003	

The mode 3 behavior (control word of 066_8) is similar to that for mode 2, except that a nearly symmetrical squarewave is produced. Deviations from symmetry occur when the counter byte is an odd number, and are most evident when the counter byte is very small.

In mode 4 (control word of 070_8), the positive edge of the $\overline{WR}$ pulse, which is applied at pin 23 of the timer when you execute the STA instruction at 003 014, initiates counting that produces a negative clock pulse of pulse width T. The time duration between the positive edge and the pulse is 2.62 seconds. The GATE0 input acts as a gating input, with a logic 0 inhibiting the counting process.

Finally, in mode 5 (control word of 072_8), a positive edge at GATE0 initiates counting. Repeatedly generating positive edges at GATE0 at less than 2.62-second time intervals repeatedly resets counter No. 0 and prevents the appearance of the single negative clock pulse.

It should be noted that in all modes, counter action begins on the first negative clock transition after $\overline{WR}$ (pin 23) or GATE0 goes to logic 1; and that $\overline{WR}$ can initiate counting in all modes except mode 1 and mode 5.

Although in many 8253 timer applications, the primary purpose is to generate the proper output signal at OUTO (as shown in Fig. 2), you can also read the contents of the 16-bit counter *without affecting the counting operation.* By inputing a control word of 000_8, 100_8, or 200_8, you can latch the 16-bit count of either counter No. 0, counter No. 1, or counter No. 2, respectively. You can then read the two bytes into the 8080A IC, with the LO counter byte first and the HI counter byte second.

To discuss complex counter applications in any detail is beyond the scope of this article. However, a 16-bit frequency counter has been described elsewhere,[2] and a scheme has been proposed[3] for measuring the half-life of a radioactive substance. **R-E**

REFERENCES:

1. *Intel Data Catalog, 1977,* Intel Corp., 3065 Bowers Ave., Santa Clara, CA 95051.
2. Lynne, P., "Implementing an LSI Frequency Counter," *Byte 2* (11), 146 (1977).
3. DeJong, M. L., private communication. (Professor DeJong will implement a number of counting schemes in a physics laboratory, and would be interested in corresponding with others who have similar interests.)