HOW TO DESIGN DIGITAL CIRCUITS FROM SCRATCH

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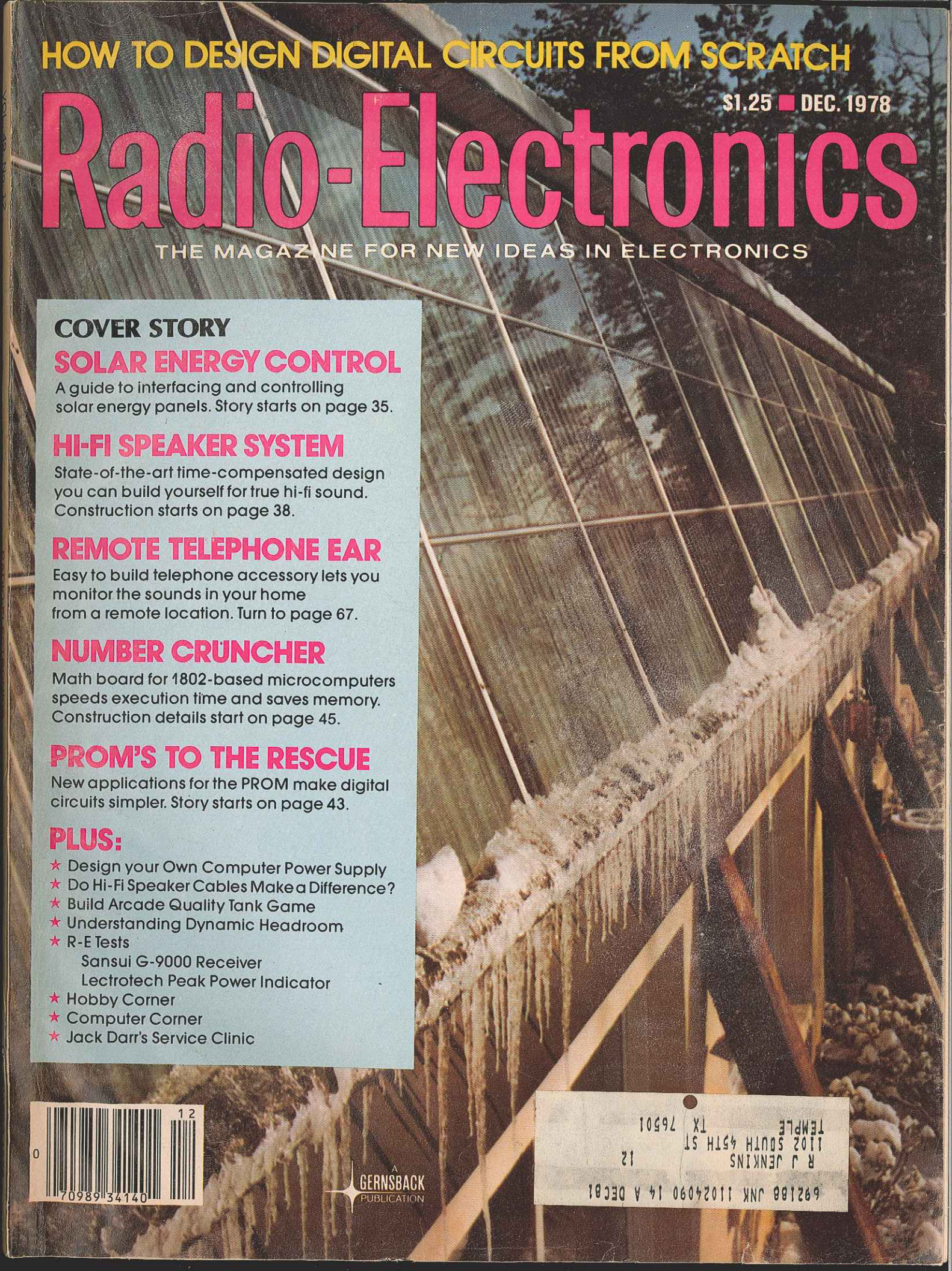
Radio-Electronics

THE MAGAZINE FOR NEW IDEAS IN ELECTRONICS



COVER STORY

SOLAR ENERGY CONTROL

A guide to interfacing and controlling solar energy panels. Story starts on page 35.

HI-FI SPEAKER SYSTEM

State-of-the-art time-compensated design you can build yourself for true hi-fi sound. Construction starts on page 38.

REMOTE TELEPHONE EAR

Easy to build telephone accessory lets you monitor the sounds in your home from a remote location. Turn to page 67.

NUMBER CRUNCHER

Math board for 1802-based microcomputers speeds execution time and saves memory. Construction details start on page 45.

PROM'S TO THE RESCUE

New applications for the PROM make digital circuits simpler. Story starts on page 43.

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- ★ Design your Own Computer Power Supply
- ★ Do Hi-Fi Speaker Cables Make a Difference?
- ★ Build Arcade Quality Tank Game
- ★ Understanding Dynamic Headroom
- ★ R-E Tests
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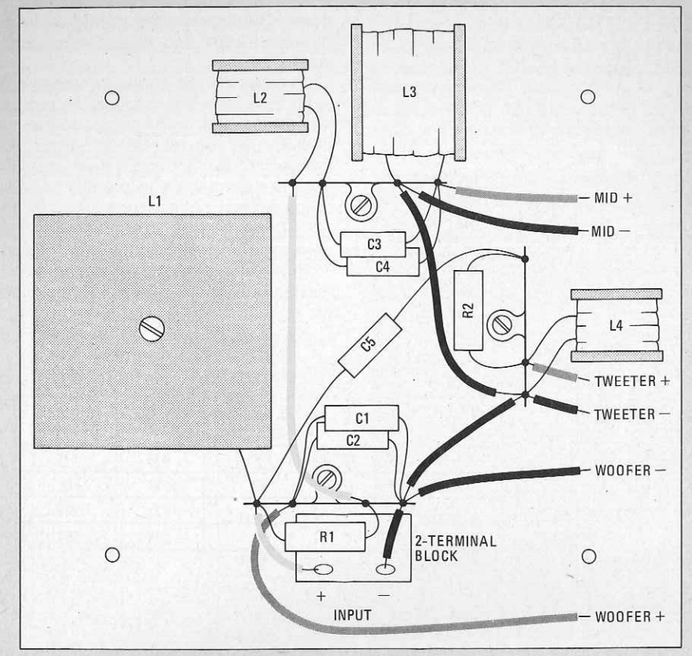

FIG. 16

With a driver in place, use the mounting holes as guides to drill the screw holes into the mounting board. For the mid-range driver and tweeter, use a 5/64-inch drill. The mounting holes for the woofer are 9/64 inch.

Next, fill the woofer compartment with glass-fiber insulation material (Fig. 17). Ordinary pink home insulation material 2 or 3 inches thick can be

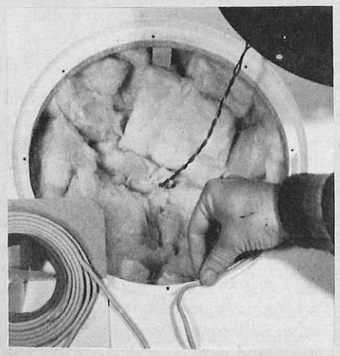

FIG. 17

used. A roll of this insulation costs less than the small packages of acoustic glass-fiber material needed to fill two systems. Insulation performance is the same or better, and you can use the remainder in your attic or under the hood of the family car.

Remove the vapor-barrier backing and cut the glass-fiber into small pieces. This will produce the smoothest bass response. Three-inch cubes will do nicely, although size is not too critical. Wear rubber gloves to avoid possible irritation to your hands. Fill the enclosure completely with loosely packed insulation material. And make sure to fill under the brace, G. No material is needed in the upper compartments because both the mid-range driver and the tweeters have sealed backs. The drivers can now be connected and installed.

Solder the color-coded wire to the positive terminal and the black wire to the negative lead. A red mark on or near the terminal indicates it is positive; if no mark appears, briefly connect a 1½-volt battery to the terminals. When the speaker diaphragm moves away from the magnet, the positive end of the battery is connected to the positive lead of the speaker. The mid-range driver and tweeter can be installed using No. 6 × ½-inch sheet-metal screws. The woofer can be installed with No. 10 × ¾-inch sheet-metal screws. Place caulking compound only around the woofer; it should be placed between the woofer basket and the woofer subpanel, L (see Fig. 18). Again, this insures a seal in the woofer compartments.

The foam grille can be cut and installed using the self-adhering strip that comes with the grille along with cutting instructions. Three grille packages are all that are needed to cover two systems. This completes the assembly. R-E

SPEAKER SYSTEM PARTS LIST

The following items are available from McGee Radio & Electronic Corporation, 1901 McGee Street, Kansas City, MO 64108:

Part No. AD12250 W8: Two 12-inch Norelco woofers, two for $77.

Part No. AD0211 SQ8: Two 2-inch soft-dome Norelco mid-ranges, $19.95 each. (This part not in McGee catalog but available.)

Part No. AD0162 T8: Two 1-inch dome tweeters, $9.95 each.

Two 3-ohm 5-watt resistors, $.20 each.

Two 6-ohm 5-watt resistors, $.49 each.

The following items are available from Radio Shack stores:

Part No. 272-999: Four 10-μF, 50-volt nonpolar capacitors, $.99 each.

Part No. 272-998: Six 4.7-μF, 50-volt nonpolar capacitors, $.89 each.

Part No. 274-688: Two 5-lug terminal-strip packs of 4, $.69 each.

Part No. 274-621: Two terminal boards, $.99 each.

Part No. 40-1951: Three foam grilles, $5.95 each.

Miscellaneous: One roll of glass-fiber insulation (approximately $5.95); two 4-foot by 8-foot sheets of ¾-inch particle board ($17); five ½-lb (100-foot) rolls No. 18 magnet wire; two ¼-pound (93-foot) rolls No. 22 magnet wire; two ¼-pound (150-foot) rolls No. 24 magnet wire; white glue ($1.79); eight No. 8 × 1-inch sheet-metal screws; 16 No. 10 × 1-inch sheet-metal screws; 14 No. 6 × ½-inch sheet-metal screws; 2 flat-head brass wood screws; hookup wire; solder; paint; caulking compound; hardwood bracing; 8-foot-long two-by-four; 1¼-inch finishing nails.

CABINET LUMBER DIMENSIONS

To construct the cabinet for the time-compensated speaker system, the following lumber should be purchased:

¾-inch-thick flakeboard:

Top panel (A): 3⅜ inches × 16 inches
Tweeter board (B): 4¼ inches × 16 inches
Tweeter bottom (C): 5⅜ inches × 16 inches
Mid-board (D): 7⅛ inches × 16 inches
Woofer top (E): 13¼ inches × 16 inches
Woofer bottom (F): 14 inches × 16 inches
Mid-brace (G): 6¾ inches × 16 inches
Back panel (H): 31⅜ inches × 16 inches
Side panels (I & J): 32⅞ inches × 14¾ inches (see Fig. 2)
Woofer board (K): 21½ inches × 16 inches
Woofer board (L): 13¼ inches × 16 inches

⅜-inch-thick flakeboard:

Mid-board (M): 7⅛ inches × 16 inches
Tweeter board (N): 4¼ inches × 16 inches

¾-inch hardwood:

Braces (O & P): 12 inches × 2½ inches
Brace (Q): 10 inches × 2½ inches

2 × 4 inch fir:

Base (R & S): 12¼ inches
Base (T & U): 15 inches

Making PROM'S Work For You

The programmable read-only memory is becoming the workhouse of modern digital electronics and will play an ever-increasing role in your everyday activities. Here is what it's all about.

ROBERT H. PENOYER

THE PROM (*PROGRAMMABLE READ-ONLY Memory*) is increasingly being accepted as a circuit element. The electronic hobbyist or home computer owner should become familiar with this very useful device. Because there have been numerous articles written about both the PROM and the EPROM (*Erasable* PROM), this article will just briefly mention their theory of operation, and concentrate on the ways these devices can be put to use.

What is a PROM?

Figure 1 shows the basic configuration of a 16 × 4-bit PROM; that is, there are 4 address lines, and, therefore, $2^4 = 16$ states can be represented. Each of these 16 states is decoded into a single control line that leads to a set of junctions in the memory array. These junctions are either closed or fused open depending upon how the PROM is programmed. The logic state of the junctions selected by the address decoder passes through the buffer and appears at the output. Figure 1 shows 4 output lines; thus, there are $2^4 \times 4$ or 16 × 4 junctions. This PROM can also be described as containing 16 words with 4 bits-per-word. There are as many words as there are address states. Therefore, if the PROM had eight address lines and one output line, it would be a $2^8 \times 1$-bit or a 256 × 1-bit PROM, or containing 256 1-bit words.

Just as there are closed or fused-open junctions in a PROM array, the EPROM uses static charges on MOSFET transistors to achieve the effects of an open or closed junction. The charges on the MOSFET's can last for years or be erased in a few minutes by special ultraviolet lamps.

Using the PROM

The PROM serves two main purposes: First, a single PROM IC can replace an entire multiple-gate logic array. Say, for example, you needed a set of gates that would perform the function described in the truth table of Fig. 2. If standard gates were used, a complex network would result. Instead, let the four left-hand columns of Fig. 2 represent the address lines, and let the column on the right represent the output line of a 16 × 1-bit PROM. Thus you would achieve the desired function using only a single IC. The result is a savings in wiring time, troubleshooting time and board space.

The second main use of a PROM is as a "look-up table." For example, suppose you wanted a counter to count in the sequence shown in the right-hand side of Fig. 3. This could be extremely difficult to accomplish using ordinary logic. Instead, you can apply the output lines of an ordinary binary counter to the address lines of a PROM. Upon reaching any of the 16 possible states, the counter causes the internal logic of the PROM to "look up" the desired output state and pass it through its buffer to the output, according to the truth table. Only two IC's, a 4-bit binary counter and a PROM are needed to arrive at a rather complicated sequential output.

Another example of using a PROM as a look-up table is a Baudot to ASCII code translator. The Baudot code can act as the address for a PROM, and the PROM output can yield equivalent ASCII characters.

Propagation delay and access time

As with any logic device, propagation delays in PROM's are important, particularly so if a PROM's output lines are used to drive counters or clocked logic of any type.

A specifically limited amount of time is required to receive an address, decode it, drive a set of junctions in the PROM array and transmit the result through the buffers to the PROM output. This is called the PROM's access time, and is

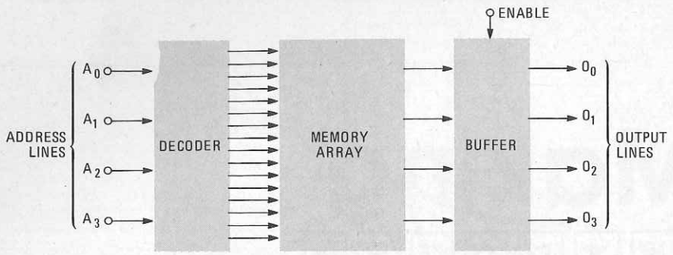

FIG. 1—PROM consists of an address decoder, output buffer and memory array.

A_0	A_1	A_2	A_3	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

FIG. 2—COMPLEX LOGIC FUNCTIONS such as the one shown in the above truth table can be easily handled by a PROM.

A_0	A_1	A_2	A_3	O_0	O_1	O_2	O_3
0	0	0	0	0	0	1	0
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	0
0	0	1	1	1	0	1	1
0	1	0	0	1	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	1	0	1	1
0	1	1	1	1	1	0	1
1	0	0	0	1	1	1	0
1	0	0	1	1	1	0	1
1	0	1	0	1	0	1	1
1	0	1	1	0	1	1	1
1	1	0	0	1	1	1	1
1	1	0	1	0	0	0	0
1	1	1	0	1	0	0	1
1	1	1	1	1	0	1	0

FIG. 3—COUNTERS with an unusual counting sequence can easily be designed using a PROM.

listed in the manufacturer's data sheet. During the access delay time, the state of the output lines on a PROM is unpredictable. A set of outputs can pass through several states during the transition from one address to the next. Therefore, if the outputs are driving clocked logic, the logic could receive undesired data. Obviously, this should not be allowed to happen. Luckily there are methods to get around this problem.

Buffer and latch isolation

As shown in Fig. 1, the output buffer of the PROM often has an enable control line. Typically, this enable line is used to select the device that is to be connected to a parallel bus system when many such tri-state devices are used. When enabled, the buffer outputs are at normal logic levels. When not enabled, the buffer outputs appear to be open circuits. If all the buffer output lines are pulled to +V through, say, 10K resistors (in the case of TTL logic) then when the output lines are disabled they will be at a known high logic level. Therefore, no output line can go low unless that particular bit was programmed low and the PROM output was enabled. Thus, it is only necessary to disable the output when changing addresses. Using such an arrangement, no glitches appear at the output and low-going pulses appear only when desired. Figure 4 shows a typical circuit using this technique.

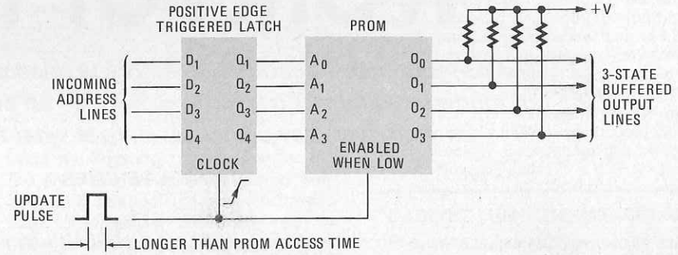

FIG. 4—DISABLING PROM during access time prevents glitches from appearing at the output.

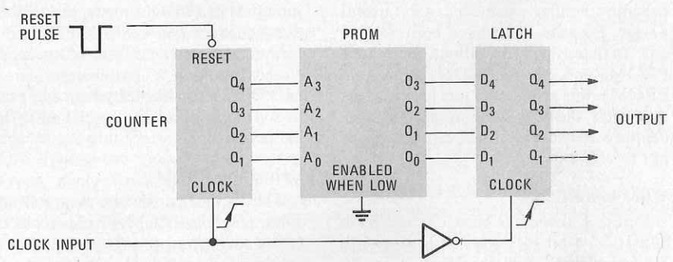

FIG. 5—CLOCK SIGNAL in synchronous circuits can be used to inhibit output during access time.

You can use a similar more desirable technique that requires no pull-up resistors on the buffered output lines. Let's say, for example, you want a circuit that counts as shown in the Fig. 3 truth table. Also assume that you could not arbitrarily allow the outputs to go high, as shown in Fig. 4.

Figure 5 shows an alternative technique: a synchronous binary counter drives the address lines of a PROM that is programmed according to the truth table shown in Fig. 3. Therefore, as the counter passes through each binary state, the desired output appears on the PROM output lines. These lines are always enabled as shown in Fig. 5. Note that both the counter and the latch are triggered by positive-going clock edges, and there is an inverter in the latch clock line. This means that while the counter still triggers on the positive-going edge of the clock, the latch will trigger on the negative-going edge. This provides a delay of one-half clock period between the time the counter is updated and the resulting PROM output appears at the latch output. If the PROM access time is shorter than one-half clock period, its output will be settled by the time the latch uses it. The result is a clean accurate set of waveforms at the latch output.

PROM sources

PROM's and EPROM's are available in many configurations. Just check through manufacturers' catalogs for the type of PROM you need for your application. Sometimes the required number of words and word length are not available and you have used a PROM with more words or bits than you need. In this case, you should consider the economics of wasting PROM capability.

Most large distributors can program a PROM for you if you purchase it from them. Find out all the necessary information before placing the order for your PROM; often the distributors will program the device for a small fee or at no additional cost. **R-E**

BUILD THIS

NOM Card For The 1802

Add-on math board for an 1802-based microcomputer. Based on a number-crunching IC, this board speeds execution time, reduces software overhead and saves memory

L. STEVEN CHEAIRS

NOW THAT YOU HAVE YOUR RCA 1802-based microcomputer up and running, what do you do next? You might consider putting it to some serious work, but in doing so, you will probably run into the software wall. In other words, for most applications a good deal of programming will be required, and a good portion of it will be for mathematical operations. It's also a known fact that you can age very rapidly writing all the software needed to perform the required mathematical operations.

One alternative is to use hardware instead of software to perform these operations. The first idea I had was to use a scientific calculator IC. This would certainly reduce the software development time, leaving me only the interfacing to worry about. While this apparently solves the software problem, it creates a Pandora's box full of new ones.

First, most calculator IC's have on-chip debounce circuitry designed to solve the problems generated by multiple character entry due to noisy keyboard switches. This is a very positive feature for a calculator, but, unfortunately, it tends to slow a microprocessor down.

Second, a calculator IC in its natural habitat is interfaced to a keyboard via a set of multiplexed input/output (I/O) pins. This requires complex interfacing to convert incoming data into the signals necessary to imitate a keyboard switch. While this is not an impossible task, it is a bit messy.

Third, a calculator is designed to stand alone, not act as a slave processor for a microcomputer system. The data is outputted in a multiplexed 7-segment, non-TTL format. Multiplexing data is not only acceptable but desirable. On the other hand, a 7-segment format is not exactly the easiest format for a computer to manipulate. It could of course be converted to a BCD (*B*inary-*C*oded *D*ecimal) format by several methods, such as a software look-up table, or a PROM could be programmed to convert a minimum of five input lines into the four BCD output lines. Another point to consider is that the calculator IC's do not have the control lines required to interface it to the processor.

You could try another approach, such as dedicating a CPU and a ROM as a mathematical processor. National Semiconductors has done just that with its new Number-Oriented Microprocessor (NOM). This special-purpose microprocessor, the MM57109, is available through distributors. This single IC will provide most, if not all, of the mathematical operations needed for any computer system. The software overhead is drastically reduced when this processor is used.

The MM57109

Figure 1 is the internal block diagram of the MM57109, showing both the signal lines and their point of origin. The internal register file is composed of five

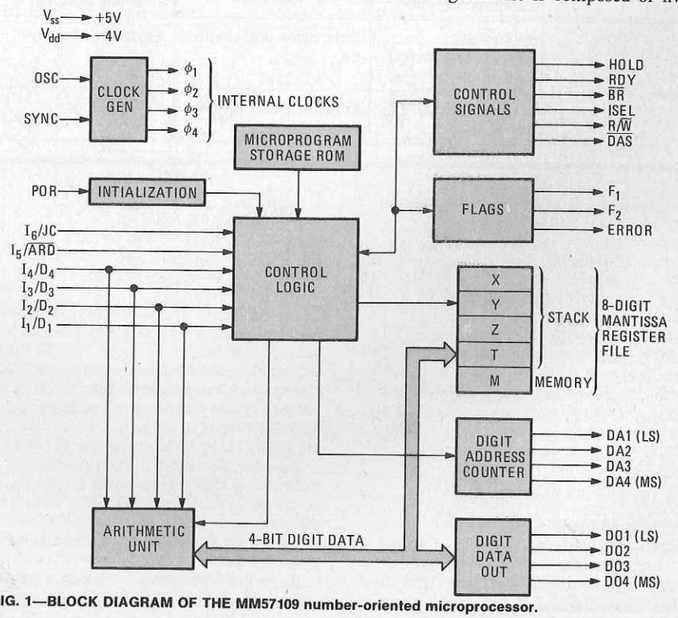

FIG. 1—BLOCK DIAGRAM OF THE MM57109 number-oriented microprocessor.

registers (X, Y, Z, T and M); each has eight mantissa digits, two exponent digits, a decimal-point position indicator, and the mantissa and exponent sign bits. The program-storage ROM stores about 1500 eight-bit micro-instruction words. The 6-bit-long program instructions enter through the $I_{1\text{-}6}$-lines and are converted into a sequence of these micro-instructions. The BCD data words enter the control logic via the $I_{1\text{-}4}$-lines.

Data is outputted, after receiving the OUT instruction, through the digit-data-out block. The digit-address-counter block sequences each digit during the I/O operations. The Read/$\overline{\text{Write}}$ control line is used during the OUT instruction to latch the data words into the interface register.

Figure 2 shows a table of the MM57109's important features. These features can be classified into four categories: scientific calculator-type instructions, I/O, branch control and interface.

Basically, the MM57109 looks like an RPN (*R*everse *P*olish *N*otation) scientific calculator. The only major difference is in the I/O and control-interface circuitry. National Semiconductor engineers state that the MM57109 is a *modified* scientific calculator. First, we'll take a look at the 1802-type interface; then, the instructions and programming techniques will be discussed. If you are not yet convinced that the MM57109 is the way to go, then look at Table 1. As stated earlier, the NOM is very easy to interface to almost any computer system. The MM57109 is only one of two NOM interfaces that Questar Engineering is marketing; the other is for the S-100 bus.

Instructions	Input/Output	Branch Control	Interface
RPN	HOLD for asynchronous and single step operation	Conditional and unconditional program branching	Single phase clock
1 to 8-digit mantissa	Asynchronous digit input instruction (AIN) *with* AIN ready (ADR) input	Increment/decrement branch on non-zero for program loops	Low power operation
2-digit exponent	Multidigit I/O instructions (IN, OUT)		Generation of I/O control signals
Four-register stack, one-memory location	Floating point or scientific notation		Separate digit input, output, and address bus
Trigonometic functions, logarithmic functions, Y^x, e^x, π, etc.	Programmable mantissa digit count for IN, OUT instructions		
Error Flag	Sense input and flag output		

FIG. 2—FEATURES OF THE MM57109 that are important to the NOM card constructor.

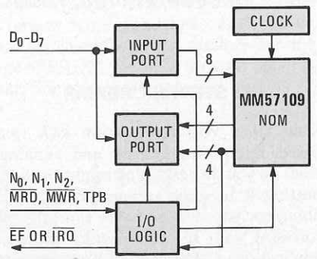

FIG. 3—1802 MICROPROCESSOR INTERFACE for the MM57109.

Circuit operation

The basic circuit operation is shown in the block diagram of Fig. 3, while the complete schematic is shown in Fig. 4. The I/O signals (N_0, N_1, N_2, TPB, $\overline{\text{MRD}}$, $\overline{\text{MWR}}$) from the 1802 are decoded, and are used to move data into and out of the NOM via two 8-bit data latches. One-half of the data output port, D_0–D_3, is the BCD data from the NOM, while the other 4 bits are used to provide status information to the 1802 CPU. Note that the address counter digit from the NOM is not provided. This is because the address digit requires 4 bits of the I/O port (thus requiring a second output port). This may seem like a poor decision just to save one output port, but it is not. The output format of the NOM is defined by the internal architecture, and with a minor amount of software added to the 1802's program, the same information may be derived. Figure 5 shows the data formats for both the scientific-notation mode and Fig. 6 shows the floating-point mode.

The other 4 data bits inform the 1802 of the NOM's status; also any of these 4 bits can be configured to output an active low signal, which should be used to set one of the event flags or initiate an interrupt. Bits D_0–D_3 of the input port supply the instructions to pins I_1–I_6 pins; input data is placed on the D_0–D_3 lines and enters through I_0–I_3. The 1802 uses the upper input data, bits D_6 and D_7, to reset and/or halt the NOM. This data is shown in Fig. 7, along with port decoding information.

The control logic is actually quite simple; and in fact, the whole circuit is also very simple. It can be described in three parts—the *input decode*, the *NOM status register* and the *interrupt request circuitry*.

The input decode circuit is formed by IC3, IC4 and IC9-a. These IC's are used to decode $\overline{N}_0$, N_1, $\overline{N}_2$, MRD, and TPB

TABLE 1—Comparison of MM57109 to the Average Microprocessor and Calculator IC's

	MM57109	MICROPROCESSOR	CALCULATOR
Speed (math or I/O)	0.5–400 ms	0.5–500 ms	14–400 ms
Data length	Variable (1- to 8-digit mantissa)	Fixed	Fixed
Data format	Floating point, and scientific notation	Binary	Floating point, and scientific notation
I/O	Multidigit, asynchronous digit and single bit	Data bytes and single bit	Keyboard/display
Program	External ROM/PC, μP or FIFO	External ROM, internal PC	Key sequence

PARTS LIST

All resistors ½ watt, 5% unless noted.
R1–R5, R17, R18—10,000 ohms
R6—300 ohms, ½ watt
R7—1000 ohms
R8—18,000 ohms
R9, R10, R12–R15—2000 ohms
R11, R16—9100 ohms
C1, C5—1-μF, 35-volt, electrolytic
C2, C3, C8, C11, C12—0.01-μF, disc
C4, C9, C10—100-pF, disc
C6, C7—10-μF, 20-volt, electrolytic
D1—1N703 Zener diode (or equal), 3.9 volts
IC1, IC2—4508, dual 4-bit latch
IC3, IC13—4069, hex inverter
IC4—4073, triple 3-input AND gate
IC5, IC6, IC8—4013, dual D-type flip-flop
IC7—4049, hex inverter buffer
IC9—4528, BCD-to-decimal decoder/binary-to-octal decoder
IC10—DS8800, dual TTL-to-MOS voltage converter
IC11—MM57109, NOM
IC12—4072, dual 4-input OR gate
S1–S4—DIP switch (8 SPST switches)
Misc.—One 28-pin DIP socket for IC11, and a PC board.

The following are available from Questar Engineering Co., 50 S. MacDonald St., Mesa, AZ 85202:
PC board, predrilled and etched, $33
Complete kit of all parts, $98
Elf II to SB-44 converter card, $6.95
MM57109 NOM IC, $18
DS8800 TTL-to-MOS converter IC, $6.45.

Questar also has a PROM containing a subroutine that will perform all the power-up housekeeping and FIFO interface between the 1802 and the NOM. Also included on the PROM is a monitor-type software package, $28.50.

Note: The decision to use a dual 22-pin card was based on the fact that this card has been a standard component of the electronic field for many years. The Vector-size card and hardware are readily available and less expensive than other components. There are a variety of other printed-circuit cards using this same bus, a few of which will be available in the future. These PC cards include a Vector-type graphic display that uses an oscilloscope as a display; a 2K-byte EROM/2K-byte low-power RAM card; and a nonvolatile 4K-byte RAM board; the EROM's are programmed in place on the card. This permits the EROM to be treated like a RAM, plus a program can be developed in RAM and transferred to EROM without unplugging any components. The program can then be executed immediately from the EROM.

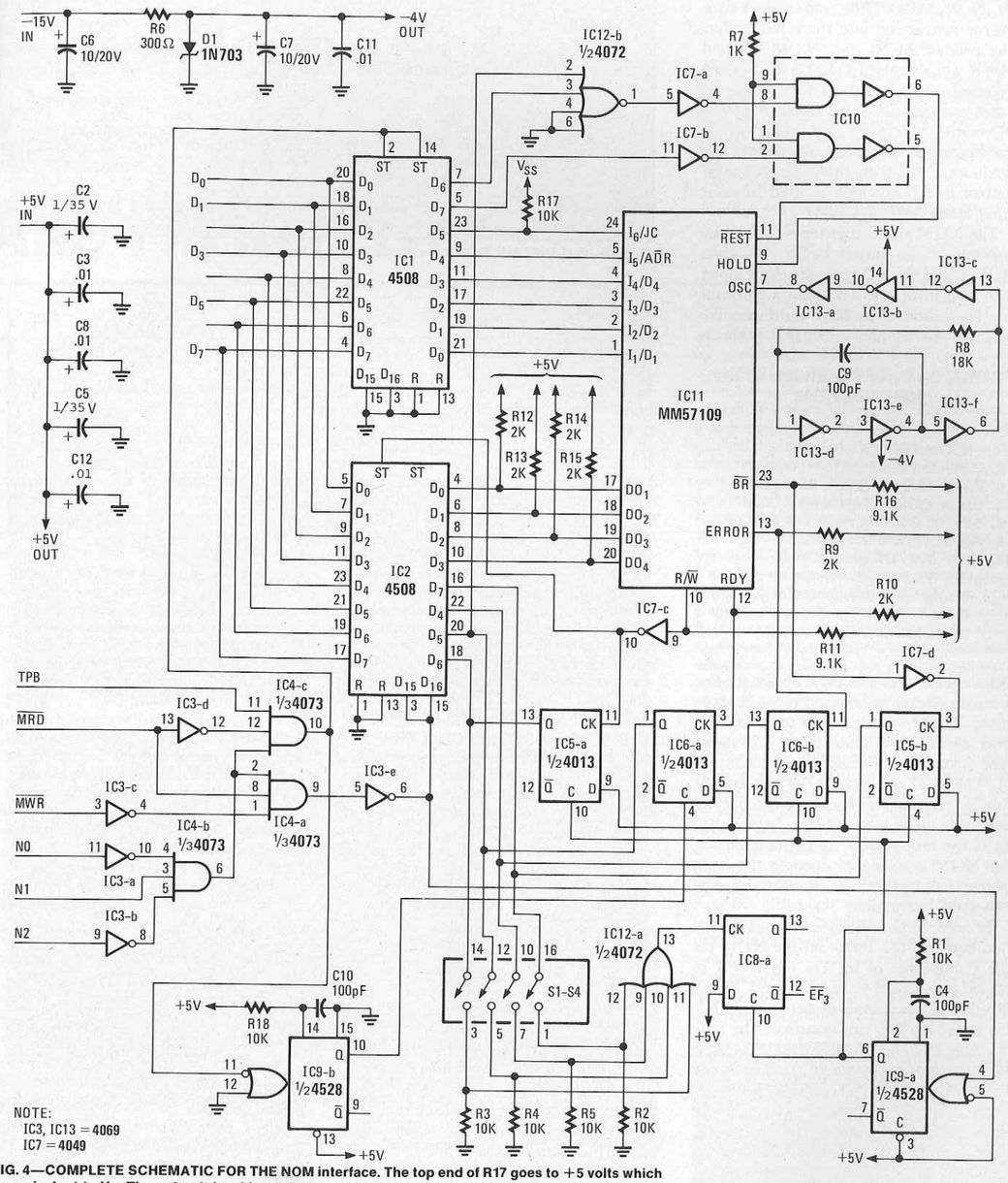

FIG. 4—COMPLETE SCHEMATIC FOR THE NOM interface. The top end of R17 goes to +5 volts which is equivalent to V_{ss}. The −4-volt level is equivalent to V_{dd}.

($\overline{N}_0.N_1.\overline{N}_2.MRD.TPB$), and to clock data and/or instruction into the input buffer. The product of $\overline{N}_0$, N_1, $\overline{N}_2$, $\overline{MRD}$, and MWR ($\overline{N}_0.N_1.\overline{N}_2.\overline{MRD}.MWR$) is used to enable the output buffers allowing status information and data from the DO_0–DO_3 output of the NOM to be transferred to the 1802. One-shot IC9-a produces a pulse on the falling edge of control line N2, which is used to reset input-ready flip-flop IC6-a.

The NOM status register is formed by one-half of the output buffer, IC_2 (bits D_4–D_7), and four D-type flip-flops along with two inverters. The least significant bit, D_4, is the error flag; eight possible types of errors are shown in Table 2.

TABLE 2—Error Conditions of the MM57109 NOM

1. LN X and LOG X when X 0
2. When any result is 10^{-99} or 10^{100}
3. When TAN 90°, 270°, 450°, etc.
4. SIN X, COS X, TAN X for X 9000°
5. $SIN^{-1}X$, $COS^{-1}X$ for X 1 or X 10^{-50}
6. For SQRT X when X O
7. For /, INV, 1/X when X = 0
8. In the floating-point mode for the OUT instruction if the number of digits to the left of the decimal point is equal to the Mantissa Digit Count.

Whenever an error occurs, an ECLR (*E*rror *F*lag *C*lear) instruction must be executed. The error flag can be tested at any time by the TERR instruction, a branch-type instruction (branches if ERROR = 1). The 1802 can also check this condition by reading the D_4 bit of the output port; this bit is reset after its access. Bit D_5 is the input-ready signal; it indicates the NOM is ready to execute the next instruction or to get the second word of a two-word instruction.

In order to permit asynchronous operation between the 1802 and the NOM on the rising edge of bit D_5, the NOM is placed into a hold state, hold = 1. When flip-flop IC6-a is reset by control line N2 (as stated earlier, this occurs on the falling edge of control line N0, which is used to load new instructions into the input port) the NOM will execute the next instruction. When the user's program is informed by bit D_5 that the input is ready, then the program provides the next instruction to the NOM.

Bit D_6 is the output-ready signal. Upon receiving this information, the user program stores the data into a software FIFO—a table in memory that acts like a first-in/first-out memory. The reason that a software FIFO is needed is due to the method in which the NOM outputs data. An OUT instruction is sent to the NOM, which, in turn, causes the NOM to output the first digit. Ten microseconds later, the output-ready flip-flop is set, and the DO_1–DO_4 output bits are clocked into the lower bits (D_0–D_3) of the output port. This data must be read and the flip-flop cleared (by reading the port) within 140 μs because the second digit will be outputted at that time. Every 140 μs, a new digit will be made available, along with a data-ready signal, until the full number is outputted. The last bit, D_7, is the branch signal. This signal indicates a program branch has been encountered; input ready is set during this signal.

The interrupt-request circuitry is formed by the 4-input OR gate, IC12-a, and the D-type flip-flop, IC8-b, along with a DIP switch and four pull-down resistors. The four status signals (error, input ready, output ready and branch) are connected to a 4-input OR gate via a set of SPST switches, along with the pull-down resistors. This permits any of the status signals to clock a logic 1 into the D-type flip-flop, providing a total of 16 possible interrupt (or event-flag) conditions. For example, if you're only interested in knowing when the output is ready (this implies that no branch instructions are to be used, that the data/instructions inputted are free of errors, and sufficient time is allowed between instructions so that a new instruction can never be inputted in the middle of an instruction already being executed), then all but the output-ready switches are opened. Thus, a logic 1 is clocked into IC8-b only when the output-ready signal is active. The $\overline{Q}$ output relays this information to the 1802 via either the $\overline{IRQ}$, or one of the four event flags ($\overline{EF}_1$,

continued on page 79

DA_4-DA_1	IN: D_4 OUT: DO_4	D_3 DO_3	D_2 DO_2	D_1 DO_1
0	Most Significant		Exponent Digit	
1	Least Significant			
2	Sign (Mantissa)	0	0	Sign (Exponent)
3	Unused			
4	Most Significant Mantissa (Followed by Decimal Point)			
.	.			
.	.			
.	.			
Mantissa Digit Count + 3	Least Significant Mantissa Digit			

FIG. 5—IN/OUT INSTRUCTIONS (Scientific Notation Mode).

DA_4-DA_1	Decimal point position	IN: D_4 OUT: DO_4	D_3 DO_3	D_2 DO_2	D_1 DO_1
2		Sign (Mantissa)	0	0	0
3		Decimal Point Position			
4	11	Most Significant Mantissa Digit=0-9			
.	10	.			
.	.	.			
.	.	.			
.	.	.			
Mantissa Digit Count + 3	12-Mantissa Digit Count	Least Significant Mantissa Digit=0-9			

Where: DA_1-DA_4 is the digit address
DO_1-DO_4 is the digit data out
D_1-D_4 is the digit data in

Also: The mantissa digit count is set by the SMDC instruction, initially it is equal to eight.
For the sign of the mantissa zero represents positive and one represents negative.
The sign of the exponent is equal to zero in the floating point node.
The decimal point position indicator is a value in the range from 11 down to (12-mantissa digit count), which indicates a digit, as given by the decimal point position indicator column in the table. The decimal point is located to the right of this digit.

FIG. 6—IN/OUT INSTRUCTIONS (Floating-Point Mode).

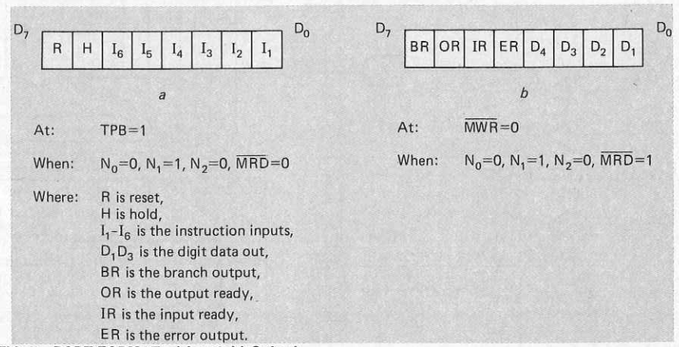

FIG. 7—PORT FORMAT. a) Input; b) Output.

Radio-Electronics Tests Sansui G-9000 AM/FM Receiver

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CIRCLE 104 ON FREE INFORMATION CARD

LEN FELDMAN
CONTRIBUTING HI-FI EDITOR

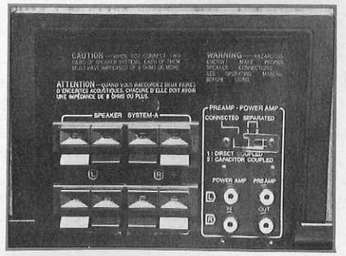
SANSUI'S TOP RECEIVERS THIS YEAR ALL feature a DC-configured power-amplifier section. This means that there are no input coupling capacitors to the power section, and that all capacitors in the feedback network have been eliminated. The advantages claimed for this circuitry are in improved transient response (lower transient intermodulation distortion) and a frequency response that goes right down to DC. The audible difference between an AC-coupled amplifier and a DC-coupled one may be subtle to inexperienced listeners, but serious audiophiles report somewhat cleaner and more accurate sound reproduction from such DC-configured circuits.

From our point of view, the Sansui *model G-9000* offers a good deal more than just a DC amplifier. The front panel, shown in Fig. 1, is loaded with features that will delight the audio buff seeking maximum control and flexibility. The light-colored, sloped frequency scales (the FM scale is linearly calibrated with markings at every 200 kHz) are surmounted by four well-illuminated meters, two of which are power-output meters, logarithmically calibrated from 0.1 watt to 300 watts (referred to 8-ohm loads). The other two meters are signal-strength and center-of-channel indicators for the tuner. To the left of the meters are four indicator lights, two showing which speaker pair is activated; the other two serve as a power-on indicator and a "protector" indicator. The protector indicator flashes intermittently for a few seconds when the power is first turned on until voltages have been fully stabilized, after which sound is heard from the speakers.

Five indicator lights to the right of the meters denote the program source selected. A series of positive-feel toggle switches just below the dial area to the left handle power, speaker selection, bass and treble control turnover frequencies (200 Hz or 400 Hz for the bass control, 3 kHz or 5 kHz for the treble), tone control defeat and −20 dB audio muting. Similar toggle switches to the right handle FM muting, stereo or mono listening modes, 25-μs or 75-μs de-emphasis, FM noise filter and wide or narrow bandwidth for the FM IF circuits. A microphone mixing level control and microphone input jack are located at the extreme lower right-hand side of the panel.

Major controls along the bottom of the front panel include BASS, TREBLE and MID-RANGE tone controls (each with fixed, detented steps for easy resetting), balance control, program SELECTOR switch and TAPE MONITOR switch (with positions for monitoring either of two connected tape decks or dubbing from one to another). Two massive knobs in the center of the panel take care of frequency tuning (the smoothest-acting flywheel-dial arrangement we've ever experienced) and master volume-control settings. The volume control contains an index tab that can be set at preferred maximum listening levels. Its clutch-like action prevents the volume control from being accidentally turned to overload or excessive listening levels—a nice feature if there are young children in the house who might inadvertently turn the volume all the way up and destroy speaker voice coils in the process! Three square pushbuttons between these two large controls activate subsonic and high-cut filters as well as the loudness compensation circuits. A similar pushbutton near the program selector switch provides a third circuit-interruption point for the insertion of a four-channel adapter, graphic equalizer, audio time-delay unit, or a Dolby noise-reduction adapter. A headphone jack just below the POWER switch on the lower left completes the panel layout.

The rear panel of the *model G-9000* contains three AC convenience outlets (one switched, two unswitched). One of the most pleasing physical features of this receiver is how the input/output jacks and terminals are positioned. These connections are located in recessed areas in the *side* wood panels of the unit, rather than at the rear. All input and (tape-out) terminals, as well as AM and FM antenna terminals, can be reached from the right side of the unit, while two sets of spring-loaded speaker terminals, preamplifier-output/main amplifier-input terminals and a switch that separates the two major receiver sections electrically are located on the opposite side panel (see Fig. 2). A cleverly designed channel along each side of the unit keeps cables neatly tucked out of sight. This innovative arrangement makes installation extremely simple, especially for a large, heavy unit such as this one, which might be difficult to hook up if all connections had to be made at the rear panel.



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No schematic diagram was supplied with our sample test unit, but it is clear from the receiver's internal layout (shown in Fig. 3) that

MANUFACTURER'S PUBLISHED SPECIFICATIONS:

FM TUNER:
Usable Sensitivity: mono, 8.7 dBf (1.5 μV); stereo, 15 dBf. **50-dB Quieting:** mono, 12.5 dBf; stereo, 34.0 dBf. **S/N Ratio:** mono, 80 dB; stereo, 76 dB. **Harmonic Distortion** (wide): mono, 0.06% at 1 kHz and 100 Hz; 0.08% at 6 kHz; stereo, 0.1% at 100 Hz and 6 kHz, 0.08% at 1 kHz. **Selectivity:** 90 dB (narrow); 55 dB (wide). **Capture Ratio:** 0.9 dB. **Image, IF and Spurious Rejection:** 110 dB. **Frequency Response:** 30 Hz to 15 kHz, +0.2, −1.0 dB. **Stereo Separation:** 50 dB at 1 kHz; 40 dB at 100 Hz and 10 kHz.

AM TUNER:
Usable Sensitivity: 300 μV/M internal antenna. **Selectivity:** 30 dB. **S/N Ratio:** 50 dB. **Distortion:** 0.45%. **Image and IF Rejection:** 70 dB.

AMPLIFIER:
Power Output: 160 watts-per-channel into 4 or 8 ohms, 20 Hz to 20 kHz at no more than 0.03% total harmonic distortion. **IM Distortion:** 0.03%. **Damping Factor:** 60. **Frequency Response:** power amplifier section, DC to 200 kHz, +0, −3 dB; overall, auxiliary inputs, 5 Hz to 50 kHz, +0.2, −1.5 dB; phono, RIAA ±0.2 dB. **Input Sensitivity:** phono 1 & 2, 2.5 mV; high level, 150 mV; mike, 6.0 mV. **S/N Ratio:** phono, 78 dB ("A" weighted); high level, 95 dB. **Bass Control Range** (400-Hz turnover): ±10 dB at 50 Hz. **Treble Control Range** (1.5 kHz turnover): ±10 dB at 10 kHz. **Mid-Range:** ±5 dB at 1.5 kHz. **Subsonic Filter:** −3 dB at 16 Hz (6 dB-per-octave). **High-cut filter:** −3 dB at 3 kHz (6 dB-per-octave).

GENERAL SPECIFICATIONS:
Rated Power Consumption: 680 watts. **Dimensions:** 22 1/16 W × 8 H × 19 1/2 inches D. **Net Weight:** 59.3 lb. **Suggested Retail Price:** $1050.