

computer corner

6502 An in-depth look at the widely used 6502 micro-processor.

WILLIAM BARDEN, JR.

THE MOS TECHNOLOGY MCS6502 MICRO-processor is one of the most widely used microprocessors today, especially in hobby computers where it is second only to the 8080. The Commodore PET, Apple, KIM-1 and Ohio scientific microcomputers are a few that use the 6502. Let's look at some of the hardware and software characteristics of the 6502.

6502 signals

The 6502's chief selling point is that it is an easy IC to interface, more so than the 8080. Only one power supply is required, +5 volts. Rather than a cumbersome two-phase clock, the 6502 uses an internal clock that requires only an external R-C network or crystal. Like the 8080, up to 64K (65,536) bytes of external memory can be used directly. Unlike the 8080, I/O devices are *memory-mapped*, meaning that I/O devices must share the 64K address with memory. All inputs and outputs are TTL-compatible.

Figure 1 shows the pinout of the 6502.

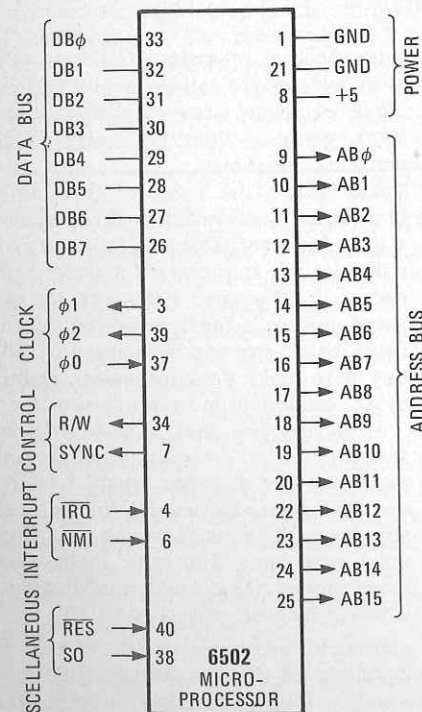


FIG. 1

There are 16 address lines, designated AB15 through AB0, and eight data lines designated DB7 through DB0; these data

lines are bidirectional. (Here, as in many other microprocessors, ABO and DB0 represent the least-significant bits.)

The clock lines are ϕ_0 , ϕ_1 and ϕ_2 . Figure 2 shows the connections for the

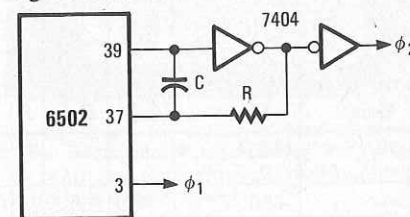


FIG. 2

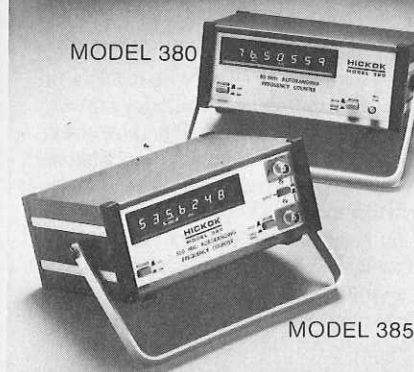
R-C network providing 1 percent accuracy for the clock frequency. Lines ϕ_1 and ϕ_2 are system clock outputs, defining a two-phase clock.

Like other microprocessors, the 6502 can execute a variety of instructions. Instruction lengths are one, two, or three bytes, and execution times range from two cycle times ($2 \mu s$) to seven cycle times ($7 \mu s$). During the course of each instruction, the one to three bytes of the instruction is *fetched* from memory by a memory read for each byte. After the CPU has fetched the instruction, the *execution* portion of the instruction is implemented. The execution portion may require additional memory reads or

TABLE 1—6502 INSTRUCTIONS

Instruction Mnemonic	Explanation	Instruction Mnemonic	Explanation
ADC	Adds 8-bit operand to accumulator with carry	LDX	Loads 8-bit operand to X index
AND	ANDs 8-bit operand to accumulator	LDY	Loads 8-bit operand to Y index
ASL	Shifts operand one bit left	LSR	Shifts operand one bit right
BCC	Branches on no carry	NOP	No operation
BCS	Branches on carry	ORA	Performs OR on 8-bit operand and accumulator
BEQ	Branch on equal	PHA	Pushes accumulator into stack
BIT	Tests operand bits	PHP	Pushes program counter into stack
BMI	Branches on minus	PLA	Pulls accumulator from stack
BNE	Branches on not equal	PLP	Pulls program counter from stack
BPL	Branches on plus	ROL	Rotates operand one bit left
BRK	Software interrupt	ROR	Rotates operand one bit right
BVC	Branches on no overflow	RTI	Return from interrupt
BVS	Branches on overflow	RTS	Return from subroutine
CLC	Clears carry	SBC	Subtracts 8-bit operand from accumulator with carry
CLD	Clears decimal mode	SEC	Sets carry
CLI	Enables interrupt	SED	Sets decimal mode
CLV	Clears overflow	SEI	Disables interrupt
CMP	Compares 8-bit operand with accumulator	STA	Stores accumulator into memory
CPX	Compares 8-bit operand with X index	STX	Stores X index into memory
CPY	Compares 8-bit operand with Y index	STY	Stores Y index into memory
DEC	Decrements 8-bit operand	TAX	Transfers A to X
DEX	Decrements X index	TAY	Transfers A to Y
DEY	Decrements Y index	TSX	Transfers S(tack) to X
EOR	Performs exclusive OR on 8-bit operand and accumulator	TXA	Transfers X to A
INC	Increments 8-bit operand	TXS	Transfers X to S
INX	Increments X index	TYA	Transfers Y to A
INY	Increments Y index		
JMP	Jump to new location		
JSR	Jump to subroutine		
LDA	Loads 8-bit operand to accumulator		

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writes, reads or writes to an I/O device, or simply perform internal processing, such as incrementing a register.

The R/W output is low for memory or I/O writes and high for reads. Transfer of data occurs during clock ϕ_2 . The direction of data transfer is determined by the state of the R/W line. As the 6502 always places known addresses on the address lines, the address, clock, and R/W signals are sufficient to control all memory and I/O reads and writes. The SYNC output identifies which cycles are fetch cycles in the instruction. The primary use of SYNC is to allow single instruction execution by using the RDY line.

The RDY line is an input used by a slow memory or I/O device to halt the microprocessor until the device can respond. Bringing down RDY during clock ϕ_1 will halt the CPU until the signal is disabled. Lines RDY and SYNC can be used in control-panel microcomputers to execute a single instruction at a time.

There are two direct interrupts available for the 6502: IRQ and NMI. NMI is a nonmaskable interrupt that can never be disabled. A negative-going edge on NMI causes the CPU to transfer control to an NMI interrupt routine in memory. Interrupt IRQ is a maskable interrupt that can be enabled or disabled by the software program. If IRQ is not disabled, an external interrupt on this line causes a

continued on page 114

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aside to hold data temporarily and to store the program-counter contents during interrupts and program subroutines. Unlike the 8080, this stack area is predefined in a page of memory located from 0100 to 01FF₁₆. As in the interrupt/reset cases, this memory area must be available and dedicated in the system.

The remaining two CPU registers are two 8-bit index registers. One of the great advantages of the 6502 is that it has a variety of addressing modes, or ways to access memory data. Indexing is a com-

mon access method on larger computers; here, the 6502 makes two registers available for indexing, making it easy for the program to acquire contiguous data.

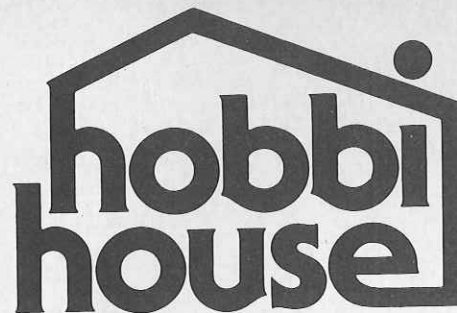
6502 instructions

There are 55 basic instructions in the 6502, but since there are 13 addressing modes there are many more unique instructions than the 55. (See Table I.)

Arithmetic instructions include an add, compare, subtract, AND, OR and exclusive OR. There are several instructions that are devoted to transferring data between CPU registers and memory, or other CPU registers. The remaining instructions are concerned with conditional branching, stack operations and subroutines. Although the 6502 does not contain any spectacular instructions (such as the Z-80 block instructions), the overall instruction repertoire, especially when you consider the 6502's powerful addressing capability, makes for a well-designed versatile microprocessor.

The 6502 is by no means overdesigned. It is an efficient microprocessor IC, easy to program at an assembly-language level and much simpler to interface than the 8080. Since there are many microcomputers built around the 6502 with much software available, you should consider it if you're buying or designing a new system.

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