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$1.00 ■ OCT. 1978

Radio-Electronics

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computer corner

6800 *An overall look at the hardware and software aspects of the 6800 microprocessor.*

WILLIAM BARDEN, Jr.

THE MOTOROLA MC6800 IS ONE OF THE "big four" microprocessors that are used in hobbyist computers. For example, it is used in the Southwest Technical Products SWTP 6800, as well as in several others. The 6800 is part of a large Motorola microcomputer family that can be used to construct a versatile microcomputer system for business, experimentation, or real-time control. Let's take a look at the hardware and software aspects of the 6800.

Hardware

The 6800 requires only an external +5-volt power supply and an external clock to implement the complete CPU function. The clock input requires a two-phase nonoverlapping type that is somewhat difficult to generate compared with the single-phase clock required by other microprocessors.

Figure 1 shows the pinout of the 6800. It contains the usual 16-line address bus A15 through A0 and an 8-line bidirectional data bus, D7 through D0. External memory and I/O (*I*nput/*O*utput) devices are addressed by the address bus, and all data is transferred between internal CPU registers, external memory and I/O devices along the data bus. As usual in this generation of microprocessors, the 16 address lines can address up to 64K (65,536) bytes of external memory and I/O devices. No differentiation is made between memory addresses and I/O device addresses in a *memory-mapped I/O* addressing scheme.

The two-phase clock inputs are at φ1 and φ2. The chief control signals for reading and writing to external memory and I/O are the VMA and R/W signals. Signal VMA is issued when a valid memory (or I/O) address is present on the address bus. Signal R/W, of course, specifies the direction of the transfer. These two signals and clock input φ2 are decoded by external logic to perform transfers between external devices and the CPU.

Bus control signals TSC (*T*hree-*S*tate *C*ontrol), DBE (*D*ata *B*us *E*nable) and BA (*B*us *A*vailable) all control the CPU bus lines for direct-memory-access (DMA) applications that transfer data between external devices and external memory, thus avoiding the CPU.

There are three interrupt inputs available with the 6800: $\overline{RESET}$, $\overline{IRQ}$, and $\overline{NMI}$. The $\overline{RESET}$ input starts the CPU from a power-down condition, or resets the CPU from a locked condition. The $\overline{IRQ}$ input is the actual external interrupt request that indicates an external device is interrupting and requires service. The $\overline{IRQ}$ input will be ignored if an interrupt-enable flip-flop in the CPU has been reset. The third interrupt, $\overline{NMI}$, can never be disabled and is used to signal catastrophic system conditions such as an imminent power loss. All three interrupts cause a *interrupt vector* address to be loaded into the program counter, effectively transferring control to one of three interrupt routines.

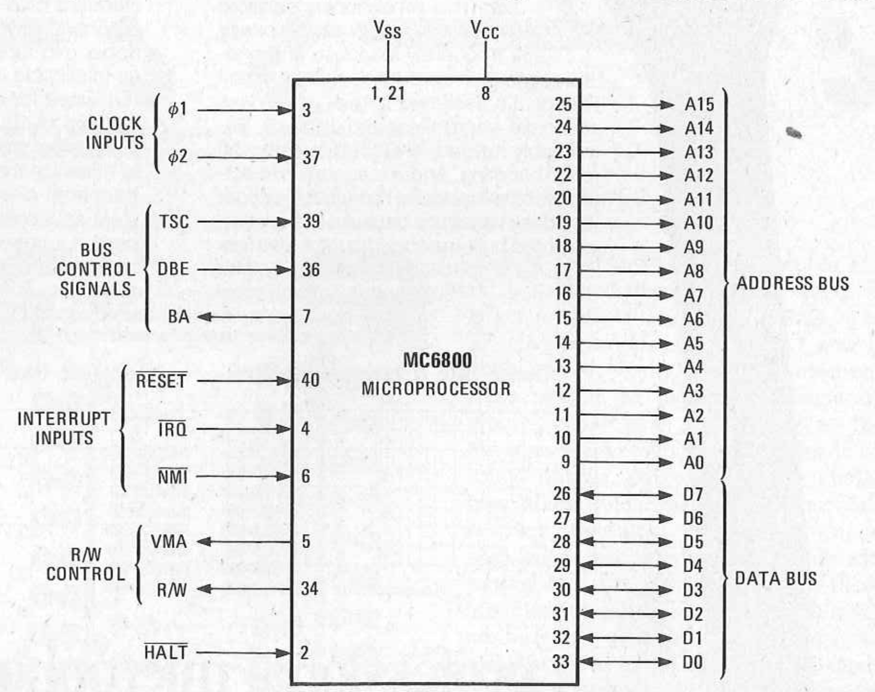

FIG. 1—PINOUT of the MC6800.

The remaining input signal, $\overline{HALT}$, is used to stop CPU activity for single-stepping and similar operations. Most of the CPU lines are three-state, reverting to a high-impedance state when disabled and allowing multiple connections to be made to the same bus or control line.

6800 architecture

Figure 2 shows the internal CPU registers of the 6800. Not shown are the nonaccessible CPU registers used in instruction fetch and execution. The program counter is a typical 16-bit register that holds the address of the instruction being executed. Addressing is performed in byte fashion, so that the program counter always holds the current external-memory address of the one- to three-byte instruction.

The stack pointer is a 16-bit register that holds the current stack address. The external memory stack is used for temporary storage of program variables and for automatic storage of CPU registers during the interrupt process. The stack can be located anywhere in external memory by properly initializing the stack pointer with the *top of stack* address.

Eight-bit accumulators A and B are used to hold one of the operands for arithmetic and logical operations in the CPU. They also serve as the registers from which data is transferred between external memory and I/O devices and the CPU. When instructions are executed in the CPU, another set of flip-flops, the condition codes, are set according to the results. Collectively, the condition codes constitute a condition-codes register that specifies carry, overflow, arithmetic sense of the last operation and interrupt-enable. As in other microprocessors, *conditional* branches in program execution can be performed by testing the states of the condition codes using proper instructions.

Index register IX is a 16-bit register that permits an *indexed addressing* mode in instruction execution in the 6800. In this mode, the *effective address* of the instruction is formed by adding a displacement in the instruction to the contents of the index register. As instructions are available to step the index register forward or backward, the indexed addressing mode can be used to sequence through tables of data or for other processing functions.

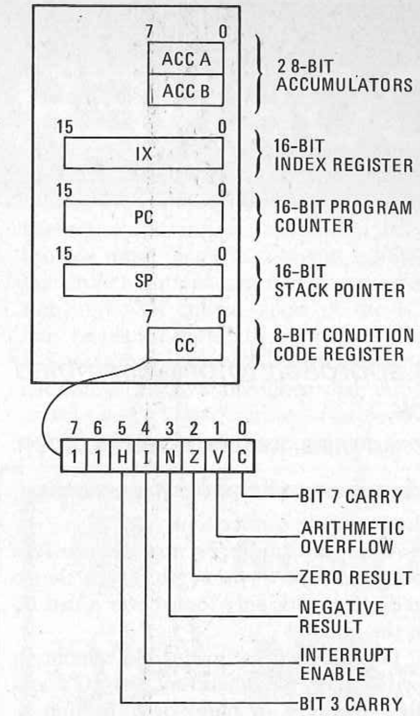

FIG. 2—INTERNAL REGISTERS of the MC6800 microprocessor.

Instruction set

The 6800 has 72 instructions. Since many of these instructions permit several addressing modes, however, the actual number of instructions is a few hundred.

The 6800 instructions are straightforward processing types: add, subtract, OR, AND, exclusive OR, shift, plus instructions to transfer data and conditionally and unconditionally branch to subroutines and other locations. (BCD arithmetic operations can also be performed.)

The instruction set's effectiveness is greatly increased by a wide range of addressing types:

1. In *immediate addressing*, an immediate 8-bit or 16-bit operand can be loaded into a CPU register from the instruction.
2. The first 256 locations in memory can be addressed by a *direct* instruction type that is only two bytes long.
3. Any location in memory can be addressed by *extended addressing* instructions that are three bytes long.
4. *Relative addressing* instruction modes address data within a range of −125 to +129 bytes of the current instruction in a compact two-byte instruction.
5. *Indexed addressing* instructions are also two bytes long.

The available addressing modes permit shorter instructions, which reduces memory and speed requirements in the system. Instruction speeds with a 1-MHz system clock range from 2 μs to 12 μs.

Other system components

The 6800 microprocessor interfaces to other IC's in the 6800 family. These include a general-purpose interface (MC6820), asynchronous communications interface (MC6850), modem (MC686OL), RAM's, and ROM's. Both the Motorola and second-source data and support are excellent, and devices are continually being developed in this family. **R-E**