computer corner

8080 *The 8253 programmable interface timer IC.*

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THIS MONTH'S COLUMN INTRODUCES THE characteristics of the Intel 8253 programmable interval timer. This versatile I/O chip can be used in a wide variety of applications (such as a real-time clock, event counting and period counting) in addition to replacing software-implemented timing loops. For example, interval timers have been used in a number of diverse applications, including a digital cardio-tachometer, a data-logging timer that uses several phototransistors to measure velocities and accelerations, and a program to sample nonperiodic waveforms for subsequent display on an oscilloscope.

The 8253 is a 24-pin IC that requires a single 5-volt supply and contains three independent 16-bit *interval timers*, each of which can be operated in six different modes. An *interval timer* has been defined[1] as a device that measures the time interval between two actions, or a timer that switches electrical circuits on or off for the duration of a preset time interval. Figure 1 shows both the pinout of the 8253 IC and how it can be interfaced with an 8080A/8085-based microcomputer system using memory-mapped I/O.[2]

TABLE 1—ADDRESSING THE 8253 programmable interval timer.

Control Inputs						
$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	COMMAND	Memory address
0	1	0	0	0	Load counter #0	200 000
0	1	0	0	1	Load counter #	200 001
0	1	0	1	0	Load counter #2	200 002
0	1	0	1	1	Load control register	200 003
0	0	1	0	0	Read counter #0	200 000
0	0	1	0	1	Read counter #1	200 001
0	0	1	1	0	Read counter #2	200 002
0	0	1	1	1	No operation (three-state)	—
1	X	X	X	X	Disable chip (three-state)	—
0	1	1	X	X	No operation (three-state)	—

Note: X = don't care (logic 0 *or* logic 1)

The 8253 IC contains four internal registers—three interval timers and a control register—that are decoded as memory locations 200 000_8 through 200 003_8 with the aid of address-bus signals A0, A1 and A15 (see Fig. 1 and Table 1). Note in Table 1 that the $\overline{RD}$ and $\overline{WR}$ control inputs determine whether you are loading or reading a specific register. It is not possible to read the contents of the control register.

Table 2 summarizes the coding for the 8-bit control register within the 8253 IC. Bits D7 and D6 determine the selection of the interval timer; bits D5 and D4 determine the nature of the read/write operation of the chosen timer; bits D3, D2 and D1 select the mode of operation of the chosen timer; and bit D0 determines whether the timer counts down in binary or binary coded decimal (BCD).

Figure 2 is the block diagram for a typical 8253 counter. The microcomputer loads the 16-bit down-counter as two successive bytes (a HI byte and a LO byte) via the bidirectional data bus, D0 through D7. If the gate line, GATE, is active, negative-edge transitions at input CLK decrement the counter. When the counter reaches zero, output pin OUT becomes active, its actual behavior depending upon the mode programmed into the control

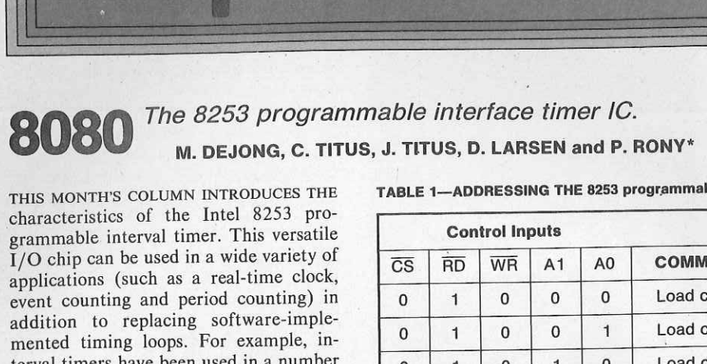

FIG. 1

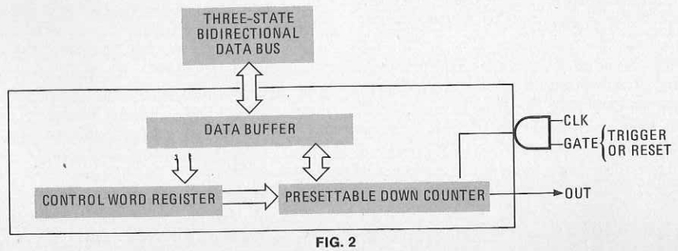

FIG. 2

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TABLE 2 (right)—CODING FOR THE 8-BIT control register in the 8253 IC.

Bits			Control Function
	D7	D6	
	0	0	Control word is for counter #0
	0	1	Control word is for counter #1
	1	0	Control word is for counter #2
	1	1	—
	D5	D4	
	0	0	Latch both bytes of chosen counter for read operation
	0	1	Load or read only most significant byte of chosen counter
	1	0	Load or read only least significant byte of chosen counter
	1	1	Load or read LS byte first, then MS byte of chosen counter
D3	D2	D1	
0	0	0	Mode 0: Output = 1 on zero counter
0	0	1	Mode 1: Retriggerable variable-width one-shot
X	1	0	Mode 2: Programmable rate generator
X	1	1	Mode 3: Programmable squarewave generator
1	0	0	Mode 4: Delayed strobe (software triggered strobe)
1	0	1	Mode 5: Triggered strobe (hardware triggered strobe)
		DO	
		0	Count down in binary
		1	Count down in binary coded decimal (BCD)

Note: X = don't care (logic 0 *or* logic 1)

register for the counter (see Table 2). The 8253 IC contains three 16-bit counters, each of which can be programmed independently in any one of the six operation modes. Counter inputs and outputs, CLK, GATE and OUT, for the chosen counter are independent of the CLK, GATE and OUT of the remaining two counters on the IC.

In addition to the address bus, data bus and control-bus connections shown in Fig. 1, inputs CLK0 and GATE0 to counter 0 are connected respectively to the $\phi 2$ (TTL) microcomputer clock output (typically 2 MHz) and to bit 0 of accumulator output port 000_8. Any TTL-level clock with a frequency of less than 2 MHz can be used as input to CLK0, and any suitably debounced switch or source of strobe pulses can be used to control the timer at GATE0. Counter output, OUT0, can be connected to an oscilloscope to observe each of the six timer operation modes.

In a future column, we will discuss a demonstration program for the 8253 interval timer that shows the loading, latching and reading of counter 0 as well as the various output modes. Other reference material[3,4] contains additional descriptions of the 8253 IC.

REFERENCES

1. Graf, R. F., *Modern Dictionary of Electronics*, Howard W. Sams & Co., Indianapolis, IN (1972).
2. Larsen, D. G., Rony, P. R., and Titus, J. A., *The Bugbook^R VI. 8080A Microcomputer Programming and Interfacing*, E&L Instruments, Inc., Derby, CT 06418 (1977).
3. *Intel Data Catalog, 1977*, Intel Corp., 3065 Bowers Ave., Santa Clara, CA 95051 (1977). Available for $2.50.
4. Osborne, A., *An Introduction to Microcomputers. Volume II. Some Real Products*, Osborne and Associates, Box 2036, Berkeley, CA 94702 (1976).

No matter what the project he's working on is supposed to be—it ends up being a light dimmer.