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8085 *A look at the 8085 and how it compares to the 8080.*

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PAST COLUMNS HAVE LOOKED AT SOME applications of the 8085 central processing unit and some of IC's that are among the 8085 family. Now let's take a closer look at the 8085 and how it compares with the 8080.

One of the 8085's main features is that it is software-compatible with the 8080 machine codes. Thus, a 303 code is a jump (JMP) instruction in both systems. (The 8085 has two additional instructions to be discussed later.) Basic 8080 systems generally include a clock generator and a status latch circuit for external control. These functions are now provided for within the 8085. A simple R–C network or a crystal can be used directly with the 8085 to generate the necessary clock pulses. Many of the control signals required by external devices are now generated in the 8085 IC, further reducing the amount of external logic required.

There is a price to pay for this, though. The 8085 uses one set of eight lines to transmit both data and address information. In some systems, it may be necessary to latch the address bits (A7–A0) so that they are readily available for use. An Address Latch Enable signal (ALE) is output by the 8085 to control such a latch circuit. This type of bus multiplexing was also done in the 8008, the first general-purpose 8-bit microprocessor IC.

The 8085 provides the high-address bits (A15–A8) on eight output pins. These signals have no other purpose and they are not multiplexed. They are equivalent to the A15–A8 lines in an 8080-based computer. Some other 8085 input and output signals such as interrupt (INTR), interrupt acknowledge (INTA), RESET, HOLD, hold-acknowledge (HLDA), and READY operate as they do in 8080 systems. Two new 8085 outputs include CLOCK OUT, a TTL-compatible clock signal of one-half the system clock frequency, and RESET OUT, which can be used to reset other system components. The RESET OUT signal is derived from the reset input to the 8085.

Three control signals manage the flow of data to and from memories and the CPU, as well as to and from I/O devices and the CPU. These signals are; IO/$\overline{M}$, $\overline{RD}$ and $\overline{WR}$. The IO/$\overline{M}$ signal is used to indicate what type of device the 8085 is attempting to communicate with: logic 1 = I/O devices and logic 0 = memories. The $\overline{RD}$ and $\overline{WR}$ signals coordinate the reading or writing of data, respectively. These three signals are used directly by the 8085-compatible memory and by I/O devices such as the 8155 and 8355. In other systems, you may have to use these signals to generate the $\overline{MR}$, $\overline{MW}$, $\overline{IN}$ and $\overline{OUT}$ signals that were discussed previously. Figure 1 shows the gating.

In almost all 8080-based systems, interrupts are implemented with an interrupt instruction port and restart instructions. The 8085 has four new interrupts that have been implemented. (See Table 1.) The overall priority of these interrupts from the highest to the lowest is as follows: TRAP, RST 7.5, RST 6.5, RST 5.5 and INT. The INT input is the usual 8080-like interrupt input. These interrupts have their vector addresses placed within the address space 000 000 to 000 100. Some of these addresses are placed between the usual 8080 vector addresses, leaving only four bytes of storage space between interrupt vector addresses. These new interrupts act in the same manner as the normal 8080-like interrupts, which means you still need a stack.

The 8085 also has a single input pin and a single output pin on the IC itself that can be controlled directly by software. Of course, the 256 addressable I/O port capability is still maintained. The two single I/O connections can be used for a single sense input and a single control output. Additionally, they could be used for serial I/O to a terminal or a teletypewriter, with the actual serialization being done by software.

Two new, single-byte instructions allow you to manage the new interrupts and the two I/O lines, SID and SOD, (*S*erial *I*nput *D*ata and *S*erial *O*utput *D*ata). These instructions are: Set Interrupt Mask (SIM = 060) and Read Interrupt Mask (RIM = 040). The A-register is used as the source or the destination of the data bytes for each operation. **R-E**

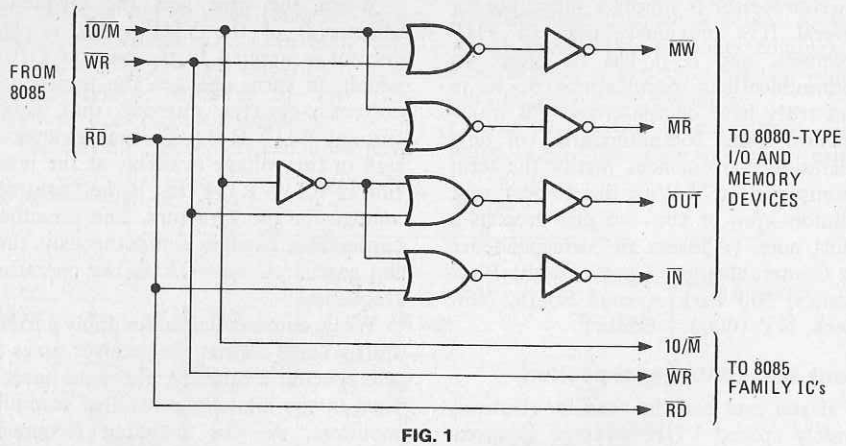

FIG. 1

TABLE 1—INTERNAL 8085 INTERRUPTS

Name	Restart Address	Characteristics
TRAP	000 044	Highest priority of all interrupts; nonmaskable, always "on"; both edge- and level-sensitive.
RST 5.5	000 054	Maskable, logic-1 sensitive
RST 6.5	000 064	Maskable, logic-1 sensitive
RST 7.5	000 074	Maskable, positive-edge sensitive

*This article is reprinted courtesy American Laboratories. Dr. Rony, Department of Chemical Engineering, and Mr. Larsen, Department of Chemistry, are with the Virginia Polytechnic Institute & State University. Both Dr. C. Titus and Mr. J. Titus are with Tychon, Inc.