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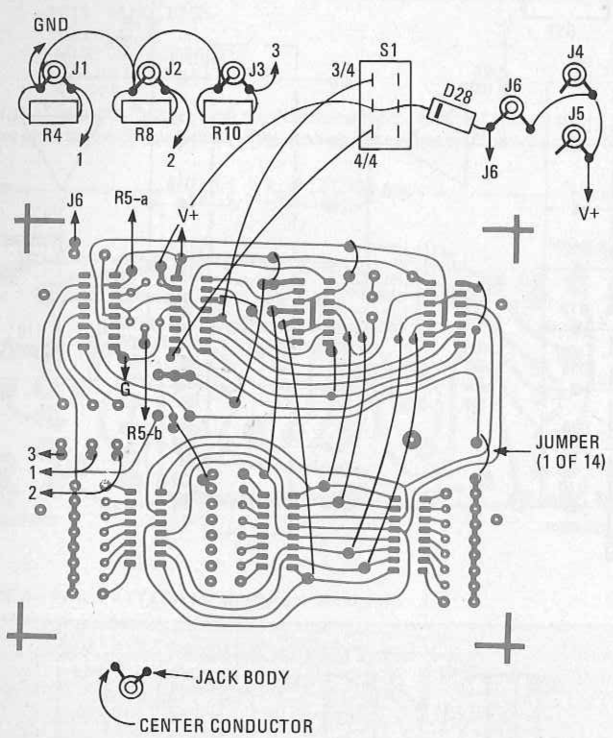
SEQUENCER PARTS LIST

Resistors ¼ watt, 10% or better
R1, R3, R6, R7, R9—100,000 ohms
R2—1000 ohms
R4, R8, R10—10,000 ohms
R5—2.2 megohms, ½-watt potentiometer
C1—0.1 μF, disc ceramic
D1-D27—1N4148 or 1N914
LED1—general-purpose LED diode, ⅛ inch
IC1—4090 CMOS hex inverter
IC2—4027 CMOS decade counter
IC3, IC4—CMOS quad 2-input NAND gate
J1-J5—phono jack, ⅛ inch
J6—phono jack, ¼ inch
S1—SPDT or DPDT slide switch
DS1—DS3—8-circuit DIP switch
Miscellaneous: PC board, enclosure, knob, wire, solder, etc.
Note: The following is available from BNB Kits, RD2, Box 242H, Tennent Road, Englishtown, NJ 07726. PC board (PSQ-PC) $25.00. Price includes shipping. No COD's. Please allow up to 6 weeks for delivery.



NOTE: ALL WIRE CONNECTIONS ON FOIL SIDE OF BOARD TACK-SOLDERED TO PADS INDICATED

FIG. 8—JUMPERS AND CONNECTIONS that are made to the foil side of the Sequencer board. Leads are tack-soldered to the pads indicated.

sound of the snare drum wires (snare), the drumstick strike as well as the drum itself.

To use the Snare accessory for steam engine or biplane effects, trigger the unit with the Pulse Generator or Sequencer, adjusting frequency (or tempo) as required.

The sequencer accessory

Circuit operation: Referring to the schematic diagram in Fig. 5, we see that IC1-a and IC1-b, R5, R7 and C1 form a variable-frequency oscillator. The oscillator clocks IC2, a decade counter with decoded outputs. The eight NAND gates in IC3 and IC4 allow the clock signal, inverted in IC1C, to pass when the corresponding output from IC2 is high. The NAND gate outputs are combined in the discrete negative-logic OR gates (D1–D8 and R3, D9–D16 and R6, D17–D24 and R9). Each OR gate input is provided through a switch. If the switch is closed, the pulse is transmitted to the OR gate. If the switch is open, no signal is provided. By opening or closing appropriate switches,

continued on page 96

TABLE 1

PROGRAM1—BASIC ROCK:
1=Bass, 2=Snare, 3=Tom-Tom
NOTE: 0=Switch Off
1=Switch On

Switch	Sequencer Channel 1	2	3
1	1	0	0
2	1	0	0
3	0	1	0
4	0	0	1
5	1	0	0
6	1	0	0
7	0	1	0
8	0	0	1

PROGRAM 2—BASIC ROCK (Modified)
1=Bass, 2=Snare, 3=Tom-Tom
NOTE: Play at twice the Tempo of Basic Rock

Switch	Sequencer Channel 1	2	3
1	1	0	0
2	0	0	0
3	1	0	0
4	0	0	0
5	0	1	0
6	0	0	0
7	0	0	0
8	0	0	1

PROGRAM 3—BONGO ROCK:
1=Bass, 2=Bongo (High Pitched),
3=Bongo (Medium Pitched)

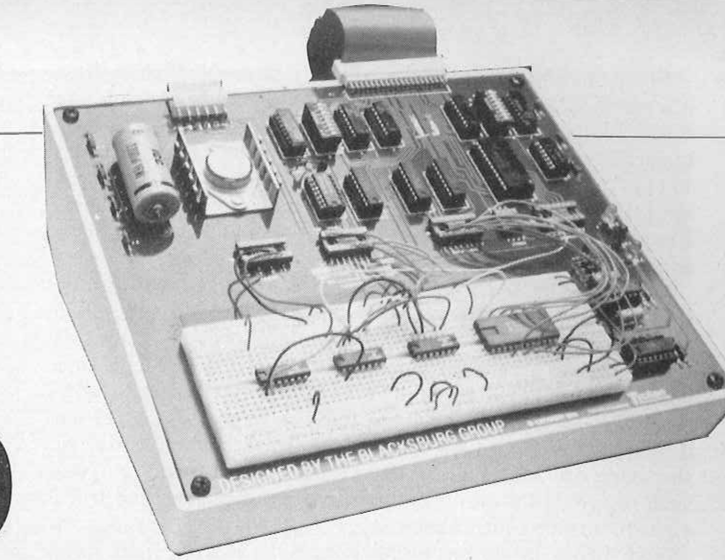
Switch	Sequencer Channel 1	2	3
1	1	1	0
2	0	1	0
3	0	1	0
4	0	1	0
5	1	0	1
6	0	1	0
7	0	1	0
8	0	1	0

PROGRAM 4—DISCO BEAT:
1=Bass, 2=Cymbal or Snare

Switch	Sequencer Channel 1	2	3
1	1	0	NOT USED
2	0	1	
3	0	1	
4	0	1	
5	1	0	
6	0	1	
7	0	1	
8	0	1	

Legend: "1=Bass" means connect Sequencer output to a Generator tuned for a Bass Drum effect.

BUILD THIS



TRS-80 BREADBOARD

Part 2—Build this breadboarding device that serves as an interface between the TRS-80 microcomputer and any circuits that you are designing or prototyping. Its design makes it easy to use.

JON TITUS, CHRIS TITUS, and DAVID LARSEN

LAST MONTH WE DISCUSSED THE NEED FOR AN INTERFACE DEVICE for the TRS-80 and began a discussion of its operation. Now, we'll complete that discussion and present the construction details.

Let's look at an example of how the decoder works. Suppose that the address switches at positions 7–4 were preset to 1011. This would set up the device address decoder so that it would be able to decode addresses of 10110000 through 10111111, although only addresses 1011000 through 10110111 would be available at the decoder's outputs. These address outputs correspond to the decimal addresses 176 through 183. The lowest switch setting at S2 must be in the open or in the D position for the decoder to operate in the device mode.

The decoder's address outputs are available at socket SO5. They are labeled "0," "1," and so on, through "7." The entire section is labeled, ADDRESS. Note that there is a bar over all of the numbers. This is to remind you that the logic zero is the asserted state for decoded addresses. The numbers are sequential, and they should help you in determining which output should be connected to your interface.

In most cases, the actual numbers, 0–7, do not correspond to the actual address values selected at the decoder. In the example just described, the "0" output would be a logic zero when address 176 (decimal) was output by the *TRS-80* on address lines A7–A0. Thus, the "0" output would correspond to an input to the decoder of 0000, while the "7" output would correspond to an input of 0111. Of course, the decoder must be enabled by the comparator before the actual decoding can take place. The decoder outputs are shown in Table 3.

Connections for address bus signals A3–A0 (unbuffered) have been provided at pins 8–5, respectively of socket SO4. These signals may be required when you are interfacing some of the advanced programmable IC's, but caution is advised since these signals are not buffered on the breadboard.

Memory addresses may also be decoded on the breadboard, if you wish to use the memory-mapped I/O technique, or if you wish to experiment with other I/O techniques. Two additional digital comparator chips, IC3 and IC4 are provided so that address bits A15–A8 may be compared with an eight-bit preset HI address. When the address bus is split into bits A15–A8 and A7–A0, the portions are often called the HI address bus, and the LO address bus, respectively.

To decode the entire 16-bit address bus, the mode switch S2 must be placed in the ON or the M position. In the memory mode, the decoder is enabled only when there is a match between the eight preset HI address bits, and the eight HI address bus signals, and when a similar match takes place between the four preset LO address bits, A7–A4, and their respective signals on the address bus. In this way, the decoder can now decode addresses that are within the range of zero to 65,536, but you should be careful not to select addresses that are presently used in your *TRS-80* system. Just as problems developed when I/O devices had the same address, similar problems can occur when devices and memory locations have the same address.

If you choose to use the memory-mapped I/O scheme, you will have to use the $\overline{RD}$ signal in place of the $\overline{IN}$ signal, and the $\overline{WR}$ signal in place of the $\overline{OUT}$ signal. In this case, the PEEK and POKE commands are used in place of the INP and OUT commands. We see little advantage in using the memory-mapped I/O technique instead of the device I/O technique, and we will not discuss it further. The memory address decoder section of the breadboard still needs some further explanation, though.

TABLE 3—ADDRESS DECODER
Connections for address Information

PIN (SO5)	LABEL	SN74154 OUTPUT PIN
1, 16	0	1
2, 15	1	2
3, 14	2	3
4, 13	3	4
5, 12	4	5
6, 11	5	6
7, 10	6	7
8, 9	7	8

Since the SN74154 decoder will only be enabled when there is a match between the preset 12 address bits, A15–A4, and the actual address bits on the address bus, the decoder can be used to decode any of the addresses between 00000000 00000000 and 11111111 11111111. These decoded addresses are indicated by a logic zero at the respective output from the decoder. Remember that only the first eight addresses in each block of 16 addresses is available at these outputs.

Let's see how a 16-bit address is decoded. We will assume that the HI address switches have been preset to 10000001, while the four LO address switches have been preset to 1110. In this way, addresses 33,248 through 33,256 would generate logic zero pulses at outputs "0" through "7," at the ADDRESS socket, SO5. If you decide to switch back and forth between the two address decoding modes, be sure that you change the switch setting of the mode control switch so that it matches the mode that you wish to use: M for 16-bit memory address decoding, and D for eight-bit device address decoding.

Two non-inverting bus buffer IC's, IC10 and IC11, are used to buffer the bus as shown in Fig. 9. This means that the *TRS-80*'s eight-bit data bus is available with a fan-out of about 30. Thus, it can directly drive up to 30 standard SN7400-series logic inputs. The bus buffers isolate the breadboarded interface circuits from the *TRS-80*'s main data bus. The eight data bus signals are available at the socket SO3. The information provided in Table 4 shows the various data bus connections.

The bus buffers are always enabled, and the normal mode of operation is for the transfer of information from the *TRS-80* to the interface breadboard. This means that you could monitor the activity of the data bus with a logic probe, logic analyzer, or oscilloscope. Output ports are implemented simply by connecting them to the data bus, and controlling them with the proper control signals. Input ports, however, must be implemented so that they can turn the bus buffers in the opposite direction to drive information into the *TRS-80*. Actually, there are two buffers for each line in the 8216 buffer IC. The EN input at pin 15 is used to select which buffer is to be used, the output buffer or the input buffer, thus directing the flow on the data bus either to, or from, the *TRS-80*. All input operations must activate the proper set of buffers, so that the information is properly transferred to the *TRS-80*. Special control circuitry has been included so that this is easily implemented.

The control circuitry on the breadboard is rather simple, consisting mainly of buffers to buffer the six useful control signals that are output by the *TRS-80*—$\overline{\text{IN}}$, $\overline{\text{RD}}$, $\overline{\text{OUT}}$, $\overline{\text{WR}}$, $\overline{\text{RESET}}$ and $\overline{\text{INTAK}}$. This is shown in Fig. 10. The interrupt input, $\overline{\text{INT}}$, has also been buffered, to protect the computer. Connections to these signals may be made at socket SO2 as noted in Table 5.

You are probably not familiar with the $\overline{\text{INTAK}}$, $\overline{\text{INT}}$, or $\overline{\text{RESET}}$ signals. The $\overline{\text{RESET}}$ signal is a short logic zero pulse that may be used to clear circuits, to get them ready for normal operation. The pulse is generated when the *TRS-80* is turned on, and when the RESET pushbutton is depressed. The RESET pushbutton is next to the interface connector on the rear of the *TRS-80*'s keyboard enclosure. The interrupt signals, $\overline{\text{INT}}$ and $\overline{\text{INTAK}}$ will not be described further, being beyond our present scope.

The control circuitry can also generate a signal that will switch the 8216 bus buffers into the input mode, so that information may be transmitted to the *TRS-80* when an INP command is executed. To handle the input ports properly, the input port's device select signal is used to gate information onto the data bus, and also to control the mode of the 8216 bus buffers. In effect, up to four input port device select pulses may be OR'ed together to place the breadboard's bus buffers in their input mode. This means that the bus buffers are placed in the input mode only when a breadboarded input port has been selected. The INP REQ, (input request) signals are required to be logic zero pulses, and they may be applied to pins 16, 15, 14 or 13 on the socket at IC17. These positions have been labeled "W," "X," "Y," and "Z."

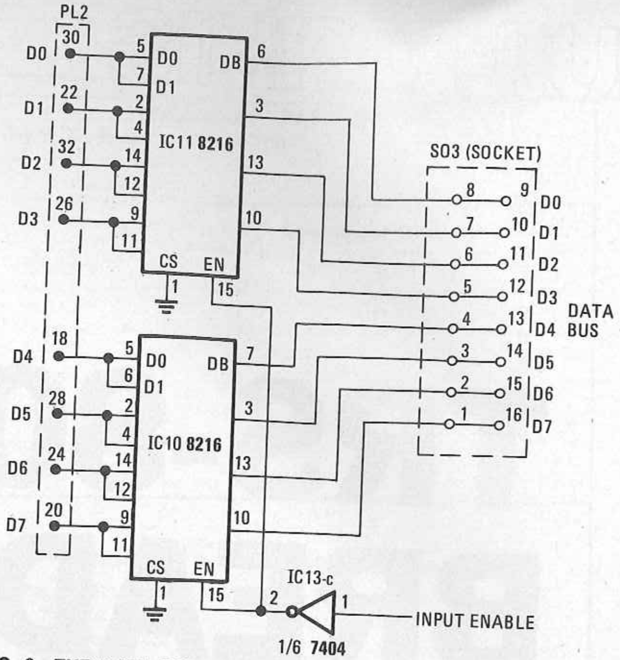


FIG. 9—THE DATA BUS BUFFERS. The EN input controls the flow of information through the 8216 buffers.

TABLE 4—DATA BUS CONNECTIONS	
PIN (IC13)	DATA BUS SIGNAL
1, 16	D7
2, 15	D6
3, 14	D5
4, 13	D4
5, 12	D3
6, 11	D2
7, 10	D1
8, 9	D0

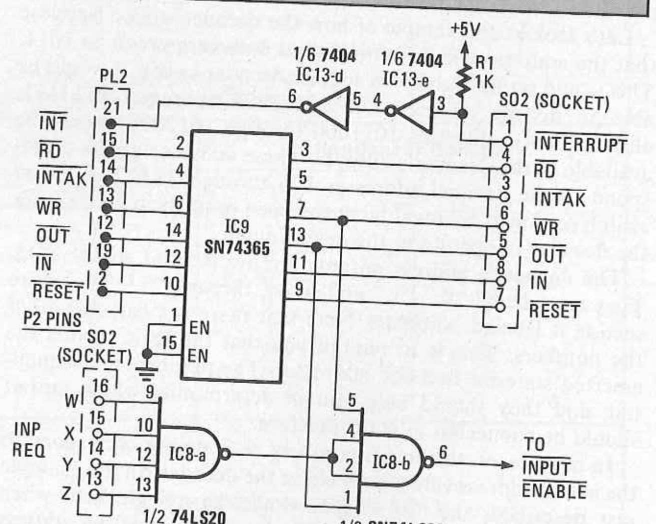


FIG. 10—SCHEMATIC DIAGRAM of the circuit used for control-circuit buffering and for control of the 8216 bus buffers.

TABLE 5—CONTROL SIGNAL CONNECTIONS		
PIN (SO2)	CONTROL SIGNAL	DIRECTION
1	$\overline{\text{INT}}$	To TRS-80
2	Not Used	—
3	$\overline{\text{INTAK}}$	From TRS-80
4	$\overline{\text{RD}}$	From TRS-80
5	$\overline{\text{OUT}}$	From TRS-80
6	$\overline{\text{WR}}$	From TRS-80
7	$\overline{\text{RESET}}$	From TRS-80
8	$\overline{\text{IN}}$	From TRS-80

PARTS LIST

Resistors ¼ watt, 5%
R1, R8—1000 ohms
R2, R3—220 ohms
R4, R5—47,000 ohms
R6—3900 ohms
R7—2200 ohms
C1—2200 μF, 16 volts, electrolytic, axial leads
C2, C4, C5—0.1 μF, 50 volts, disc ceramic
C3, C6—1 μF, 35 volts, tantalum electrolytic
C7, C8—3.3 μF, 50 volts, electrolytic, axial leads

Semiconductors
IC1, IC7—16-pin resistor network (eight 1K resistors)
IC2, IC6—Not used
IC3—IC5—SN74LS85 quad comparator (do not substitute SN74L85)
IC8—SN74LS20 dual 4-input NAND gate
IC9—SN74365 or DM8095 three-state buffer
IC10, IC11—8216 non-inverting bus buffer (Intel or equal)
IC12—SN74154 4-line to 16-line decoder
IC13—SN7404 hex inverter
IC14—SN74123 or SN74LS123—dual retriggerable one-shot
IC15—LM319N dual comparator (14-pin package)
IC16—LM309K, voltage regulator, 5 volts, 1 amp.
D1-D4—1N4001 or equal, 50 PIV, 1-amp, diode
D5, D6—1N4148 or 1N4154 small-signal diode
LED1—yellow LED
LED2—red LED
LED3—green LED
S01, S02, S03, S05—High-quality 16-pin DIP socket (Augat 516-AG-10D or equal)
S04—high-quality 8-pin DIP socket (Augat 508-AG-10D or equal)
PL1—Molex right-angle 6-pin connector (PN 09-75-1061) optional. Requires 1 mating female housing (PN 09-50-7061) and 6 connector pins (PN 08-50-0106 or 08-50-0108)
PL2—40-pin right-angle jumper header, AP Products 923875R or equal
T1—transformer, 12.6 volts, 1 amp

Miscellaneous
Solderless breadboard socket. E&L Instruments model SK-10, AP Products model Superstrip II, Continental Specialties model EXP-300 or equal.
Cable assembly, 40-pin header on one end and 40-pin card-edge connector on the other—facing the same direction.

The following parts are available from E & L Instruments, Inc., 61 First St., Derby, CT 06418.
Order No. 355-6125—Complete kit including PC board, case and all parts. Does not include interconnect cable. Specify 117V or 230V version. $139.00.
Order No. 355-6175—Interconnect cable assembly (connects breadboard to TRS-80 computer). $25.00.
Order No. 355-6100—Assembled 117-volt version. $185.00.
Order No. 355-6150—Assembled 230-volt version. $185.00.
Connecticut residents add state and local taxes as applicable.
A pre-drilled and etched PC board is available from Techniques, Inc., 235 Jackson St., Englewood, NJ 07631, for $24.50 postpaid. New Jersey residents add 5% sales tax.
Copies of the book *TRS-80 Interfacing* (published by Howard W. Sams and Co.) is available for $7.95 plus 79¢ for shipping and handling from Group Technology, Ltd., PO Box 87, Check, VA 24072

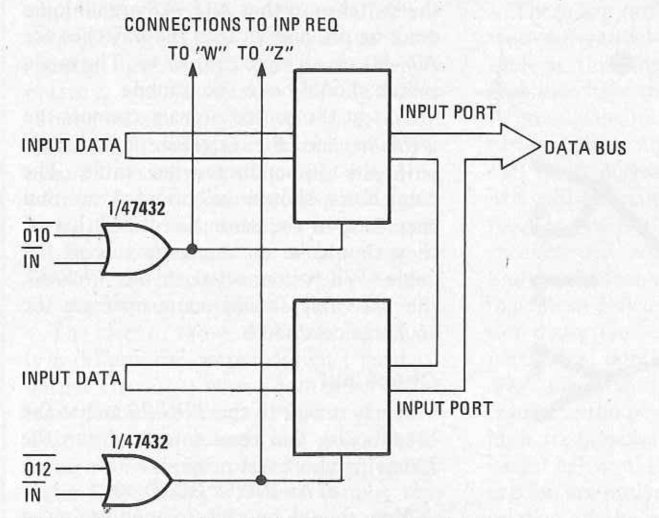


FIG. 11—BLOCK DIAGRAM of two input ports, showing the generation of the required input request (INP REQ) signal for bus control.

Figure 11 shows how these INP REQ signals are generated. Actually, they are the same signal that has been used for the selection and control of the input port, itself. Thus, whenever an input port is constructed, the logic zero device select pulse ($\overline{\text{IN}}$ and the device address) is used to control the input mode of the bus buffers. The actual OR'ing of the various INP REQ signals is performed by IC8. The input request signal that is generated by IC8 is further gated with both $\overline{\text{OUT}}$ and $\overline{\text{WR}}$. This additional gating provides a safety interlock, so that the bus can not be mistakenly placed in the input mode while the *TRS-80* is performing an output, or a memory write operation. The resulting control signal, INPUT REQUEST, BUT NOT $\overline{\text{OUT}}$ OR $\overline{\text{WR}}$, is what turns the bus drivers around, placing them in the input mode.

Construction

The interface breadboard circuits may be constructed using the wire-wrap technique, but this may mean that the breadboard is somewhat difficult to use. A printed circuit board has been developed, and we recommend its use for this project. The foil patterns are shown in Figs. 12 and 13, with a parts placement overlay shown in Fig. 14.

In addition to the parts listed for the construction of the *TRS-80* interface breadboard, you will need the following to perform various tests on the interface. These are general-purpose parts, and they are readily obtained from many sources. You will find that they are used in many interfaces, since they are not specific to the tests outlines in this article.

1. One solderless breadboard (may be available on your breadboard)
2. Two SN7402 quad NOR gates
3. Three SN74LS373 octal buffer-latches
4. Two DM8095 or SN74365 three-state buffers
5. Eight LED's (red)
6. Jumper wires (No. 24) stripped at both ends

If you are going to use a printed circuit board inspect the board carefully before you start. Pay careful attention to the etched areas, and to the remaining conductor paths, looking for bridging of conductor paths, and for over-etched sections that may cause a conductor to be open. Once you are satisfied that your circuit board is properly etched, you are ready to start the construction of the interface breadboard.

Start your construction with the power supply section. Install and solder power diodes D1–D4, filter capacitor C1 and regulator IC16 if you plan to use the on-board regulator circuit. As mentioned previously, we recommend a small heat sink for the voltage regulator. If you will be using an external +5-volt power supply, these parts are not required, and they should not be installed on the board. Connector PL1 is used to make connections with the power supply, or the external transformer. Pins 1 and 2 are used to connect the on-board power circuit with a 12.6 VAC transformer, while pins 5 and 6 are used for connections to +5 volts and ground, respectively, when an external power supply is used. Two spare pins, 3 and 4, have been provided, so that other voltages may be connected to the POWER socket on the breadboard. These connections may also be made by soldering directly to the PC board.

Once the proper power supply connections have been made, connect power to your system, and check for +5 volts at pins 7 and 10 at socket SO1. You should also be able to detect ground (zero volts) at pins 5 and 12 on the same socket.

With the power supply section of the breadboard operating

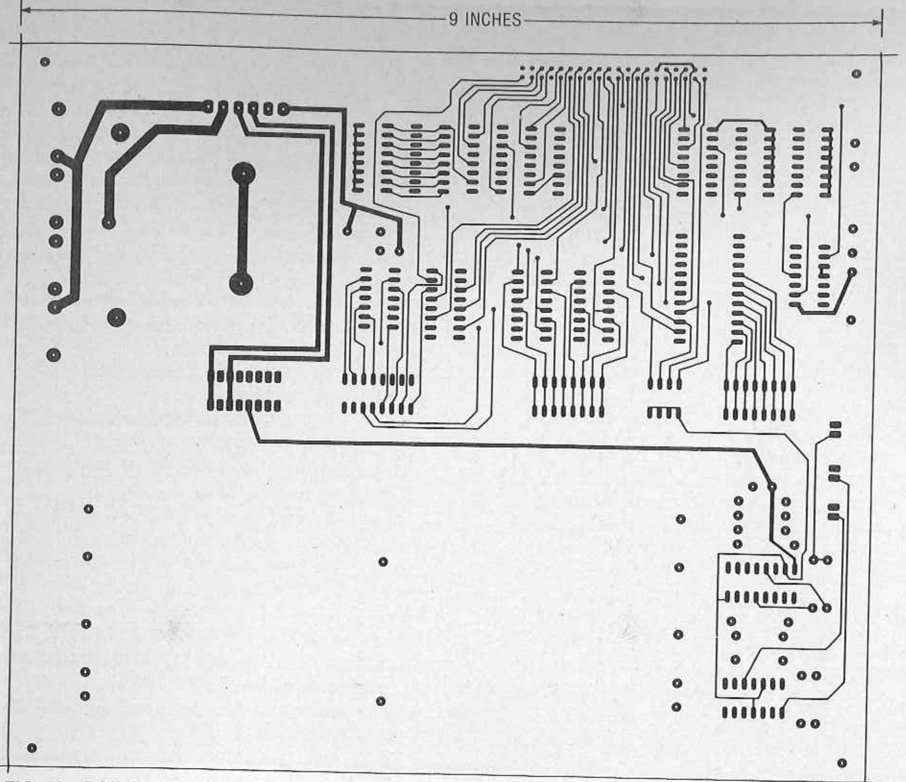


FIG. 12—FOIL PATTERN for the component side of the PC board.

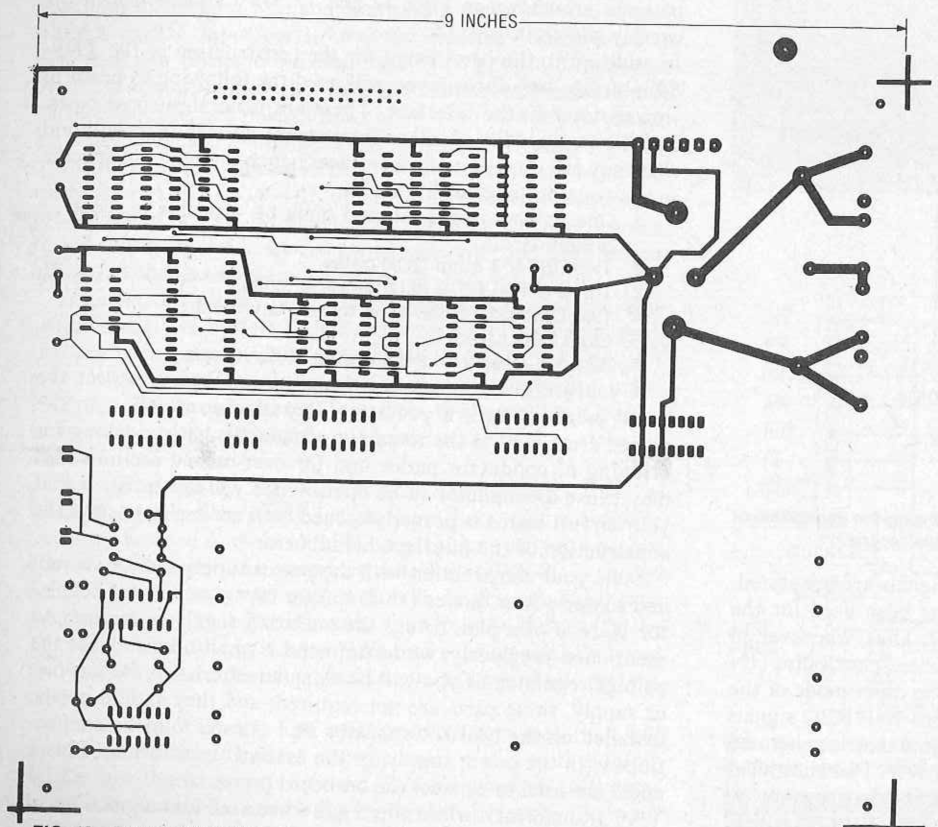


FIG. 13—FOIL PATTERN for the under side of the printed-circuit board.

properly, the logic probe should be constructed next. You may skip this section if you have chosen to use an external probe. Add those parts to the breadboard that are located to the lower right of SO5. These parts include LED1–LED3, D5, R2–R8, C6–C8 and IC14 and IC15.

Once this section has been constructed, apply power to your system. None of the logic probe LED's should be lit. If either the "1" or the "0" LED is lit, check the comparator circuit. If the P LED flashes as power is applied, this is acceptable. If it remains lit, test the SN74LS123, or the SN74123, that you have used.

Remove the power and install sockets SO1–SO5. These are the high-quality sockets that are used to make contact with the interfacing signals. Once these have been installed, turn the power on once again and place a jumper wire (8 to 10 inches long) in one of the P inputs of SO4. Connect the other end to the +5-volt pin of SO1. The "1" LED should be lit. Now connect it to the ground pin. The "0" LED should be lit.

The remaining IC's should now be added to the PC board, along with the 40-pin male connector (PL2), and the remaining components. If you are going to substitute individual 1000-ohm ¼-watt resistors for the two dual in-line resistor packages, IC1 and IC7, you will need 13 individual resistors. These resistors should be soldered between pin 1 and pin 16, and so on, across the space left for the integrated circuits at IC1 and IC7. All eight of the resistors should be soldered in at IC1, while only five are required at IC7.

Do not install the two 8216 bus buffers at this time. They will be added to the circuit later. Pay careful attention to the orientation of the two eight-switch dual in-line packages. The switches' on position should be on the left side. Initially set the switches so that A15–A8 are all logic zero, or on, and so that the switches for A7–A0 are all logic zero, or on. The mode switch should be in the D mode.

To test the control signals, connect the *TRS-80* and the interface breadboard with the 40-conductor flat cable. The connectors should be oriented so that they face in the same direction; that is, they should be on the same side of the cable. When connected to the *TRS-80*, the flat cable should come up from the socket access hatch.

Check out

Apply power to the *TRS-80* and to the breadboard, and then enter and run the following short test program:

```
10 A=INP(5): GOTO 10
```

You should be able to monitor pulse activity at the $\overline{\text{IN}}$ signal output at the CONTROL SIGNALS socket. Once you have been able to monitor these pulses, enter and run the following program:

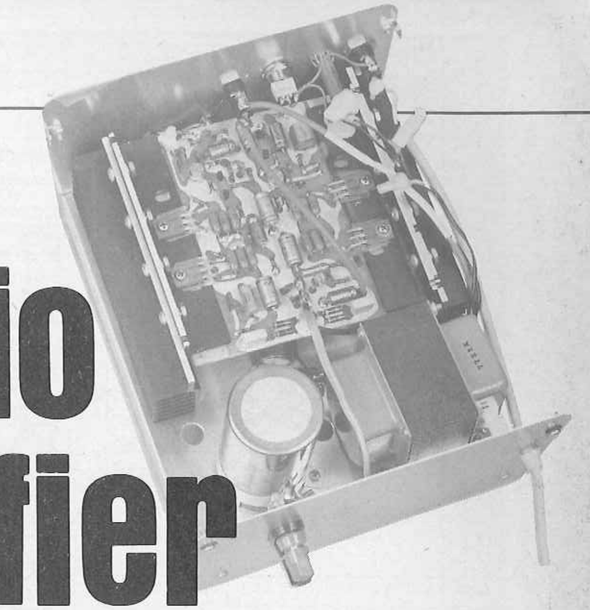
```
10 OUT 7,0: GOTO 10
```

When this program is being run, you should be able to monitor pulse activity at the $\overline{\text{OUT}}$ signal output pin. If you were not able to monitor these pulses, check both the DM8095 (or SN74365) buffer, and the SN74LS123 (or SN74123) monostable. You are testing two things here, the availability of the control signals, and the correct operation of the logic probe's pulse detecting circuit. If the probe is operating properly, you should observe that the "1" LED is lit, while the $\overline{\text{IN}}$ or the $\overline{\text{OUT}}$ pulse also causes the P LED to be lit. This indicates that the normal logic state is logic one, while the pulses are logic zero pulses.

continued on page 94

BUILD THIS

Super Audio Amplifier



Bridge-type power output configuration lets you use inexpensive "plastic" transistors and a simpler power supply to provide a wide frequency response and a signal-to-noise ratio of 100 dB.

DAN TALBOT

THIS AUDIO POWER AMPLIFIER ELIMINATES the need to AC-couple the loudspeaker, uses only one power supply polarity, and needs only half the power supply voltage of a conventional circuit approach, allowing the use of inexpensive plastic transistors in the output stages! In addition, its frequency response goes "way down" and, since no large output coupling capacitors are used, space is saved on the chassis, especially important for quadriphonic applications.

The circuit, shown in Fig. 1, is basically a differential-output design ("bridge" output circuitry) where *both* sides of the loudspeaker are driven 180° out of phase. This amplifier delivers 60 watts RMS using a 38-volt DC power supply, or 100 watts RMS using a 44-volt supply, into an 8-ohm speaker. Conventional amplifiers drive only one terminal of the loudspeaker and fix the other speaker terminal at ground. This approach requires twice the power supply voltage for the same output power as the circuit described in this article. A conventional circuit would, therefore, require output transistors having 80-volt (or higher) breakdown ratings, and large "safe area" operating regions. Additionally, a conventional circuit approach would require a coupling capacitor to the loudspeaker (usually about 4000 µF at 50 volts) or would require a two-polarity power supply (in which case the capacitor is not really "saved," but is required for filtering the additional supply).

The amplifier in this article can be built for about $35.00 per channel, less power supply. Frequency response is flat from 10 Hz to over 30 kHz, and distortion is less than 0.5%.

There are other advantages, also, to a true differential-output power amplifier such as this one. If both halves of the amplifier have the opposite phase-versus-frequency characteristics, as in this independent-twin amplifier approach, then 180° shift across the loudspeaker terminals will be maintained out to very high frequencies. This means that the loudspeaker will see symmetrical slew-rate limiting, a factor important in minimizing the so-called "transient intermodulation distortion" components. Also, in this particular configuration, the constant 180° phase shift across the loudspeaker results in the power output holding up at high frequencies, even though the individual halves of the amplifier twin-configuration are undergoing severe phase-shift relative to the audio input signal. This results in greatly reduced group-delay (time-dispersion) versus frequency compared to many other possible bridge configurations.

All of these technical advantages translate into a highly pleasing amplifier for the serious audiophile who is content with 100 watts. (The sound of an amplifier which clips before the loudspeaker clips is vastly preferable to the sound of a loudspeaker being driven "against the stops." The 100-watts level is ideal for most standard loudspeaker configurations.

Other variations of the circuit realization of a paraphase-output amplifier are possible, but this approach was settled on as the ultimate for simplicity and performance, using inexpensive components.

Notice the deliberate absence of electronic protection circuits. A fuse in the $+V_{cc}$ (B+) line of the power supply, see Fig. 2, protects the loudspeakers in the event of a transistor short. The absence of electronic protection circuitry ensures that transient "spiking" will not occur as a result of constant-current limit drive to an inductive load.

When an ordinary protection circuit is activated, the amplifier output impedance is suddenly forced to a very high value

R-E TESTS IT

Input sensitivity: 1.7V input, for 60 watts output across 8-ohm load
Frequency response: 8Hz to 62 kHz (−1 dB rolloff points)

8-OHM LOAD	
Output at clipping, 20 Hz:	52 Watts
Output at clipping, 20 kHz:	62 watts
Output for 0.5% THD, at 1 kHz:	60 watts

4-OHM LOAD	
Output for 0.5% THD, 1 kHz:	72 watts (author claimed 70 watts)

Signal-to-Noise Ratio (re: 60 W output, 8 ohms): 100 dB

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TRS-80 BREADBOARD
continued from page 54

To test the decoder section of the breadboard, you will need a NOR gate integrated circuit, such as the SN7402, and a solderless breadboard that can be used to help you set up a test circuit. Wire the circuit that is shown in Fig. 15. The $\overline{IN}$ and $\overline{OUT}$ signals are provided at SO2, while the $\overline{6}$ and $\overline{7}$ signals may be found at the ADDRESS socket SO5. Once the switches have been set to the positions noted previously (all zeros, mode D), run the following program.:

```
10 A=INP(7): GOTO 10
```

You should observe pulse activity at point A, but not at either B or C. Change the program, so that input port 6 is accessed:

```
10 A=INP(6): GOTO 10
```

You should observe activity at point B. To test the output control, use the following program.:

```
10 OUT 6,0: GOTO 10
```

When this program is run, you should observe activity at point C. You may wish to try other addresses, and also the PEEK and POKE commands, so that the HI address decoders are accessed. If you use the address decoders for memory addresses, remember to use the formula:

Address = −1*(Desired Address −32,767)

when the address that you wish to access is above 32,767. This has no effect upon the interface. It simply causes the *TRS-80* to generate the proper 16-bit address. Thus, to access a location, or a memory-mapped I/O device, with an address of 36871, the following short program could be used:

```
10 POKE −1*(36871-32767),0
20 A = PEEK (−1*(36871-32767)
30 PRINT A: GOTO 10
```

If you wish to observe this program in operation, you would have to replace the $\overline{IN}$ signal with $\overline{RD}$, and the $\overline{OUT}$ signal with $\overline{WR}$, as previously shown in Fig. 15. You would also have to switch to the memory address mode, M, and then set the address bits so that they corresponded to the binary equivalent of 36,871; that is 10010000 00000111. If you run the program shown above, you would be able to monitor pulse activity at point A as shown in Fig. 15. Point A would correspond to the pulse generated by a read operation at location 36,871, corresponding to the PEEK operation. No pulse activity would be observed at points B or C, since there is no address 36,870 being used in the program. Again, we see no advantage in using memory-mapped I/O, but we have presented this example so that you can check out the HI address decoding section of the interface breadboard. If you perform these tests, remember to place the mode switch in position, D when you have completed the test.

You are now ready to test the data bus buffers. Add bus buffers IC10 and IC11.

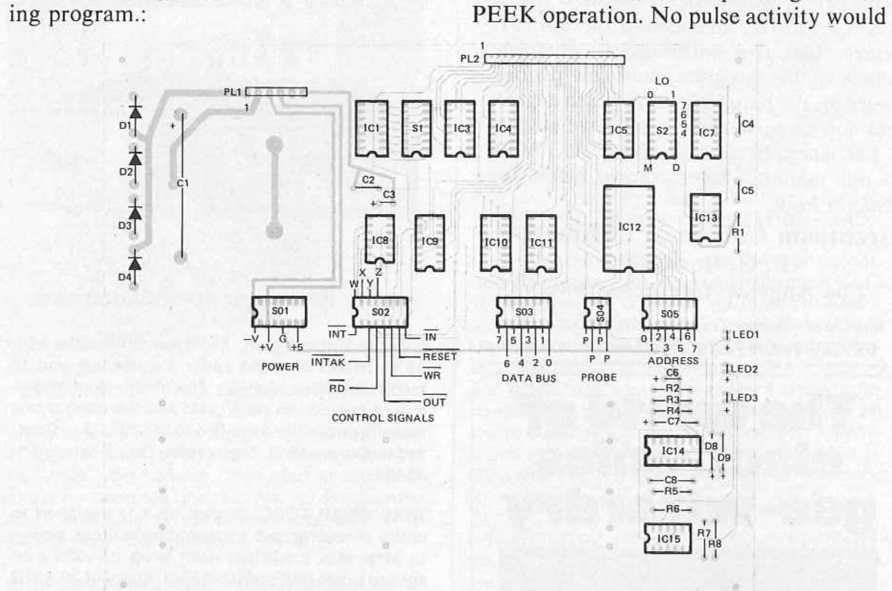

FIG. 14—HOW COMPONENTS ARE PLACED on the PC board. Several of the IC sockets are used for connections to point-to-point jumpers.

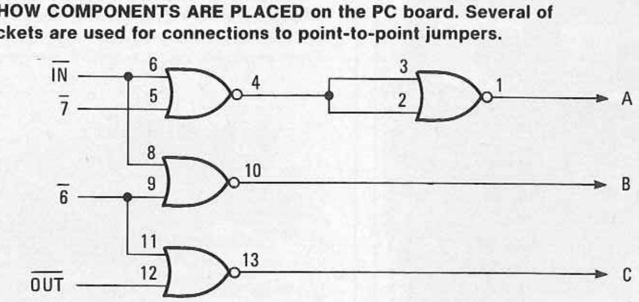

FIG. 15—SCHEMATIC DIAGRAM of the NOR gate circuit used for testing the breadboard.

The *TRS-80* should run properly with these IC's in place, and with the power applied to the breadboard. If it does not, remove the IC's and check their orientation. If this still doesn't cure the problem, you may wish to breadboard a test circuit for the 8216's. You want to be sure that the EN input to both IC's, pin 15, is in the logic zero state for normal operation. If this condition is not found, check back through the two SN74LS20 NAND gates.

Once the *TRS-80* is operational, as it probably will be in almost all cases, you will need to construct an input port, and an output port to thoroughly test the data bus connections. Refer to Figs. 4 and 5 for the details of each port. You may use the test circuit in Fig. 15 to generate the device select pulses required to control each port. If you have performed the memory address tests, be sure to rewire the test circuit so that the $\overline{IN}$ and $\overline{OUT}$ signals are used, as shown in Fig. 15. Output A from the test circuit may be used as the $\overline{DEVICE\ SELECT}$ pulse for the input port IC's (DM8095's or SN74365's), while output C may be used to control the output port (SN74LS373). The lamp monitors may be LED's, and the logic switches may be simply jumper wires that are easily switched between connections with +5 volts (logic one), and ground (logic zero). Once this has been wired, make a connection between the SN7402's A output, and one of the INP REQ pins at SO2.

Enter and run the following program, with power applied to the breadboard:

```
10 FOR A=0 TO 255
20 OUT 6,A
30 NEXT A
40 GOTO 10
```

This program will generate an incrementing count at the output port, and you should be able to observe an eight-bit binary count on the LED's that are connected to the SN74LS373. If this counting action is not observable, check output C on the SN7402, to be sure that the output port is being activated by the computer. You should also be sure that the SN74LS373 is operating properly, and that all of the connections have been properly made. When wiring an interface of this type, it is often easy to "twist" a data bus wire, so that data bit D4 appears where bit D5 should, and vice versa. Recheck your bus wiring. If a bit is not observed to be counting (constantly on, or constantly off), switch the 8216's. If the "bad bit" moves, you probably need to replace the 8216 bus buffer. Don't forget that if you can't observe any action on the LED's, the logic probe can be used.

Once the output port has been tested, enter and run the following program:

```
10 A=INP(7)
20 PRINT A
30 OUT 6,A
40 GOTO 10
```

This program transfers information from the logic switches to the *TRS-80*. The *TRS-80* prints the decimal value on the screen, and it then outputs the information to the output port. When the program is running, you should be able to change the logic switch or jumper settings and then observe the effect upon the displayed value, and the value printed on the *TRS-80*'s screen.

Before you dismantle the two ports that you have constructed, you may wish to try and use them in other ways. Space has been left on the PC board so that a solderless breadboard may be added to make your experimenting easy. We think that you will find the breadboard to be a valuable tool, since all of the generally used *TRS-80* I/O control signals have been provided for you, along with a suitable decoding scheme, and an on-board logic probe. If you are interested in some of the things that can be done with the breadboard, we suggest that you obtain a copy of the *TRS-80 Interfacing* book mentioned previously. It contains 18 experiments that you can do on the interface breadboard, including experiments on decoders, I/O ports, flags and A/D and D/A converters. But for now, let's look at two experiments you can do. Next month we'll develop the software for controlling a traffic light and then see how to use the TRS-80 to develop analog control voltages. **R-E**

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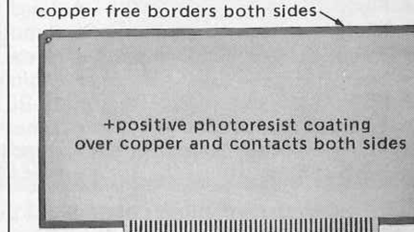

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