computer corner

8085 *A look at Intel's 8085 μP and the MCS-48 μP family.*

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INTEL CORPORATION, DESIGNERS OF THE 8008 and 8080 microprocessors, have developed two new devices. One is the Intel 8085, a microprocessor that is designed to replace the 8080A. It is a larger-scale microprocessor because it is designed to be used in applications that in some cases were only in the realm of minicomputers. The MCS-48 family of microprocessor components, on the other hand, is a minimum-configuration type of microprocessor that will be used to implement low-cost consumer and business computer products.

The 8085

The 8085 is a redesigned 8080A microprocessor. One of the weaknesses of the 8080 microprocessor was that for a basic system it required a dozen or so TTL IC's in addition to the basic CPU. The 8085 requires only a few external components to produce a viable microcomputer. Although the 8085 is not pin-compatible with the 8080, it is software-compatible *downwards;* that is, all software written for the 8080 will run on the 8085, except that which is specifically geared for an existing 8080 microcomputer system, which may differ in I/O addresses, memory cycle times, and the like in a new 8085 system.

Figure 1 shows the pinout of the 8085 microprocessor, which uses only one supply voltage, +5 volts, with the input at V_{CC}; V_{SS} is the ground reference. The −5 VDC and +12 VDC of the 8080 are eliminated. The 8085 uses an on-chip clock generator, with only an external crystal or R–C network, whereas the 8080 uses a two-phase external clock. The basic clock speed is 3 MHz, and the basic instruction cycle is 1.3 μs, which is an improvement over the 8080's 2-μs instruction cycle.

The 8085 *multiplexes* the address and data outputs during the instruction cycle. Lines A15 through A8 are the address lines, as in the 8080, but lines AD7 through AD0 are used both as the lower half of the address lines and the data bus. These lines are used as the address bus during the first clock cycle of a machine cycle and as the data bus during the second and third clock cycles. Signal ALE (*A*ddress *L*atch *E*nable) occurs during the first clock cycle to allow components to latch the address.

In the 8080, status signals needed further decoding to produce read and write signals to memory and I/O. In the 8085, these signals are provided directly by $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$; the latter indicates whether the read or write is to memory or I/O. Outputs S0 and S1 provide encoded status of the bus cycle (HALT, WRITE, READ, or FETCH). The READY instruction is used similarly as with the 8080—to interface slow-speed memory or I/O devices by deferring CPU operation. Instructions HOLD and HLDA are also similar to the 8080, allowing external devices to control the CPU buses for direct-memory-access action.

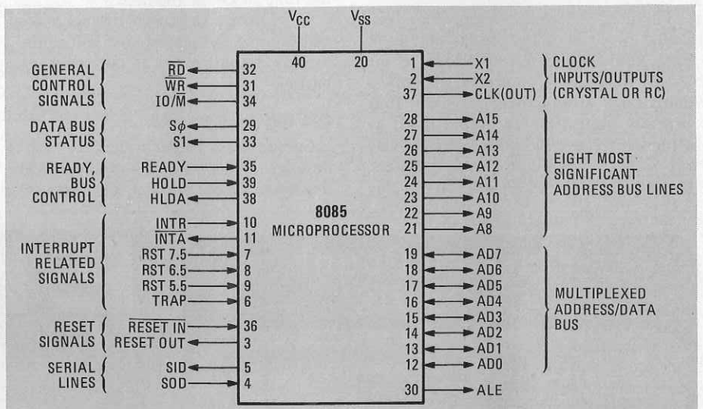

FIG. 1

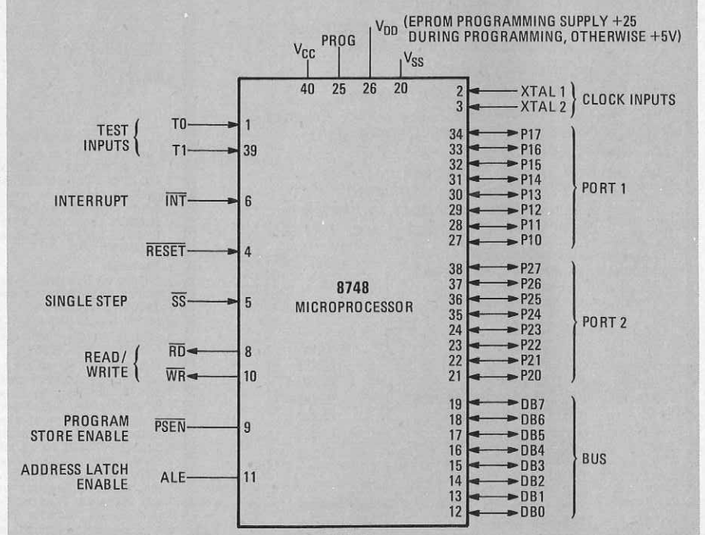

FIG. 2

Interrupt action in the 8085 is more sophisticated than in the 8080. Signals INTR (*INT*errupt *R*equest) and $\overline{INTA}$ (*INT*errupt *A*cknowledge) are used as before, but three additional interrupt inputs, RST 5.5, RST 6.5 and RST 7.5 cause predefined internal RESTARTS (rather than an *external* RESTART response). In addition, a *nonmaskable* interrupt that cannot be disabled under program control is provided by signal TRAP. A $\overline{RESET\ IN}$ input is similar to the 8080's RESET input; the output RESET OUT indicates that the CPU is currently being reset.

One serial-input line and one serial-output line are provided in the 8085; the 8080 had neither. Data on the SID (*S*erial *I*nput *D*ata) line is loaded into accumulator bit 7 whenever a RIM instruction is executed. The serial-output data line can be set or reset by an SIM instruction. These two lines allow serial I/O devices such as *Teletypes* or audio tape cassettes to be directly interfaced to the CPU. Instructions RIM and SIM are the only two new instructions in the 8085. Internal registers within the 8085 central processor unit remain the same as in the 8080.

A dedicated function microcomputer using the 8085, a 2K-byte EPROM chip (8755), a 256-byte RAM (8155) and six discrete components can be assembled on a 4-inch by 3-inch PC board. This is quite a change from the 8080! Such a single board microcomputer can easily handle many control applications and its small size makes it easier to design into household appliances.

MCS-48 family

Speaking of computers on a chip, the microprocessors in the MCS-48 family certainly fit the description. The 8048 microprocessor IC of this family is the most elaborate of them all. The 8048 provides an 8-bit CPU, 1K-byte ROM, 64-byte RAM, 27 I/O lines (which may be programmed for input and output as required) and an 8-bit timer/event counter, all on one IC! The 8748 microprocessor is identical to the 8048 except that it contains a 1K-byte EPROM (*E*rasable *P*rogrammable *R*ead-*O*nly *M*emory). Other versions of these two microprocessors contain additional ROM and data (RAM) memory, or no internal memory. A low-cost version, the 8021, contains an instruction subset of the 8048 and fewer hardware features.

Let's take a brief look at the 8748 (EPROM) version. Figure 2 shows a standard 40-pin 8748 package. In this version, only a single +5-volt power supply is required. A crystal clock input is provided, although this may be an L–C network or an external clock rather than a crystal controlled clock.

Input/output port 1 (P10–P17) and I/O port 2 (P20–P27) are two 8-bit ports than can be used either as input or output ports. Input and output on the same pin and a mixture of input and output lines on the same port is permitted. Lines DB7 through DB0 are also an 8-bit port that serves either as a latched output port or a nonlatching input port. Two additional input pins, T0 and T1, are test inputs that can be tested under program control by specific instructions. One interrupt input, $\overline{INT}$, is implemented so that an interrupt occurs if an internal interrupt-enable flip-flop is set. Various other control signals are provided.

Figure 3 shows the architecture of the 8748. One 8-bit accumulator serves as the main data register for arithmetic and other operations; both binary and decimal arithmetic are implemented in the CPU. Program memory of 1K bytes is provided on the resident EPROM. Locations 0, 3 and 7 of program memory are dedicated to reset, external interrupt and timer/counter interrupt processing routines, respectively. Data memory consists of 64 bytes of RAM, in which two sets of eight locations are designated bank 0 and bank 1 working registers. Either bank 0 or bank 1 can be selected under program control. When one or the other bank is selected, all registers in the bank are directly addressable by several instructions. An eight-level stack and additional user RAM comprise the remainder of the data memory.

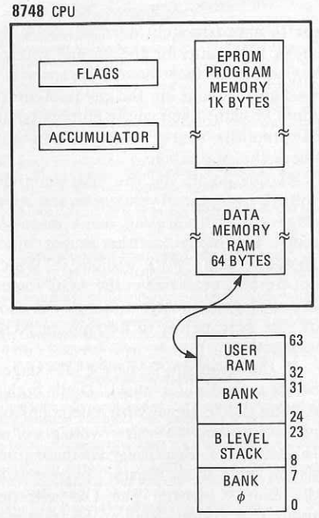

Fig. 3

The 8748's instructions include both 1- and 2-byte instructions plus the usual complement of arithmetic, logical, data movement, and conditional and unconditional jumps. Since 70% of the instructions are only 1 byte long, the MCS-48 microprocessors provide efficient programming within the limitations of the relatively small RAM storage and program area. **R-E**