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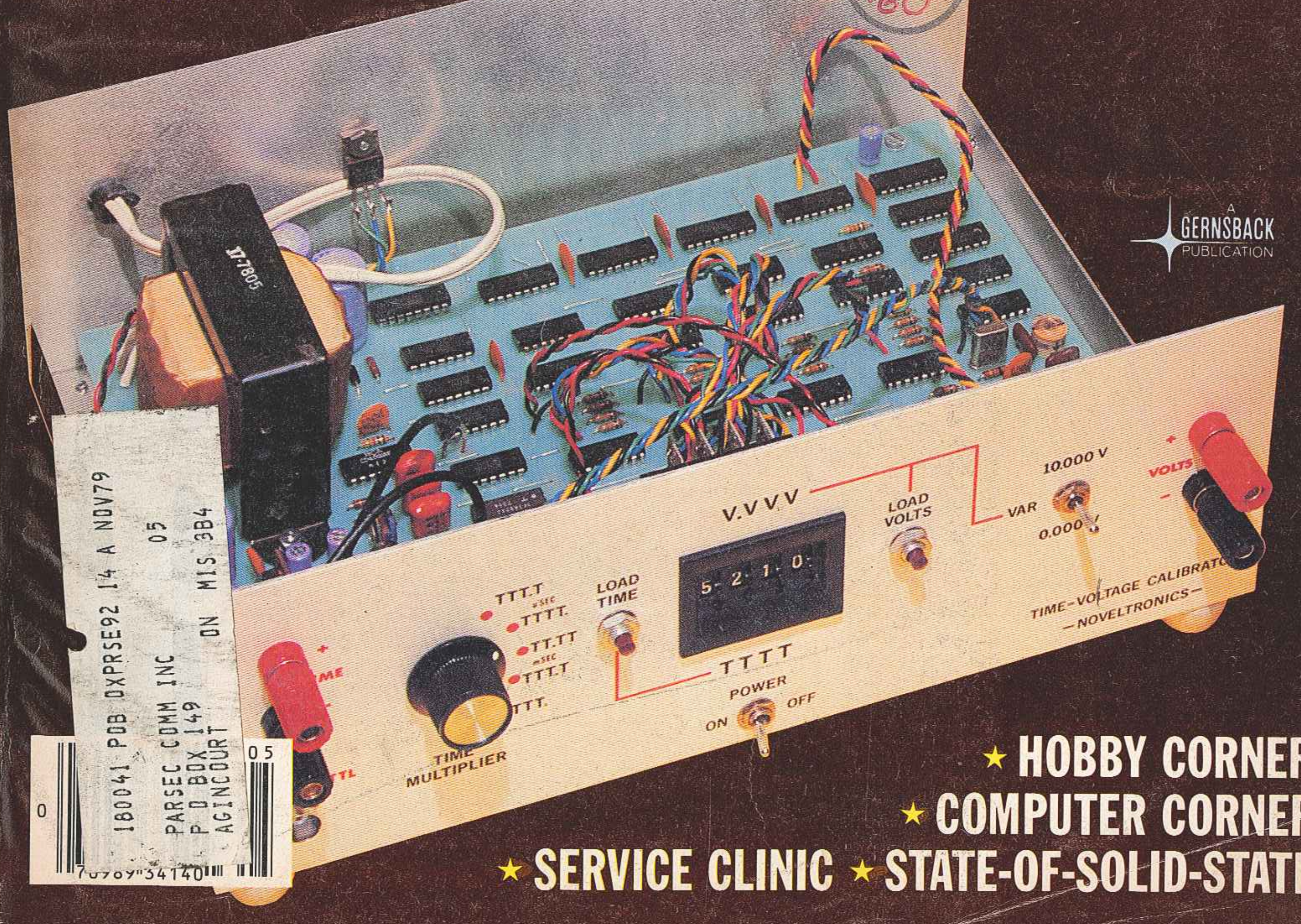

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computer corner

Direct Memory Access—a look at what it is and how it's used.

D. LARSEN, P. RONY, J. TITUS AND C. TITUS*

DIRECT MEMORY ACCESS (DMA) IS A TECHnique that allows a computer user to have direct access to individual memory locations without first having to go through the computer's central processing unit (CPU). The DMA interfacing technique has a number of uses, but few computer users completely understand it, and even fewer have fully implemented it for scientific data acquisition or control purposes.

A fairly elementary calculation shows that a simple software routine that inputs an 8-bit word and transfers it to a memory location will take many microseconds. Furthermore, if additional 8-bit words are to be taken and stored in some sort of a sequential file, additional software steps are needed for such "housekeeping" tasks as counting the number of words, incrementing the address pointer, etc. When these additional software steps are introduced into the test program, an 8-bit data word may only be acquired every 30 to 40 μs. In many cases, however, higher data-acquisition or data-transfer rates are required. Providing a direct access to the memory section of the computer is not a new idea. A DMA scheme was incorporated in Digital Equipment Corporation's popular PDP-8 minicomputer series. Additional hardware was required and interfacing was not particularly easy to do.

Most current microcomputers have a built-in DMA capability that is rarely considered. This capability allows microcomputers to be used in high-speed data-acquisition systems where the data-transfer rates are higher than those that can be achieved under program control. How is this possible?

Most microprocessor IC's, such as the 8080, Z-80 and 8085, have data-bus and address-bus outputs that are three-state. Three-state devices can pass normal logic 1 or logic 0 levels, and they can also be forced into a third logic state, in which their outputs appear to be very high-impedance loads on the bus. Thus, they no longer sink or source current and they are, in effect, disconnected from the bus. This third logic state allows external devices to obtain the use of the address and data bus lines when the computer's operations are suspended, and its outputs are removed from the bus lines. It is easy to control the microcomputer's bus signals to force them into this third state. The 8080 has a HOLD input. When this input is driven to a logic 1, it forces the 8080 to complete its current operation and then place its data-bus and address-bus outputs in their third state. A handshaking hold-acknowledge (HLDA) signal is output by the 8080 to indicate that it has actually placed these signals in the high-impedance state.

External devices that wish to make use of the address and data-bus lines are synchronized so that they will not attempt to use the bus lines until they receive the hold-acknowledge signal from the 8080. In general, these same devices have generated the bus-use request signal or hold signal that indicates to the 8080 that they want to use the buses. In many microcomputer systems, additional buffers are used between external devices and the address-bus and data-bus connections to the microprocessor IC itself. If this is the case, it is very important to make sure that these buffers sense the hold-acknowledge signal and place their respective outputs in the third state also. In the HOLD state, the CPU and its associated buffer circuitry must all be disconnected from the address and data buses.

External devices that are configured for DMA transfers generally have their own registers that provide address data, usually in 16-bit format. These address registers also have three-state outputs, which are normally disabled. They are enabled (or turned on) only when the 8080 is in the HOLD state. Then, they can use the address bus to address the particular memory location to or from which they wish to transfer data. The data path between the external device and the memory IC's has also been placed in the third state, so it also can be used for transferring data—in this case, the 8-bit value that will be transferred between the external device and the location being addressed by the external three-state address registers.

One other important detail must be discussed before the actual data transfer can take place. In most microcomputer systems, the reading-from and writing-to operations are controlled by two signals, memory-read ($\overline{MEMR}$ or $\overline{MR}$) and memory-write ($\overline{MEMW}$ or $\overline{MW}$). These signals may, or may not, be available with three-state outputs. In some systems, where a control-logic section has been constructed with discrete IC's, these two signals probably will not have three-state outputs. When a system controller IC has been used, the outputs are probably three-state devices. In either case, it is easy to gate an 8080-generated read or write pulse with the corresponding pulse generated by the microprocessor IC. In this way, either the external hardware, *or* the microprocessor can generate a read or a write signal. Since the 8080 processor does not operate or execute program steps while it is in the HOLD mode, it cannot generate a read or a write signal. By using the HLDA signal to enable the read and write signals generated by the external device, the proper signals will be generated by either the 8080 in the normal mode and by the external device in the HOLD mode.

While the DMA interface described thus far does not seem to be very useful, since it transfers only one 8-bit data word to a single location, it *does* illustrate the simplicity with which a DMA interface can be constructed. In most situations, however, a block of data will be transferred between the memory and an external device. Note that the transfer may be in either direction—i.e., from a high-speed data-acquisition device to the computer memory, or from the computer's memory to a high-speed data-storage device, such as a floppy disc.

In one application, a series of SN74193 programmable up-down counters were used to provide the 16-bit address information during the DMA transfer, and a first-in/first-out (FIFO) buffer memory was used to provide a block of data to the microcomputer's memory. Some simple control logic generated a write pulse (MEMW) and then incremented the address (count) present at the SN74193

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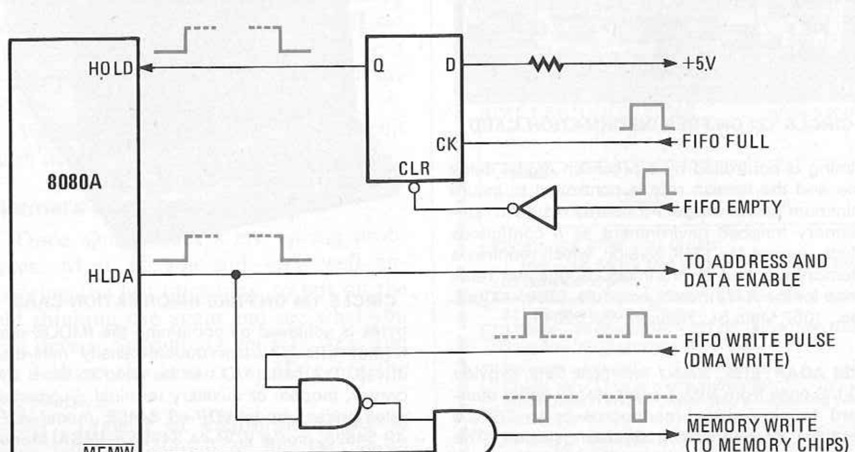

FIG. 1

*This article is reprinted courtesy American Laboratories. Dr. Rony, Department of Chemical Engineering, and Mr. Larsen, Department of Chemistry, are with the Virginia Polytechnic Institute & State University. Both Mr. J. Titus and Dr. C. Titus are with Tychon, Inc.

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counters. A series of switches allowed presetting the starting address at which the block of data was to be stored. Once a complete block of data was accumulated in the 256-byte long FIFO memory, external circuitry was used to detect the FIFO FULL condition, and to initiate the request for the use of the bus, asserting the HOLD line to the 8080. When the 8080 acknowledged the HOLD mode with the HLDA signal, the data was transferred from the FIFO memory to the microcomputer's main read/write memory at a rate of 500K bytes-per-second, or one byte every 2 μs. This data-transfer rate could have been increased at least fourfold, but it was unnecessary in this particular case.

Figure 1 is the block diagram of the interface that was used to control the DMA data transfers.

The DMA interfacing technique is also used in front-panel control circuits. Control panels are often provided on microcomputers so that memory locations can be addressed and the user can examine their content. The user may elect to "deposit" new data in one or more memory locations, again through via a front panel. A simple front-panel control system is easily constructed using the DMA technique,

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between the injector emitter and the N region, and the junction between the N region and the base of the NPN.

The current sources serve as high impedances to the driving collectors. This very efficient arrangement allows compact use of the IC area because of the numerous devices contained in a single N-isolated area compared with the noninverted single transistor-per-collector isolation ratio. In addition, because of the injector PNP current sources, there is a complete absence of resistors in this logic scheme.

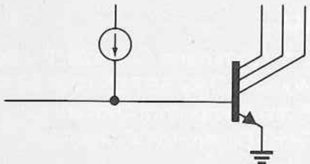

FIG. 3

The deep N+ region shown at the extreme right of Fig. 2 does not have a counterpart in the conventional transistor shown in Fig. 1. This area is a guard band that prevents parasitic currents from flowing to the wrong places.

We can now see how inverted transistors are used to implement a typical logic function. Figure 4 shows how output currents from several collectors are summed by simply connecting them together at the base of a transistor. Along with the inverter transistor, this connection creates a wired NAND gate. If currents i1, i2 and i3 are all 0, current source I1 turns on Q4 and its output voltage is 0.

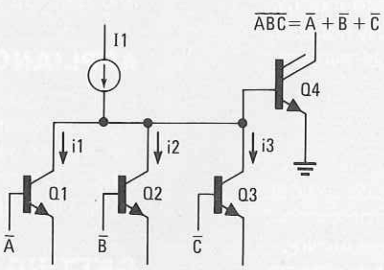

FIG. 4

If any of the three input currents is nonzero, Q4 is turned off and its collector swings high. In other words, current i1, i2 or i3 switches Q4's collector low. Using inverter transistors Q1, Q2 and Q3 creates an AND function. Assume the inputs to the transistors are A, B and C. Their collector currents are summed at the base of Q4, which swings high only when the three driving transistors are off—this is the AND function. You'll also observe that the NAND function, $\overline{ABC}$, is equivalent to $\overline{A} + \overline{B} + \overline{C}$.

Ignition circuit

Motorola's MC3333 *Vari-Dwell* ignition circuit uses a flux-averaging sensor instead of automotive points. The addition of the MJ10012, a Darlington driver transistor, to supply the high-energy ignition coil plus some resistors and capacitors complete the ignition system. The circuit operates from battery voltages from 4 to 24. Dwelltime and overvoltage shutdown are externally programmable.

Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036.

New power devices

The RCA 9113 NPN power-transistor series is designed for high-voltage switching applications. Its specific uses are for switch-mode power supplies, inverters, converters, pulse-width-modulated regulators and motor controls. These transistors are rated to 400 volts V_{CEO} and have switching speeds in the range of 1 μs. RCA Solid State Division, Box 3200, Somerville, NJ 08876.

Hitachi has developed complementary power audio-equipment MOSFET's that it expects to market at the end of the year as the *models HS8401* and *HS8402.*

Newly developed technology such as ion implantation adds the high-voltage and high gain necessary in power amps. The company claims these devices have greater frequency response and reliability compared with conventional power transistors. Their high-speed switching capability reduces distortion and dissipation to a greater degree than bipolar transistors. **R-E**

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since a 16-bit three-state buffer can be used to supply the address and eight indicators can be used to show the state of each bit in the memory location addressed. Eight logic switches are used to load new data into a location and two control switches, EXAMINE and DEPOSIT, are configured to generate the memory-read and memory-write control pulses, respectively. Additional features can be added to such a simple control circuit to automatically increment or decrement the 16-bit memory address, etc.

There are, however, some words of caution that must be noted when considering the use of DMA. The 8080 microprocessors are locked out of performing any program steps while they are in the HOLD state.

Some microprocessors such as the MC6800 series require that DMA-based devices regularly relinquish control of the bus. The three-state control (TSC) line in 6800-based systems can only be asserted for periods of 5 μs at a time. Similarly, in systems that use dynamic read/write memory devices, the address and data buses cannot be used continuously by DMA-based devices for more than 1 ms or so. **R-E**